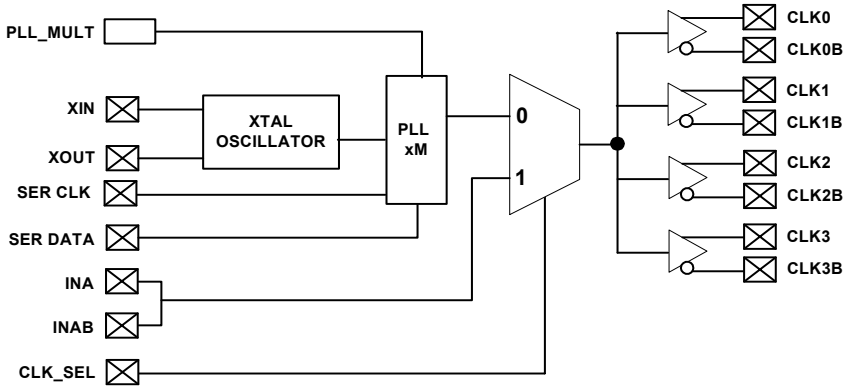
CY2XP304

High-Frequency Programmable PECL Clock Generation Module

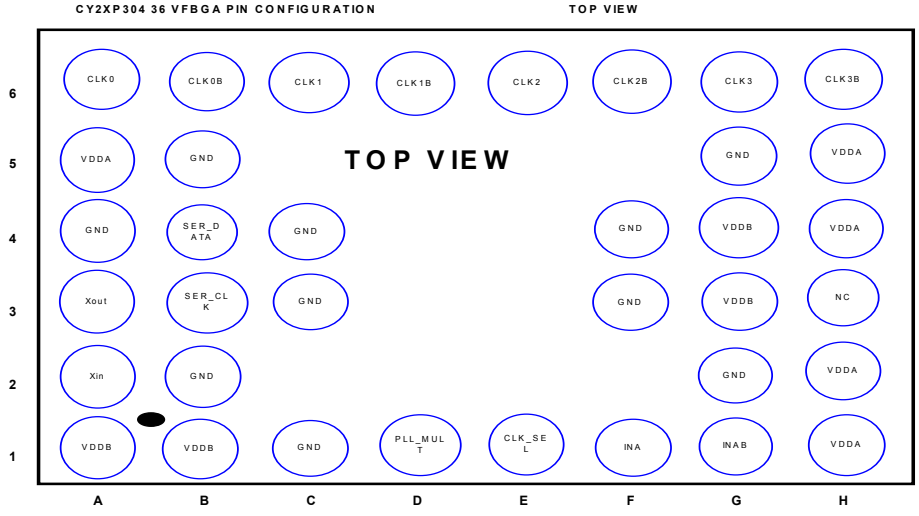
Features

- Period jitter peak-peak 125MHz(max.) = 55 ps
- Four low-skew LVPECL outputs
- Phase-locked loop (PLL) multiplier select
- Serially-configurable multiply ratios
- Eight-bit feedback counter and six-bit reference counter for high accuracy
- HSTL inputs—HSTL-to-LVPECL level translation
- 125- to 500-MHz output range for high-speed applications
- High-speed PLL bypass mode to 1.5 GHz
- 36-VFBGA, 6 × 8 × 1 mm
- 3.3V operation

Block Diagram



Pin Configuration



Pin Definitions

Pin #	Pin Name	Pin Description
A1,B1,G3,G4	VDDB	**3.3V Power Supply for Crystal Driver**
A2	XIN	**Reference Crystal Input**
A3	XOUT	**Reference Crystal Feedback**
A4,B2,C1,C3,C4,F3,F4,G2,G5,B5	GND	**Ground**
A5,H1,H2,H4,H5	VDDA	**3.3V Power Supply**
A6	CLK0	**LVPECL Clock Output**
B6	CLK0B	**LVPECL Clock Output** (Complement)
C6	CLK1	**LVPECL Clock Output**
D6	CLK1B	**LVPECL Clock Output** (Complement)
E6	CLK2	**LVPECL Clock Output**
F6	CLK2B	**LVPECL Clock Output** (Complement)
G6	CLK3	**LVPECL Clock Output**
H6	CLK3B	**LVPECL Clock Output** (Complement)
B3	SER_CLK	**Serial Interface Clock**
B4	SER_DATA	**Serial Interface Data**
D1	PLL_MULT	**PLL Multiplier Select Input**, Internal pull-up resistor, see *Frequency Table*
E1	CLK_SEL	**Clock Select Input, Internal Pull down**. HIGH select INA/INAB, Internal PLL is bypassed. LOW select internal PLL
F1,G1	INA,INAB	**Differential Clock Input pair**, used in PLL-bypassed mode
H3	NC	**No Connect**

Frequency Table

PLL_Mult	M (PLL Multiplier)	Example Input Crystal Frequency	CLK[0:3],CLKB[0:3]
0	x16	25 MHz	400 MHz
		31.25 MHz	500 MHz
1	x8	15.625 MHz	125 MHz

CY2XP304 Two-Wire Serial Interface

Introduction

The CY2XP304 has a two-wire serial interface designed for data transfer operations, and is used for programming the P and Q values for frequency generation. S_{clk} is the serial clock line controlled by the master device. S_{data} is a serial bidirectional data line. The CY2XP304 is a slave device and can either read or write information on the dataline upon request from the master device.

Figure 1 shows the basic bus connections between master and slave device. The buses are shared by a number of devices and are pulled HIGH by a pull-up resistor.

Serial Interface Specifications

Figure 2 shows the basic transmission specification. To begin and end a transmission, the master device generates a start signal (S) and a stop signal (P). Start (S) is defined as switching the S_{data} from HIGH to LOW while the S_{clk} is at HIGH. Similarly, stop (P) is defined as switching the S_{data} from LOW to HIGH while holding the S_{clk} HIGH. Between these two signals, data on S_{data} is synchronous with the clock on the S_{clk}. Data is allowed to change only at LOW period of clock, and must be stable at the HIGH period of clock. To acknowledge, drive the S_{data} LOW before the S_{clk} rising edge and hold it LOW until the S_{clk} falling edge.

Serial Interface Format

Each slave carries an address. The data transfer is initiated by a start signal (S). Each transfer segment is one byte in length. The slave address and the read/write bit are first sent from the master device after the start signal. The addressed slave device must acknowledge (Ack) the master device. Depending on the Read/Write bit, the master device will either write data into (logic 0) or read data (logic 1) from the slave device. Each time a byte of data is successfully transferred, the receiving device must acknowledge. At the end of the transfer, the master device will generate a stop signal (P).

Serial Interface Transfer Format

Figure 2 shows the serial interface transfer format used with the CY2XP304. Two dummy bytes must be transferred before the first data byte. The CY2XP304 has only three bytes of latches to store information, and the third byte of data is reserved. Extra data will be ignored.

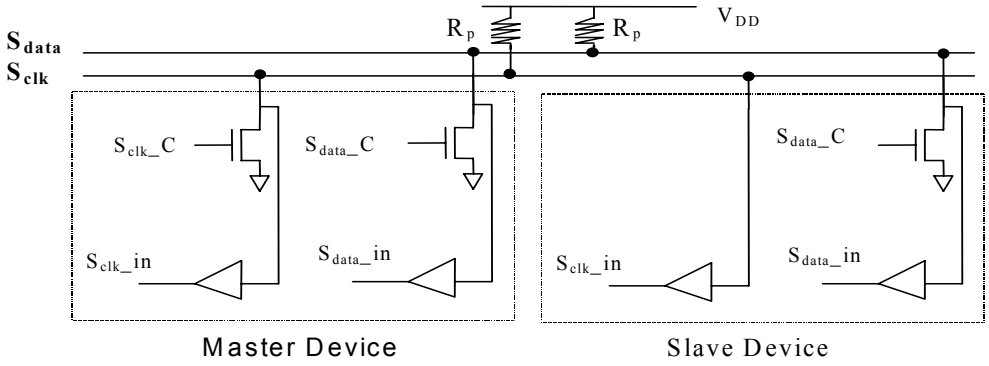


Figure 1. Device Connections

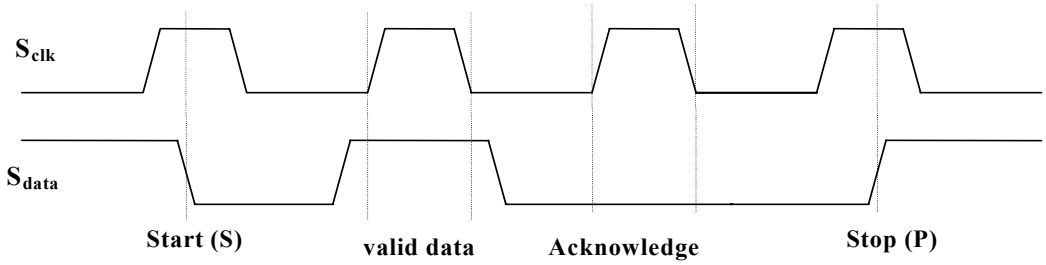


Figure 2. Serial Interface Specifications

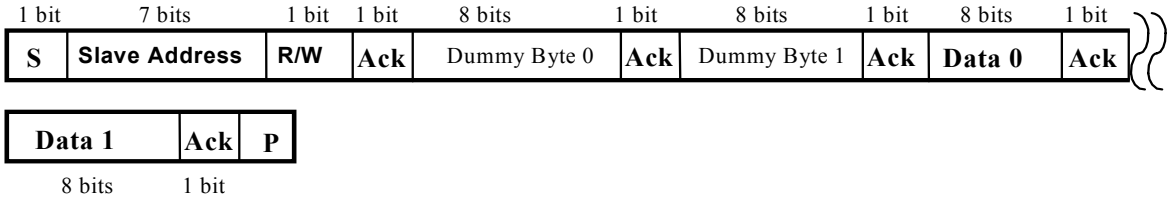


Figure 3. CY2XP304 Transfer Format

Serial Interface Address for the CY2XP304

A6	A5	A4	A3	A2	A1	A0	R/W
1	1	0	0	1	0	1	0

Serial Interface Programming for the CY2XP304

	b7	b6	b5	b4	b3	b2	b1	b0
Data0	QCNTBYP	SELPQ	Q<5>	Q<4>	Q<3>	Q<2>	Q<1>	Q<0>
Data1	P<7>	P<6>	P<5>	P<4>	P<3>	P<2>	P<1>	P<0>
Data2	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

To program the CY2XP304 using the two-wire serial interface, set the SELPQ bit HIGH. The default setting of this bit is LOW. The P and Q values are determined by the following formulas:

$P_{final} = (P_{7..0} + 3) * 2$

$Q_{final} = Q_{5..0} + 2$

If the QCNTBYP bit is set HIGH, then Q_{final} defaults to a value of 1. The default setting of this bit is LOW.

If the SELPQ bit is set LOW, the PLL multipliers will be set using the values in the Select Function Table.

CyberClocks™ has been developed to generate P and Q values for stable PLL operation. This software is downloadable from www.cypress.com.

PLL Frequency = Reference x P/Q = Output

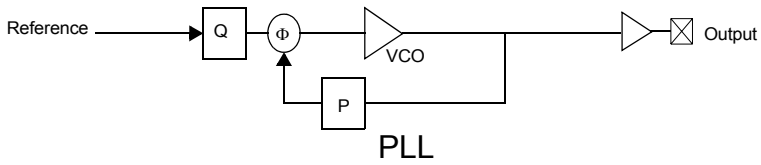


Figure 4. PLL Block Diagram

Functional Specifications

Crystal Input

The CY2XP304 receives its reference from an external crystal. Pin XIN is the reference crystal input, and pin XOUT is the reference crystal feedback. The parameters for the crystal are given on page 5 of this data sheet. The oscillator circuit requires external capacitors. Please refer to the application note entitled *Crystal Oscillator Topics* for details.

Select Input

There are two select input pins, the PLL_MULT and CLK_SEL. PLL_MULT pin selects the frequency multiplier in the PLL, and is a standard LVCMOS input. The S pin has an internal pull-up resistor. The multiplier selection is given on page 2 of this data sheet (see *Frequency Table).*

State Transition Characteristics

Specifies the maximum settling time of the CLK and CLKB outputs from device power-up. For V_{DD} and V_{DDX} any sequences are allowed to power-up and power-down the CY2XP304.

State Transition Characteristics

From	To	Transition Latency	Description
V_{DD}/V_{DDX} On	CLK/CLKB Normal	3 ms	Time from V_{DD}/V_{DDX} is applied and settled to CLK/CLKB outputs settled.

Absolute Maximum Conditions

Parameter	Description	Condition	Min.	Max.	Unit
V_{CC}	Supply Voltage	Non-functional	–0.3	4.6	V
V_{CC}	Operating Voltage	Functional	3.135	3.465	V
VTT	Output Termination Voltage	Relative to V_{CC}[1]	V_{CC} – 2		V
V_{IN}	Input Voltage	Relative to V_{CC}[1]	–0.3	V_{CC} + 0.3	V
V_{OUT}	Output Voltage	Relative to V_{CC}[1]	–0.3	V_{CC} + 0.3	V
LU_I	Latch Up Immunity	Functional	100		mA
T_S	Temperature, Storage	Non-functional	–65	+150	°C
T_A	Temperature, Operating Ambient	Functional	–40	+85	°C
T_J	Temperature, Junction	Non-functional	–	150	°C
$Ø_{Jc}$	Dissipation, Junction to Case	Functional	11.38		°C/W
$Ø_{Ja}$	Dissipation, Junction to Ambient	Functional	85.83		°C/W
ESD_h	ESD Protection (Human Body Model)		2000		V
M_{SL}	Moisture Sensitivity Level		3		N.A.
G_{ATES}	Total Functional Gate Count	Assembled die	50		Ea.

Crystal Requirements

Requirements to use parallel mode fundamental xtal. External capacitors are required in the crystal oscillator circuit. Please refer to the application note entitled *Crystal Oscillator Topics* for details.

Crystal Requirements

Parameter	Description	Min.	Max.	Unit
X_F	Frequency	10	31.25	MHz

DC Electrical Specifications

Parameter	Description	Min.	Max.	Unit
V_{DD}	Supply voltage	3.135	3.465	V
V_{IL}	Input signal low voltage at pin PLL_MULT	–	0.35	V
V_{IH}	Input signal high voltage at pin PLL_MULT	0.65	–	V
R_{PUP}	Internal pull-up resistance	10	100	kΩ
t_{PU}	Power-up time for all V_{DD}s to reach minimum specified voltage (power ramps must be monotonic)	0.05	500	ms

Operating Conditions

Parameter	Description	Min.	Max.	Unit
T_A	Commercial Temperature	0	70	°C
	Industrial Temperature	–40	85	°C

Note:
1. Where V_{CC} is 3.3V±5%

DC Specifications (V_{CC} = 3.3 V ± 5%, Commercial and Industrial temp.)

Parameter	Description	Condition	Min.	Max.	Unit
Clock Input Pair INA, INAB (HSTL differential signals)					
V_{DIF}	HSTL Differential Input Voltage[2]		0.4	1.9	V
V_X	HSTL Differential Crosspoint Voltage[3]		0.68	0.9	V
I_{IN}	Input Current	$V_{IN} = V_X \pm 0.2V$		|150|	uA
PECL Outputs CLK[0:3], CLK[0:3]B (PECL differential signals)					
V_{OL}	Output Low Voltage V_{CC} = 3.3V ± 5%	I_{OL} = –5 mA[4]	V_{CC} – 1.995	V_{CC} – 1.5	V
V_{OH}	Output High Voltage	I_{OH} = –30 mA[4]	V_{CC} – 1.25	V_{CC} – 0.7	V
Supply Current and V_{BB}					
I_{EE}	Maximum Quiescent Supply Current without Output Termination Current			150	mA
C_{IN}	Input Pin Capacitance	INA, INAB		3	pF
L_{IN}	Pin Inductance			1	nH

AC Electrical Specifications–Input

Parameter	Description	Min.	Max.	Unit
f_{IN}	Input frequency with driven reference, crystal inputs	1	133	MHz
$f_{XTAL,IN}$	Input frequency with crystal input	10	31.25	MHz
f_{INA_IN}	Input Frequency with INA/INAB inputs	0	1500	MHz
$C_{IN,CMOS}$	Input capacitance at PLL_MULT pin[5]	–	10	pF

AC Specifications–PECL Clock Outputs CLK[0:3], CLK[0:3]B

Parameter	Description	Conditions	Min.	Max.	Unit
f_O	Output Frequency	CLK_SEL = 0	125	500	MHz
		CLK_SEL = 1	0	1500	MHz
$Vo_{(P-P)}$	Differential output voltage (peak-to-peak)	f_O < 1GHz	0.375	–	V
V_{CMRO}	Output Common Voltage Range		V_{CC} – 1.425		V
$tsk_{(O)}$	Output-to-output skew	400-MHz 50% duty cycle Standard load Differential Operation	–	50	ps
$tsk_{(PP)}$	Part-to-part output skew	400-MHz 50% duty cycle Standard load Differential Operation	–	150	ps
T_R,T_F	Output Rise / Fall time	400-MHz 50% duty cycle Differential 20% to 80%	–	0.3	ns
DC	Long-term average output duty cycle		45	55	%
$t_{DC,ERR}$	Cycle-cycle duty cycle error at x8 with 15.625-MHz input		–	70	ps
Phase Noise	Phase Noise at 10 kHz (x8 mode) @ 125 MHz		–107	–92	dBc
BW_{LOOP}	PLL Loop Bandwidth		50		kHz (–3 dB)

Notes:
2. V_{DIF} (DC) is the amplitude of the differential HSTL input voltage swing required for device functionality.
3. V_X (DC) is the crosspoint of the differential HSTL input signal. Functional operations is obtained when the crosspoint is within the V_X (DC) range and the input swing lies within the V_{DIF} (DC) specification.
4. Equivalent to a termination of 50Ω to V_{TT}.
5. Capacitance measured at freq. = 1 MHz, DC Bias = 0.9V, and VAC < 100 mV.

AC Specifications–PECL Clock Outputs CLK[0:3], CLK[0:3]B (continued)

Parameter	Description	Conditions	Min.	Max.	Unit
t_{JCRMS}	Cycle-to-cycle RMS jitter	At 125-MHz frequency	–	15	ps
		At 400-MHz frequency	–	10	ps
		At 500-MHz frequency	–	12	ps
t_{JCPK}	Cycle-to-cycle jitter (pk-pk)	At 125-MHz frequency	–	95	ps
		At 200-MHz frequency, XF = 25 MHz	–	65	ps
		At 400-MHz frequency	–	55	ps
		At 500-MHz frequency	–	65	ps
t_{JPRMS}	Period jitter RMS	At 125-MHz frequency	–	6.8	ps
		At 400-MHz frequency	–	5.6	ps
		At 500-MHz frequency	–	6.8	ps
t_{JPPK}	Period jitter (pk-pk)	At 125-MHz frequency	–	55	ps
		At 200-MHz frequency, XF = 25 MHz	–	50	ps
		At 400-MHz frequency	–	45	ps
		At 500-MHz frequency	–	50	ps
t_{JLT}	Long term RMS Jitter (P < 20)	At 125-MHz frequency	–	25	ps
		At 400-MHz frequency	–	20	ps
		At 500-MHz frequency	–	25	ps
t_{JLT}	Long term RMS Jitter (20 < P < 40)	At 125-MHz frequency	–	55	ps
		At 400-MHz frequency	–	65	ps
		At 500-MHz frequency	–	55	ps
t_{JLT}	Long-term RMS Jitter (40 < P < 60)	At 125-MHz frequency	–	70	ps
		At 400-MHz frequency	–	90	ps
		At 500-MHz frequency	–	65	ps

AC Electrical Specifications–PECL Clock Outputs: PLL Bypass Mode

Parameter	Description	Conditions	Min	Max	Unit
$Vo_{(P-P)}$	Differential output voltage (peak-to-peak)	Differential PRBS fo < 1.0 GHz	0.375	–	V
J_P	Period Jitter	660 MHz 50% duty cycle Standard load	–	1.3	ps r.m.s.
T_{PD}	Propagation delay (INA/INAB to output)	PECL, 660MHz	280	650	ps
		HSTL, <1 GHz	280	750	ps

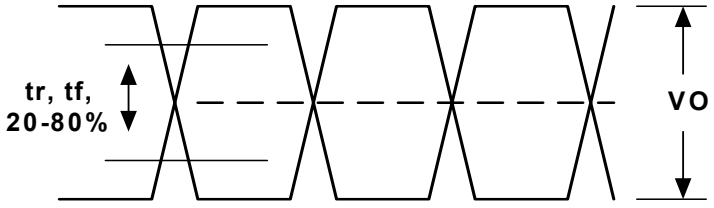


Figure 5. ECL/LVPECL Output

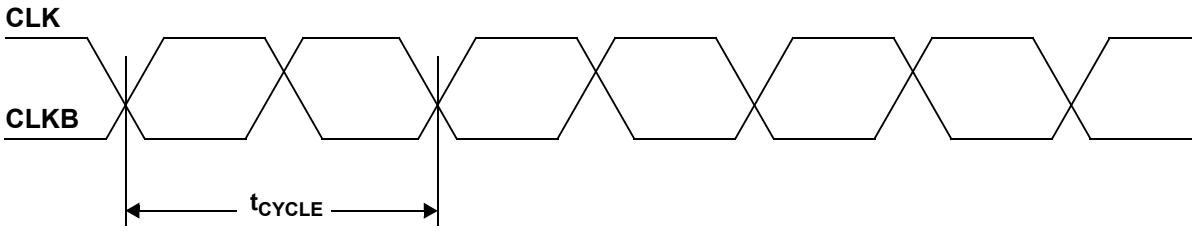
Jitter

This section defines the specifications that relate to timing uncertainty (or jitter) of the input and output waveforms. *Figure 6* shows the definition of period jitter with respect to the falling edge of the CLK signal. Period jitter is the difference between the minimum and maximum cycle times over many cycles (typically 12800 cycles at 400 MHz). Equal requirements apply for rising edges of the CLK signal. t_{JP} is defined as the output period jitter.

Figure 7 shows the definition of cycle-to-cycle jitter with respect to the falling edge of the CLK signal. Cycle-to-cycle jitter is the difference between cycle times of adjacent cycles over many cycles (typically 12800 cycles at 400 MHz). Equal requirements apply for rising edges of the CLK signal. t_{JC} is defined as the clock output cycle-to-cycle jitter.

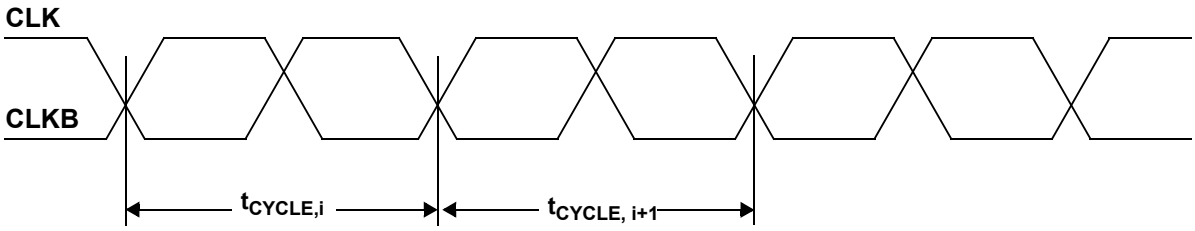
Figure 8 shows the definition of cycle-to-cycle duty cycle error. Cycle-to-cycle duty cycle error is defined as the difference between high-times of adjacent cycles over many cycles (typically 12800 cycles at 400 MHz). Equal requirements apply to the low-times. $t_{DC,ERR}$ is defined as the clock output cycle-to-cycle duty cycle error.

Figure 9 shows the definition of long-term jitter error. Long-term jitter is defined as the accumulated timing error over many cycles (typically 12800 cycles at 400 MHz). It applies to both rising and falling edges. t_{JLT} is defined as the long-term jitter.



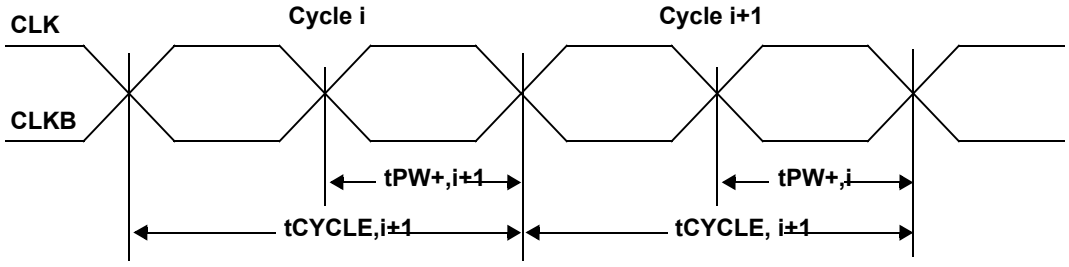
$t_{JP} = t_{CYCLE,max} - t_{CYCLE,\ min.\ over\ many\ cycles}$

Figure 6. Period Jitter



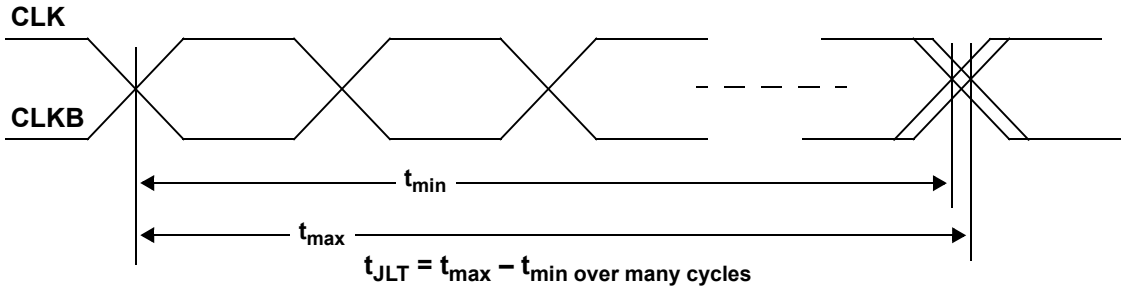
$t_{JC} = t_{CYLCE,i} - t_{CYCLE,i+1}$ over many consecutive cycles

Figure 7. Cycle-to-cycle Jitter



$t_{DC,ERR} = t_{PW+,i} - t_{PW+,i+1}$ over many consecutive cycles

Figure 8. Cycle-to-cycle Duty Cycle Error



$t_{JLT} = t_{max} - t_{min}$ over many cycles

Figure 9. Long-term Jitter

Test Configurations

Standard test load using a differential pulse generator and differential measurement instrument.

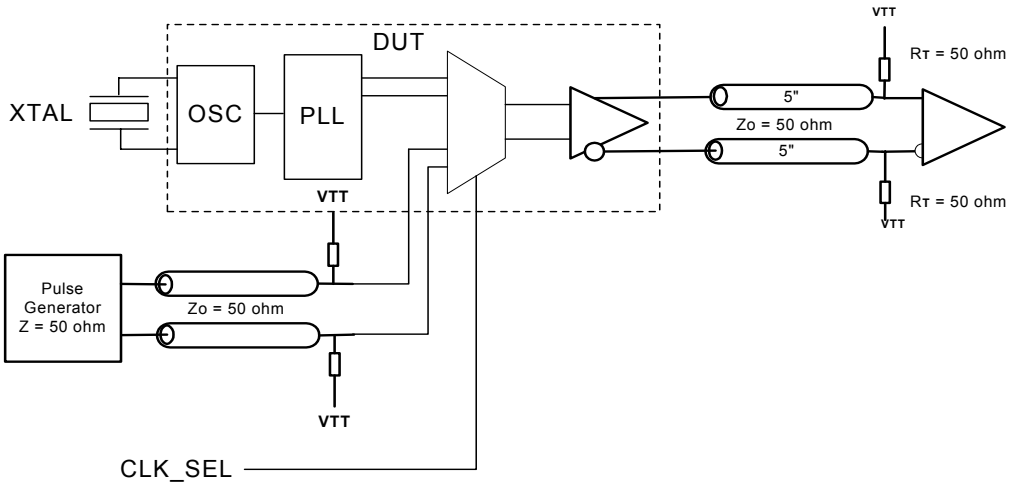


Figure 10. CY2XP304 AC Test Reference

Applications Information

Termination Examples

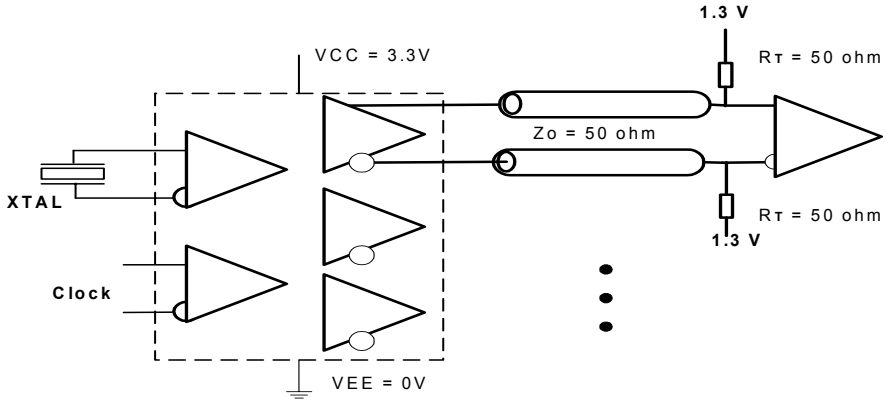


Figure 11. Standard LVPECL–PECL Output Termination

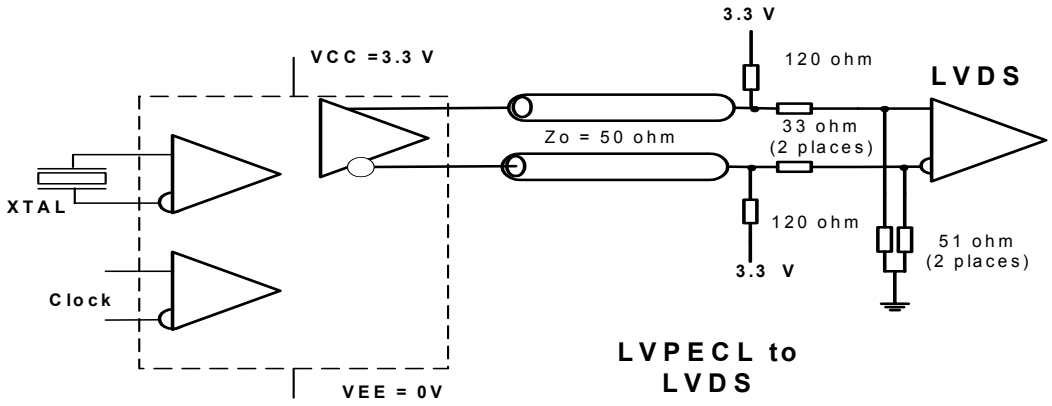


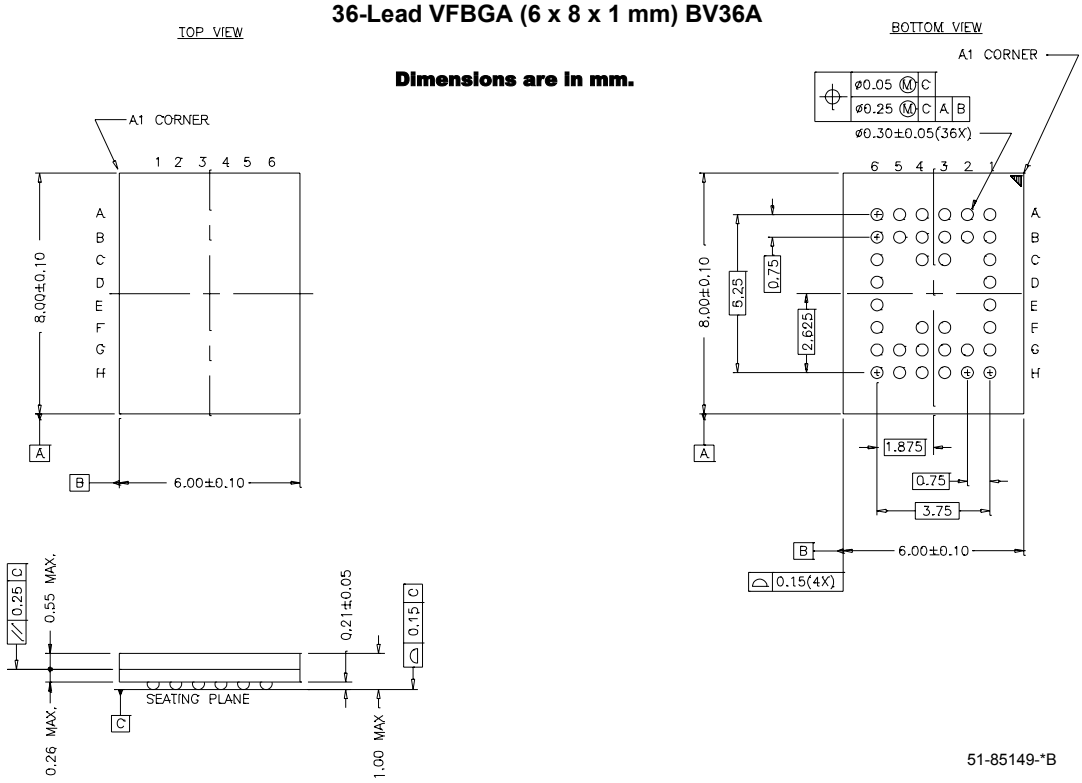
Figure 12. Low-Voltage Positive Emitter-Coupled Logic (LVPECL) to a Low-voltage Differential Signaling (LVDS) Interface

Ordering Information

Ordering Code	Package Type	Operating Range	Operating Voltage
CY2XP304BVC	36-lead VFBGA	Commercial, to 400 MHz	3.3V
CY2XP304BVCT	36-lead VFBGA – Tape and Reel	Commercial, to 400 MHz	3.3V
CY2XP304BVI	36-lead VFBGA	Industrial, to 400 MHz	3.3V
CY2XP304BVIT	36-lead VFBGA – Tape and Reel	Industrial, to 400 MHz	3.3V

Package Drawing and Dimensions

36-Lead VFBGA (6 x 8 x 1 mm) BV36A



Document History Page

Document Title: CY2XP304 High-Frequency Programmable PECL Clock Generation Module Document Number: 38-07589				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	129898	12/02/03	RGL	New Data Sheet
*A	235868	See ECN	RGL	Updated Jitter spec based on the characterization report
*B	247601	See ECN	RGL/GGK	Changed V_{OH} and V_{OL} to match the Char Data