512Kx32 Static RAM CMOS, High Speed Module

FEATURES

- 512Kx32 bit CMOS Static RAM
- Random Access Memory
  - Access Times: 15, 20, and 25ns
  - Individual Byte Selects
  - Fully Static, No Clocks
  - TTL Compatible I/O
- High Density Package
  - 72 Pin ZIP, No. 173
  - 72 lead SIMM, No. 174 (Gold Option)
  - Common Data Inputs and Outputs
- Single +3.3V (±10%) Supply Operation

* This product is subject to change without notice.

DESCRIPTION

The EDI8F32512V is a high speed 16 Mb Static RAM module organized as 512K words by 32 bits. This module is constructed from four 512Kx8 Static RAMs in SOJ packages on an epoxy laminate (FR4) board.

Four chip enables (E0#-E3#) are used to independently enable the four bytes. Reading or writing can be executed on individual bytes or any combination of multiple bytes through proper use of selects.

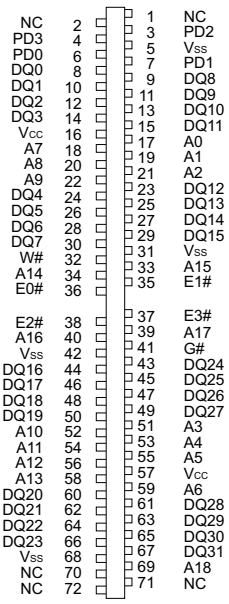
The EDI8F32512V is offered in 72 pin ZIP and 72 lead SIMM packages, which enable 16 Mb of memory to be placed in less than 1.3 square inches of board space.

All inputs and outputs are TTL compatible and operate from a single 3.3V supply. Fully asynchronous circuitry requires no clocks or refreshing for operation and provides equal access and cycle times for ease of use.

Pins PD0- PD3, are used to identify module memory density in applications where alternate modules can be interchanged.

FIG. 1

Pin Configurations and Block Diagram

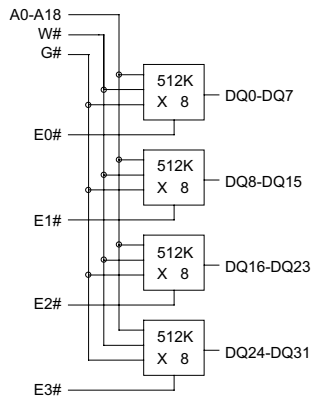


PD0, PD1, PD3= OPEN
PD2= V_{SS}

8G32512V Pin Config.

Pin Names

A0-A18	Address Inputs
E0#-E3#	Chip Enables
W#	Write Enable
G#	Output Enable
DQ0-DQ31	Common Data Input/Output
V_{CC}	Power (+3.3V±10%)
V_{SS}	Ground
NC	No Connectiona



8G32512V Blk Dia.

ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin relative to V_{SS}	-0.5V to 4.6V
Operating Temperature TA (Ambient)	
Commercial	0°C to +70°C
Storage Temperature, Plastic	-55°C to +125°C
Power Dissipation	2.5 Watts
Output Current	20 mA

*Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

Parameter	Sym	Min	Typ	Max	Units
Supply Voltage	V_{CC}	3.0	3.3	3.6	V
Supply Voltage	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.2	--	V_{CC} +0.3	V
Input Low Voltage	V_{IL}	-0.3	--	0.8	V

AC TEST CONDITIONS

Input Pulse Levels	V_{SS} to 3.0V
Input Rise and Fall Times	5ns
Input and Output Timing Levels	1.5V
Output Load	1TTL, CL = 30pF

(Note: For t_{EHQZ},t_{GHQZ} and t_{WLQZ}, CL = 5pF)

DC ELECTRICAL CHARACTERISTICS

Parameter	Sym	Conditions	Min	Typ*	Max	Units
Operating Power Supply Current	$I_{CC}1$	W#, E# = V_{IL}, II/O = 0mA, Min Cycle			800	mA
Standby (TTL) Power Supply Current	$I_{CC}2$	E# $\geq$ V_{IH}, $V_{IN} \geq V_{IL}$ or $V_{IN} \geq V_{IH}$			240	mA
Full Standby Power Supply Current CMOS	$I_{CC}3$	E# $\geq$ V_{CC}-0.2V $V_{IN} \geq V_{CC}$=0.2V or $V_{IN} \geq$ 0.2V			40	mA
Input Leakage Current	I_{LI}	V_{IN} = 0V to V_{CC}	--	--	±20	µA
Output Leakage Current	I_{LO}	V I/O = 0V TO V_{CC}	--	--	±20	µA
Output High Voltage	V_{OH}	I_{OH} = -4.0mA	2.4	--	--	V
Output Low Voltage	V_{OL}	I_{OL} = 8.0mA	--	--	0.4	V

*Typical: TA = 25°C, V_{CC} = 5.0V

TRUTH TABLE

E#	W#	G#	Mode	Output	Power
H	X	X	Standby	HIGH Z	$I_{CC}2/I_{CC}3$
L	H	L	Read	D_{OUT}	$I_{CC}1$
L	L	X	Write	D_{IN}	$I_{CC}1$
L	H	H	Output Deselect	HIGH Z	$I_{CC}1$

CAPACITANCE

(f=1.0MHz, V_{IN}=V_{CC} or V_{SS})

Parameter	Sym	Max	Unit
Address Lines	CI	45	pF
Data Lines	CD/Q	20	pF
Chip Enable Line	CC	20	pF
Write Line	CN	45	pF

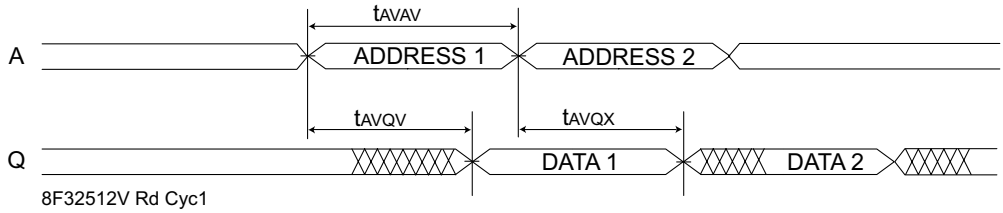
These parameters are sampled, not 100% tested.

AC CHARACTERISTICS READ CYCLE

Parameter	Symbol		15ns		20ns		25ns		Units
	JEDEC	Alt.	Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{AVAV}	t_{RC}	15		20		25		ns
Address Access Time	t_{AVQV}	t_{AA}		15		20		25	ns
Chip Enable Access	t_{ELQV}	t_{ACS}		15		20		25	ns
Chip Enable to Output in Low Z (1)	t_{ELQX}	t_{CLZ}	3		3		3		ns
Chip Disable to Output in High Z (1)	t_{EHQZ}	t_{CHZ}		7		10		12	ns
Output Hold from Address Change	t_{AVQX}	t_{OH}	3		3		3		ns
Output Enable to Output Valid	t_{GLQV}	t_{OE}		7		8		10	ns
Output Enable to Output in Low Z (1)	t_{GLQX}	t_{OLZ}	0		0		0		ns
Output Disable to Output in High (1)	t_{GHQZ}	t_{OHZ}		7		8		10	ns

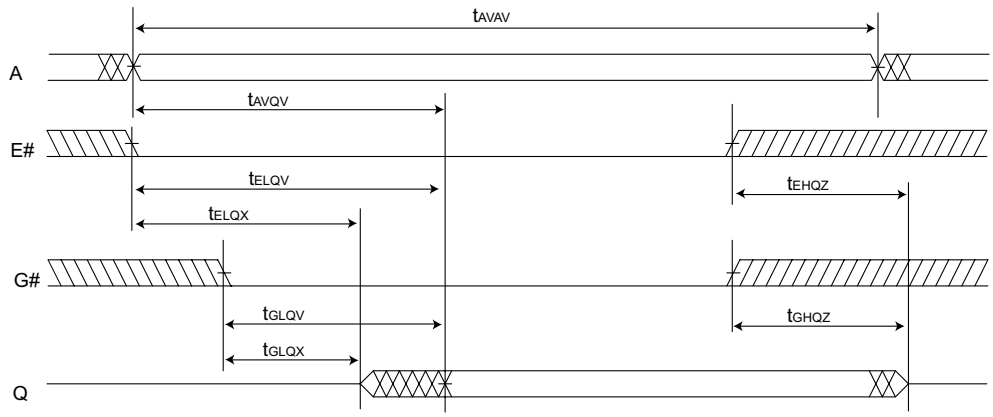
Notes: 1. Parameter guaranteed, but not tested.

FIG. 2
READ CYCLE 1 - W# HIGH, G#, E# LOW



8F32512V Rd Cyc1

FIG. 3
READ CYCLE 2 - W# HIGH



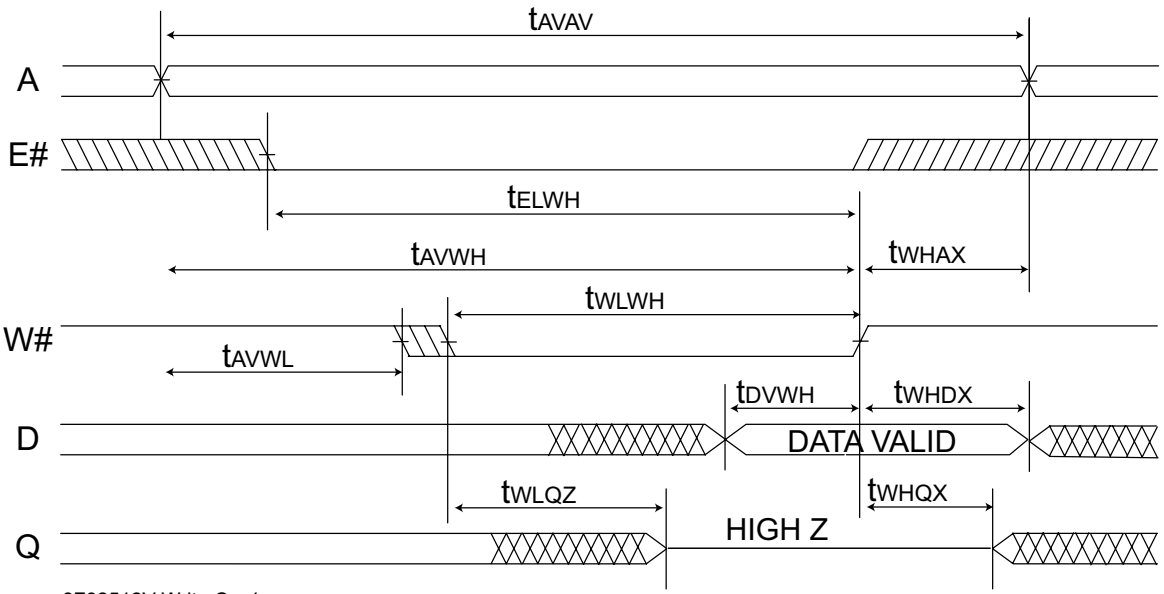
8F32512V Rd Cyc2

AC CHARACTERISTICS WRITE CYCLE

Parameter	Symbol		15ns		20ns		25ns		Units
	JEDEC	Alt.	Min	Max	Min	Max	Min	Max	
Write Cycle Time	t_{AVAV}	t_{WC}	15		20		25		ns
Chip Enable to End of Write	t_{ELWH} t_{WLEH}	t_{CW} t_{CW}	10 10		15 15		20 20		ns ns
Address Setup Time	t_{AVWL} t_{AVEL}	t_{AS} t_{AS}	0 0		0 0		0 0		ns ns
Address Valid to End of Write	t_{AVWH} t_{AHEH}	t_{AW} t_{AW}	10 10		15 15		15 15		ns ns
Write Pulse Width	t_{WLWH} t_{ELEH}	t_{WP} t_{WP}	10 10		15 15		15 15		ns ns
Write Recovery Time	t_{WHAX} t_{EHAX}	t_{WR} t_{WR}	0 0		0 0		0 0		ns ns
Data Hold Time	t_{WHDX} t_{EHDX}	t_{DH} t_{DH}	0 0		0 0		0 0		ns ns
Write to Output in High Z (1)	t_{WLQZ}	t_{WHZ}	0	6	0	8	0	12	ns
Data to Write Time	t_{DVWH} t_{DVEH}	t_{DW} t_{DW}	7 7		9 9		10 10		ns ns
Output Active from End of Write (1)	t_{WHQX}	t_{WLZ}	3		3		3		ns

Notes: 1. Parameter guaranteed, but not tested.

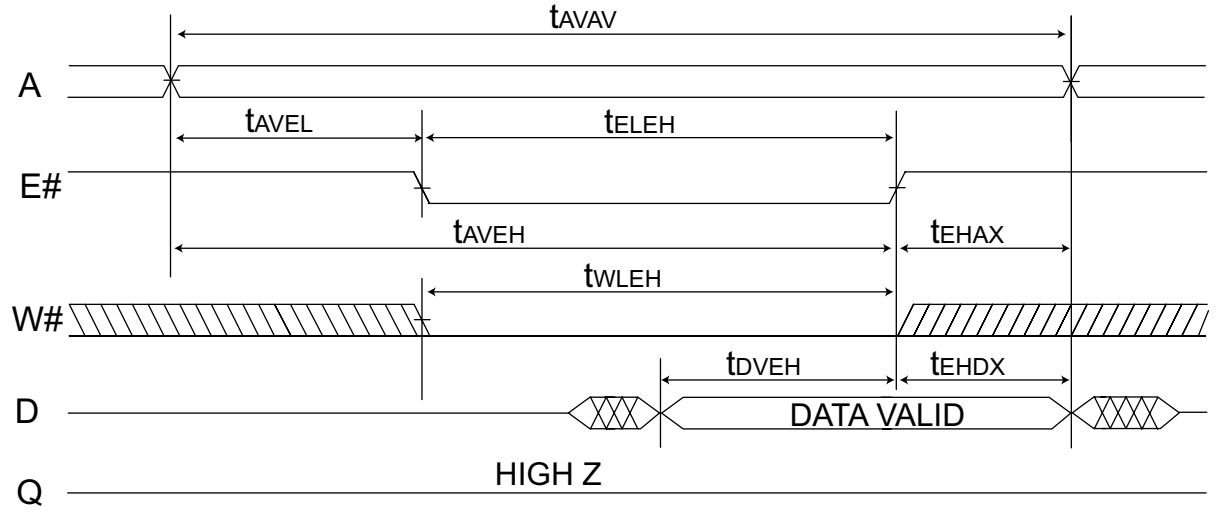
FIG. 4
WRITE CYCLE 1 - W# CONTROLLED



8F32512V Write Cyc1

FIG. 5

WRITE CYCLE 2 - E# CONTROLLED



8F32512V Write Cyc2

ORDERING INFORMATION

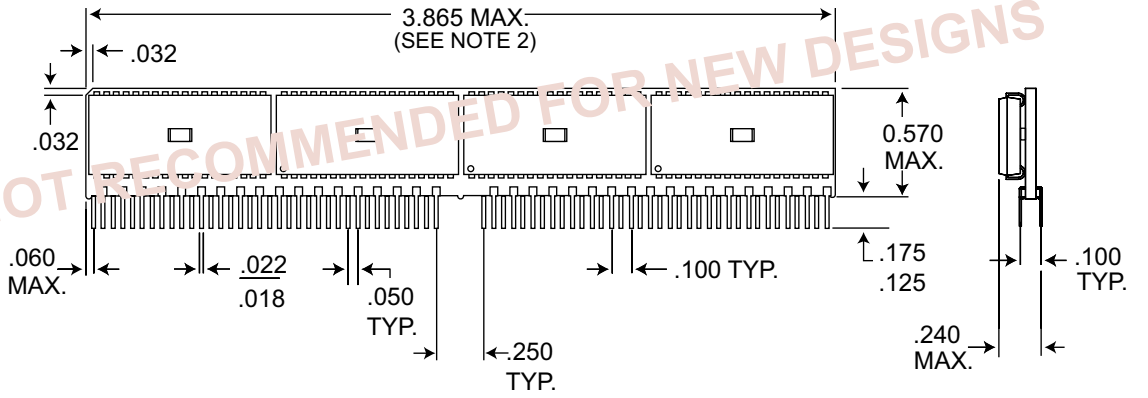
Part Number	Speed (ns)	Package No.
EDI8F32512V15MMC	15	174
EDI8F32512V20MMC	20	174
EDI8F32512V25MMC	25	174

Part Number	Speed (ns)	Package No.
EDI8F32512V15MZC	15	173
EDI8F32512V20MZC	20	173
EDI8F32512V25MZC	25	173

Note: To order gold SIMM option, change from "EDI8F" to "EDI8G".

PACKAGE DESCRPTION

PACKAGE NO. 173: 72 PIN ZIP



PACKAGE NO. 174: 72 LEAD SIMM