Ultra Low Power 8-pin Microcontroller

Features

- **True Low Power:** 4.0 µA active mode
  3.0 µA standby mode
  0.35 µA sleep mode
  @ 1.5V, 32kHz, 25°C
- **Low Supply Voltage 0.9 V to 5.5 V**
  - **Medium voltage version: 1.4V to 5.5V**
  - **Low voltage version: 0.9V to 1.8V**
- **No external component needed**
- **Available in TSSOP-8/14, SO-8/14 packages and die**
- **4-bit ADC or 12 levels Supply Voltage Level Detector (SVLD)**

- Max 4 (5*) outputs with 2 high drive outputs of 10mA
- Max. 5 (6*) inputs
- Sleep Counter Reset (automatic wake-up from sleep mode (EM patent))
- Mask ROM 1536 × 16 bits
- RAM 80 × 4 bits
- Internal RC oscillator 32 kHz – 800 kHz
- 2 clocks per instruction cycle
- 72 basic instructions
- External CPU clock source possible
- Watchdog timer (2 sec)
- Power-On-Reset with Power-Check on Start-Up
- 3 wire serial port , 8 bit, master and slave mode
- Universal 10-bit counter, PWM, event counter
- Prescaler down to 1 Hz (freq. = 32 kHz)
- Frequency output 1Hz, 2048 Hz, Fosc, PWM
- 6 internal interrupt sources (2×10-bit counter, 2× prescaler, SVLD, Serial Interface)
- 2 external interrupt sources (port A)

Description

The EM6682 is an ultra-low voltage, low power microcontroller coming in a package as small as 8-pin TSSOP and working up to 0.4 MIPS. It comes with an integrated 4-bit ADC and 2 high drive outputs of 10mA and it requires no external component. It has a sleep counter reset allowing automatic wake-up from sleep mode. It is designed for use in battery-operated and field-powered applications requiring an extended lifetime. A high integration level make it an ideal choice for cost sensitive applications.

The EM6682 contains the equivalent of 3kB mask ROM and a RC oscillator with frequencies between 32 and 800kHz selectable by metal option or register. It also has a power-on reset, watchdog timer, 10 bit up/down counter, PWM and several clock functions.

Tools include windows-based simulator and emulator. The EM6682 simulator is usable for most of the EM6682 functions.

Figure 1. Architecture

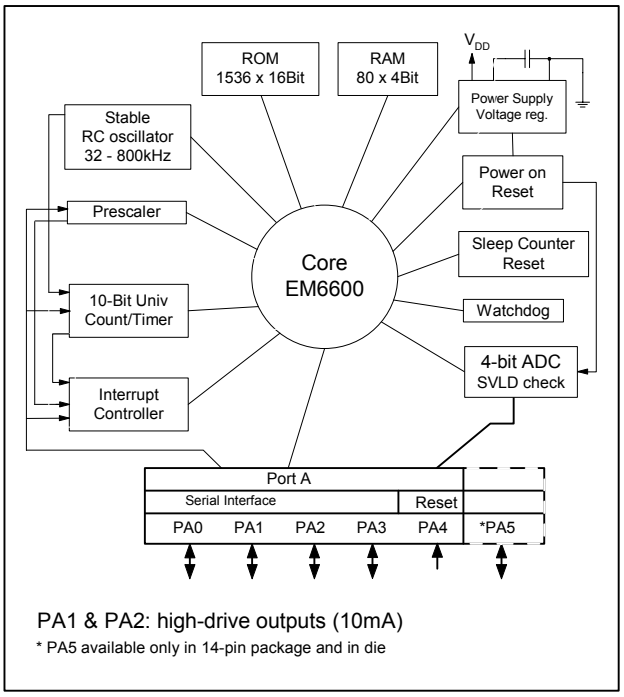
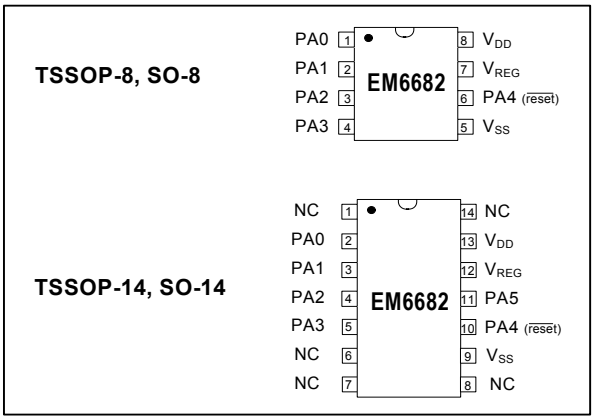


Figure 2. Pin Configuration



Typical Applications

- Household appliances
- Safety and security devices
- Automotive controls
- Sensor interfaces
- Watchdog
- Intelligent ADC
- Driver (LED, triac)

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EM6682 at a glance

❑ Power Supply
- Low voltage low power architecture including internal voltage regulator
- 1.4 V to 5.5 V in medium voltage version
- 0.9 V to 1.8 V in low voltage version
- 4.0 µA in active mode
- 3.5 µA in standby mode
- 0.35 µA in sleep mode @ 1.5V, 32kHz, 25°C

❑ RAM
- 80 x 4 bit, directly addressable

❑ ROM
- 1536 x 16 bit (~3k Byte), metal mask programmable

❑ CPU
- 4-bit RISC architecture
- 2 clock cycles per instruction (CPI=2)
- 72 basic instructions

❑ Main Operating Modes and Resets
- Active mode (CPU is running)
- Standby mode (CPU in halt, peripherals running)
- Sleep mode (no clock, reset state, data kept)
- Initial Power-On-Reset with Power-Check
- power-check after any reset settable by metal option
- Watchdog reset (logic)
- Reset terminal (software option on PA[3/4])
- Sleep Counter reset from Sleep mode
- Wakeup on change from Sleep mode

❑ Prescaler
- Divider (4 stages) to best fit CPU clock (32kHz – 1MHz to 32kHz system clock to keep peripherals timing close to specification
- 15 stage system clock divider from 32kHz down to 1Hz
- 2 Interrupt requests (3 different frequencies)
- Prescaler reset (4kHz to 1Hz)

❑ 8-Bit Serial Interface
- 3 wire (Clock, DataIn , DataOut) master/slave mode
- READY output during data transfer
- Maximum shift clock is equal to the main system clock
- Interrupt request to the CPU after 8 bit data transfer
- Supports different serial formats
- pins shared with general 4 bit PA[3:0] I/O port

❑ Oscillator
- RC Oscillator range: 32/50kHz to 500/800kHz (metal or register selectable from 32/50, 64/100, 128/200, 256/400 or 500/800 kHz typ. for CPU clock)
- No external components are necessary
- Temperature compensated
- External clock source possible from PA1

❑ 4(5)-Bit I/O PA[3:0] & PA[4] / PA[5]*
- Direct input read on the port terminals
- 2 Debounce function available muxed on 4 inputs
- 2 Interrupt request on positive or negative edge
- Pull-up or pull-down or none selectable by register, except PA[4] where pullup/down is mask or register selection
- 2 Test variables (software) for conditional jumps
- PA[1] and PA[3/4] are inputs for the event counter
- PA[3/4] Reset input (register selectable)
- All outputs can be put tri-state (default)
- Selectable pull-downs in input mode
- CMOS or Nch. open drain outputs
- Weak pull-up selectable in Nch. open drain mode

❑ 4-bit ADC & Voltage Level Det. (SVLD)
- External voltage compare from PA[4] input possible (low resolution 4 bit AD converter)
- Levels above Vdd min are available for SVLD
- Used for Power Check after POR (level 9 or level 5 selectable by metal option)
- Busy flag during measure
- Interrupt generated if SVLD measurement low

❑ 10-Bit Universal Counter
- 10, 8, 6 or 4 bit up/down counting
- Parallel load
- Event counting (PA[1] or PA[3/4])
- 8 different input clocks
- Full 10 bit or limited (8, 6, 4 bit) compare function
- 2 interrupt requests (on compare and on 0)
- Hi-frequency input on PA[1] and PA[3/4]
- Pulse width modulation (**PWM**) output
- Metal option for bit0 don't care, reduces timer by 1 bit

❑ Interrupt Controller
- 2 external and 6 internal interrupt request sources
- Each interrupt request can individually be masked
- Each interrupt flag can individually be reset
- Automatic reset of each interrupt request after read
- General interrupt request to CPU can be disabled
- Automatic enabling of general interrupt request flag when going into HALT mode

❑ Sleep Counter Reset (SCR)
- wake up the EM6682 from sleep mode
- 4 timings selectable by register
- Inhibit SCR by register

❑ Package form available
- TSSOP-8/14
- SO-8/14
- Die form (9 pin possible due to additional I/O pin)

NB: All frequencies written in this document are related to a typical system clock of 32 kHz !

Table of Contents

1. Pin Description for EM6682

Table 1 EM6682 pin descriptions

# On Chip	SO-8	Signal Name	Description
1	1	PA0	General I/O, serial In, Wake-Up on Change, IRQ source,…
2	2	PA1	General I/O, serial CLK, timer source, external clock
3	3	PA2	General I/O, serial Out, freq. out, CPU reset status output,…
4	4	PA3	general I/O, serial Rdy/Cs, Interrupt source, Reset
5	5	V_{ss}	ground – negative supply pin
6	6	PA4	general I, Reset, timer source, Interrupt source, Wake-Up, Compare I
7*	NC	PA5	general I/O, freq. Out, wake-up on change, IRQ source
8	7	V_{reg}	regulated voltage supported by 100nF tw. V_{ss}
9	8	V_{dd}	positive supply pin – capacitance tw. V_{dd} (C depends on V_{dd} noise)

Figure 3. Typical configuration for medium voltage version from 1.4V to 5.5V

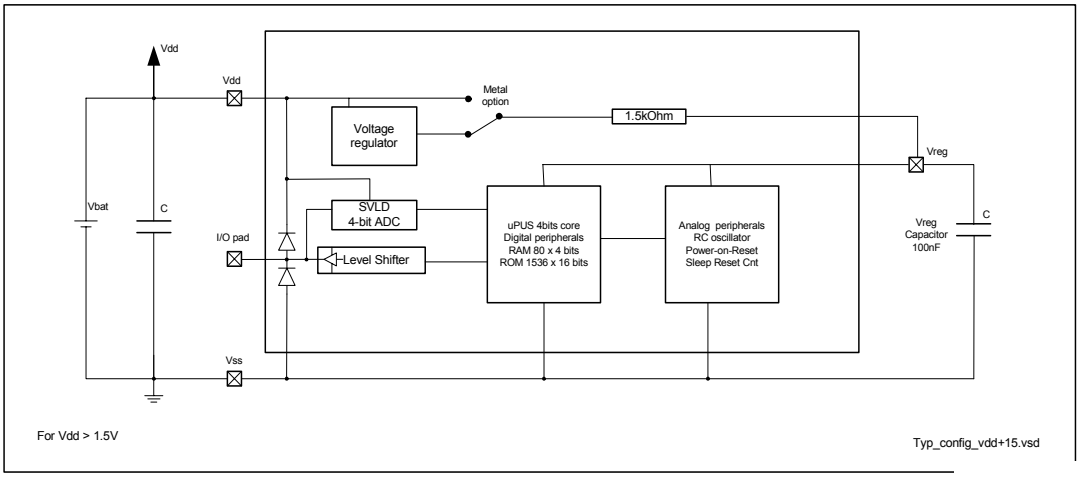
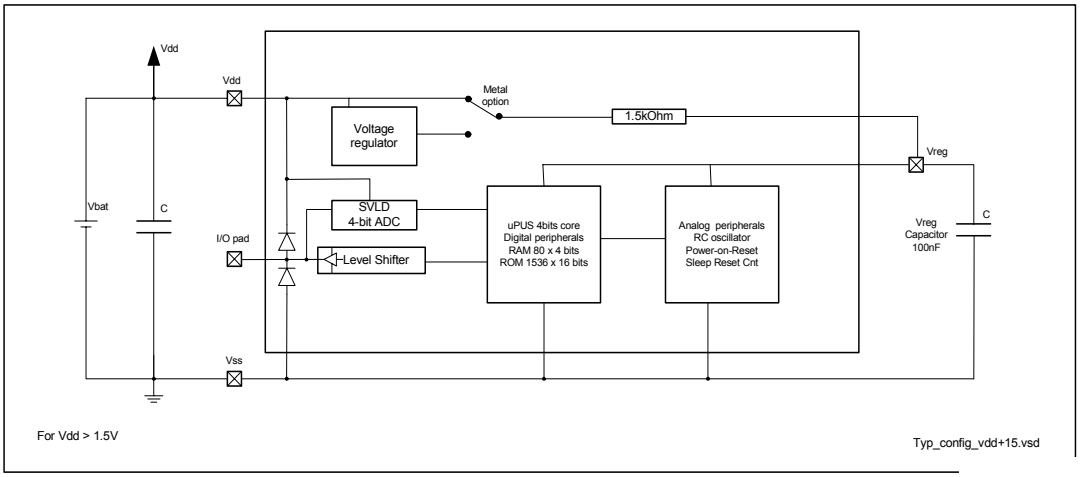


Figure 4. Typical configuration for low voltage version from 0.9V to 1.8V



NOTE: State of I/O pads may not be defined until V_{reg} reaches typ. 0.8V and Power-On-Reset logic supplied by V_{reg} clears them to Inputs.

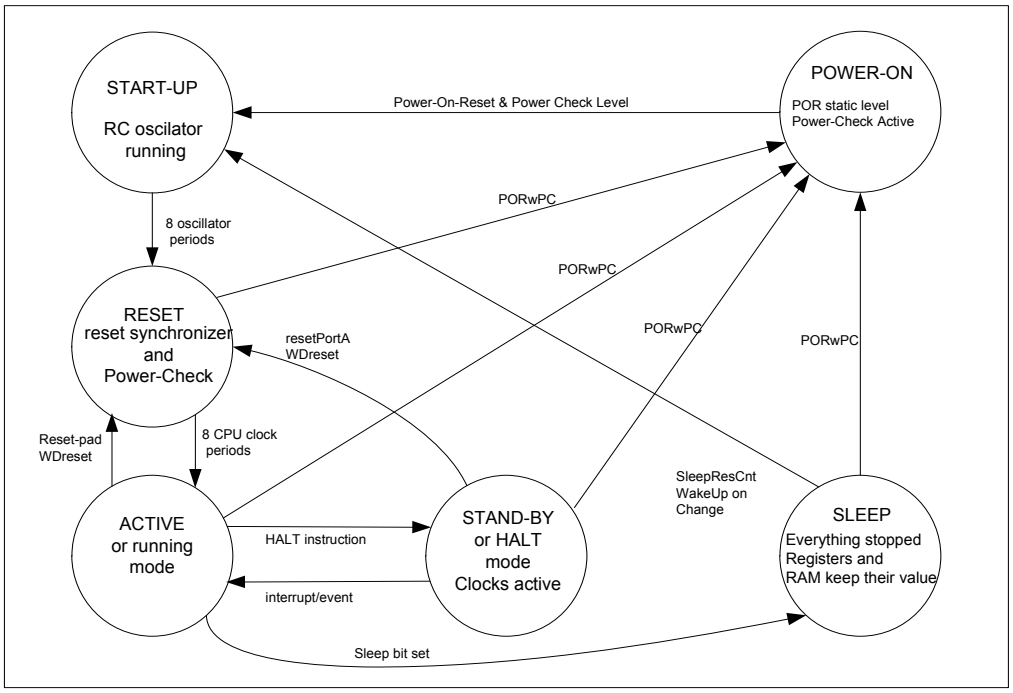
On I/O pins there are protective diodes towards V_{dd} and V_{ss}.

2. Operating modes

The EM6682 can operate in three different modes of which 2 are low-power dissipation modes (Stand-By and Sleep). The modes and transitions between them are shown in Figure 5.

1.) **Active** mode
2.) **Stand-By** mode
3.) **Sleep** mode

Figure 5. **EM6682** operating mode transitions



It is possible to initiate Power-Check at every reset by metal option. In this case, in order to change from reset state to active state, the supply voltage must be higher than the active Power-Check selection l
selection level corresponds to the SVLD level 5 (default) after power-up or to the SVLD level selection active at the end of the reset state.

2.1 ACTIVE Mode

The active mode is the actual CPU running mode. Instructions are read from the internal ROM and executed by the CPU. Leaving the active mode: via the halt instruction to go into standby mode, writing the **SLEEP** bit to go into Sleep mode or detecting the reset to go into reset mode.

2.2 STANDBY (Halt) Mode

Executing a HALT instruction puts the EM6682 into standby mode. The voltage regulator, oscillator, watchdog timer, interrupts, timers and counters are operating. However, the CPU stops since the clock related to instruction execution stops. Registers, RAM and I/O pins retain their states prior to STANDBY mode. STANDBY is cancelled by a RESET or an Interrupt request if enabled.

2.3 SLEEP Mode

Writing to the **Sleep** bit in the **RegSysCntl1** register puts the EM6682 in sleep mode. The oscillator stops and most functions of the EM6682 are inactive. To be able to write to the **Sleep** bit, the **SleepEn** bit in **RegSysCntl2** must first be set to "1". In SLEEP mode only the voltage regulator is active to maintain the RAM data integrity, all other functions are in reset state. SLEEP mode may be cancelled by Wake/Up on change, external reset or by Sleep Reset Counter if any of them is enabled.

Waking up from sleep mode may takes some time to guarantee stable oscillation. Coming back from sleep mode puts the EM6682 in reset state and as such reinitializes all registers to their reset value. Waking up from sleep mode clears the **Sleep** flag but not the **SleepEn** bit. Inspecting the **SleepEn** allows to determine if the EM6682 was powered up (**SleepEn** = "0") or woken from sleep mode (SleepEn = "1").

After every sleep mode, a Power-Check can be performed depending on metal option. The systems will only resume to active mode if the Power-Check condition is full-filled. The SVLD level which was selected at the time one entered sleep mode will be used as Power-Check level (exception: if during Sleep one has a POR condition then the default SVLD level will be applied.)

Table 2.3.1 Shows the Status of different EM6682 blocks in these three main operating modes.

Peripheral /// EM6682 mode	**ACTIVE** mode	**STAND-BY** mode	**SLEEP** mode
POR (static)	On	On	On
Voltage regulator	On	On	On (Low-Power)
RC-oscillator	On	On	Off
Clocks (Prescaler & RC divider)	On	On	Off
CPU	Running	In HALT – Stopped	Stopped
Peripheral register	"On"	"On" retain value	retain value
RAM	"On"	retain value	retain value
Timer/Counter	"On"	"On" if activated before	stopped
Supply Voltage Level Det.=SVLD	can be activated	"On" if activated before	Off
PortA / Reset pad debounced	Yes	Yes	No
Interrupts / events	Yes - possible	Yes – possible	No – not possible
Watch-Dog timer	On / Off (soft selectable)	On / Off (soft selectable)	No
Wake Up on Change PortA	No	No	On/Off (soft select.)
Sleep Reset Counter	Off	Off	On/Off (soft select.)

3. Power Supply

The EM6682 is supplied by a single external power supply between V_{dd} (V_{BAT}) and V_{SS} (ground). A built-in voltage regulator generates V_{reg} providing regulated voltage for the oscillator and the internal logic. The output drivers are supplied directly from the external supply V_{DD}. Internal power configuration is shown in Figure 3 and Figure 4.

To supply the internal core logic it is possible to use either the internal voltage regulator ($V_{reg} < V_{DD}$) or directly ($V_{reg} = V_{DD}$). The selection is done by metal 1 mask option. By default the voltage regulator is used. Refer to chapter 15 for the metal mask selection.

The internal voltage regulator is chosen for high voltage systems. It saves power by reducing the internal core logic's power supply to an optimum value. However, due to the inherent voltage drop over the regulator the minimal V_{DD} value is restricted to 1.4V .

A direct V_{DD} connection can be selected for systems running on a 1.5V battery. The 1.5kΩ resistor together with the external capacitor on V_{reg} is filtering the V_{dd} supply to the internal core. In this case the minimum V_{DD} value can be as low as 0.9V.

4. Reset

Figure 6. illustrates the reset structure of the EM6682. One can see that there are five possible reset sources :

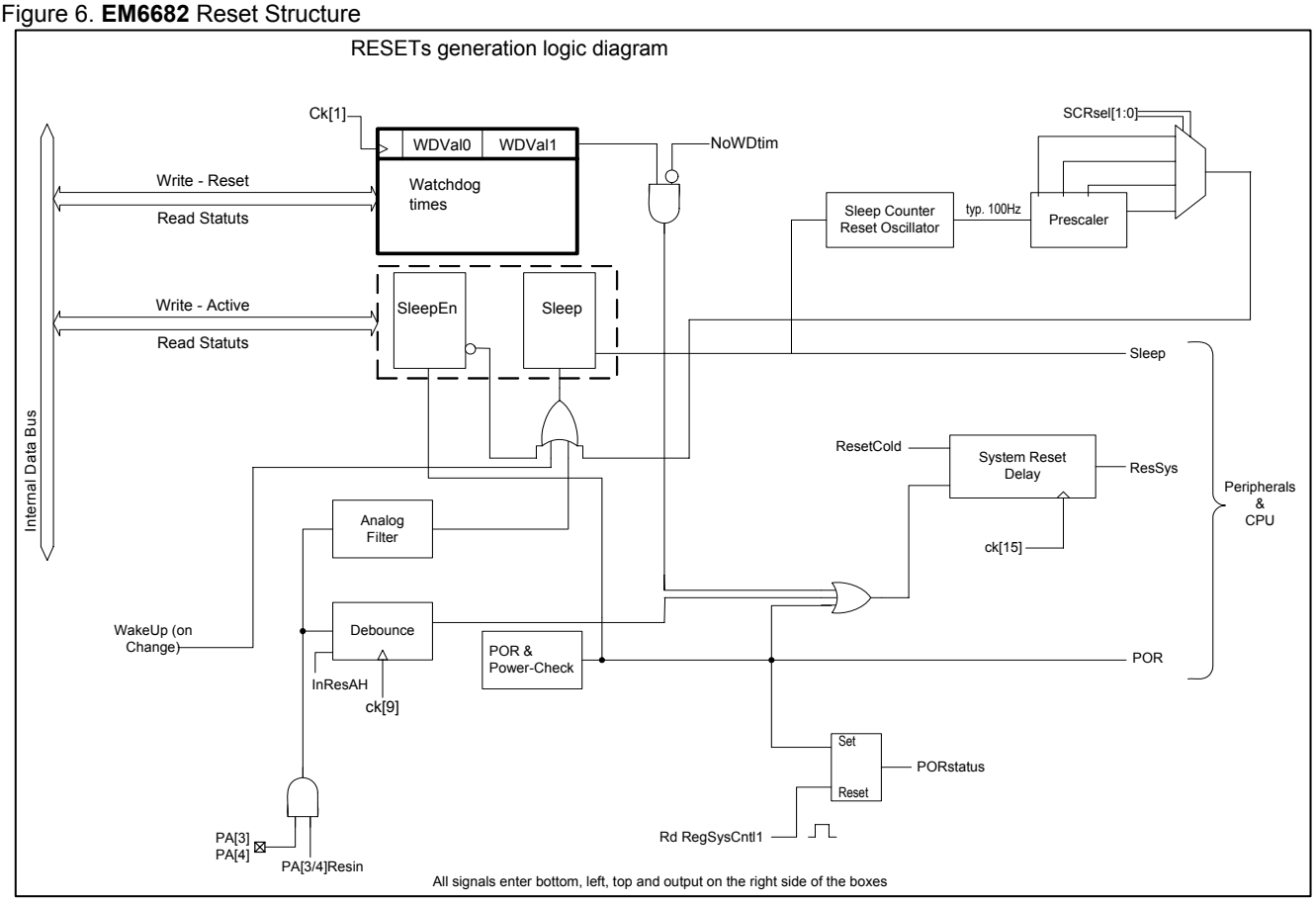
(1) Internal initial Power On Reset (POR) circuitry with Power-Check. → POR, ResetCold, System reset, ResetCPU
(2) External reset from PA[3/4] if software enabled → System Reset, Reset CPU
(3) Internal reset from the Digital Watchdog. → System Reset, Reset CPU
(4) Internal reset from the Sleep Counter Reset. → System Reset, Reset CPU
(5) Wake-Up on change from PA[0/5] or PA[3/4] if software enabled. → System Reset, Reset CPU

Table 4.1 Reset sources that can be used in different Operating modes

Reset Sources	**ACTIVE** mode	**STAND-BY** mode	**SLEEP** mode
POR (static) with Power Check	**Yes**	**Yes**	**Yes**
Software enabled reset on PA[3/4]	**XS** dig. debounce	**XS** dig. debounce	**XS** analog debounce
Digital Watch-Dog Timer	**XS**	**XS**	**No**
Sleep Counter Reset	**No**	**No**	**XS**
Wake Up on Change from Sleep	**No**	**No**	**XS**
Going in Sleep mode	**YES**	**No**	**No**

XS = software enable

Figure 6. **EM6682** Reset Structure



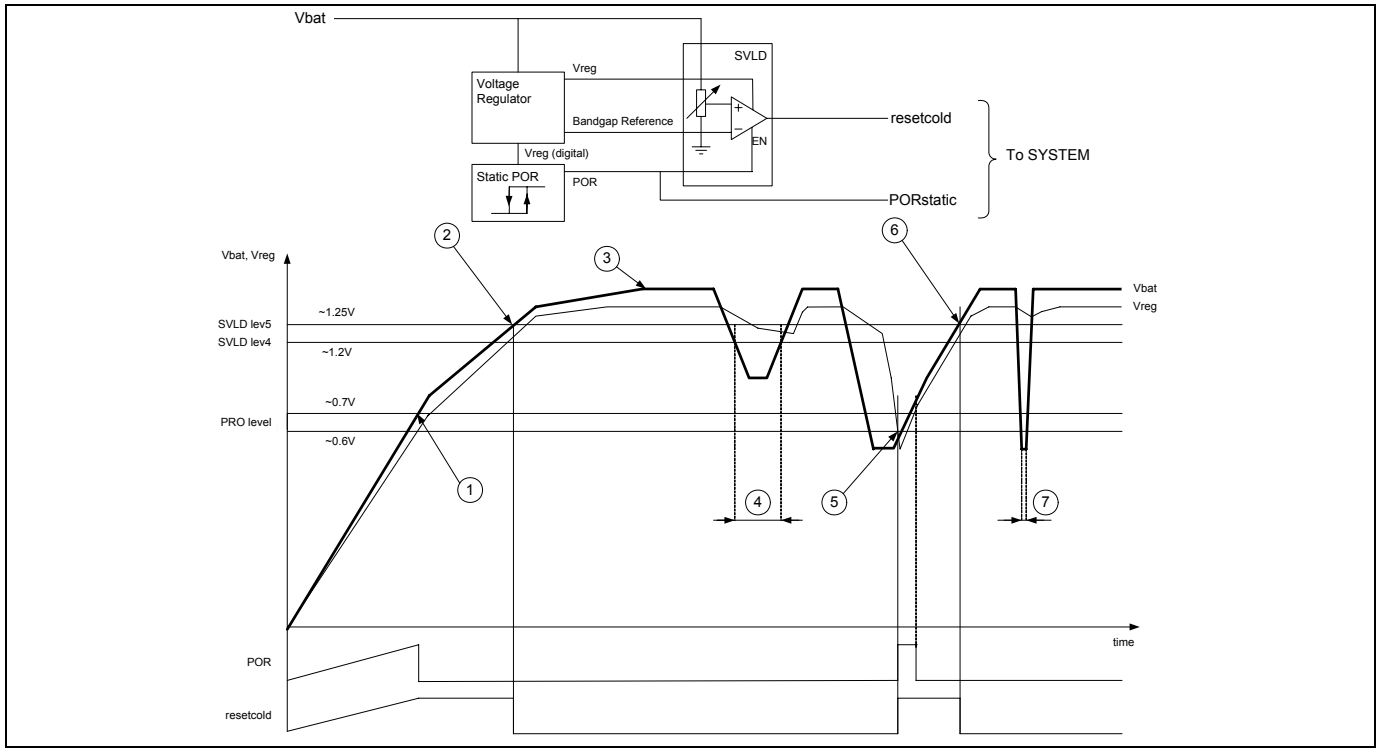
All reset sources activate the System Reset (ResSys). The 'System Reset Delay' ensures that the system reset remains active long enough for all system functions to be reset (active for N system clock cycles. CPU is reset by the same reset

As well as activating the system reset, the POR also resets all bits in registers marked '**p**' and the sleep enable (**SleepEn**) latch. System reset do not reset these registers bits, nor the sleep enable latch.

4.1 POR with Power-Check Reset

POR and Power-Check are supervising the $\mathbf{V_{reg}}$(digital) which follows more or less the $\mathbf{V_{dd}}$ supply voltage on start-up to guarantee proper operation after Power-On. The power check initiates a ***resetcold*** signal, which gets released when $\mathbf{V_{dd}}$ supply voltage is enough for the IC to function correctly.

Figure 7. **EM6682** ***resetcold*** signal as a result of Power-On-Reset and Power-Check



At power-on a POR cell with a static level of typ. 0.7V is checked. At time (1) in Figure 7. when the supply is increasing a power-check logic is switched-on with POR signal high. This logic enables the SVLD-level5 check which keeps ***resetcold*** active high until V_{dd} > SVLD-level5 (2). The circuit enters the active operating mode at (3). If afterwards V_{dd} drops below the selected SVLD-level4 (4) low supply will be detected, but this does not generate a POR signal. Low supply will be detected only if the measurement is done at time (4).

If V_{reg} drops below the static POR level of 0.60V when V_{dd} Supply is going down (POR static level has a hysteresys) then the POR and ***resetcold*** signals go high immediately (5) , SVLD level5 gets forced and power check is switched on. Because POR was done, the **Vld_lev[3:0]** was reset to value 0101, and Power-check makes ***resetcold*** inactive low again at 1.25V at time (6).

If there is only a very short V_{dd} drop (of few μs), below the POR level, POR will not react because V_{reg} is supported by external capacitance and it drops slower than V_{dd} and the logic still works (7).

IMPORTANT: special care should be taken, when Power Supply starts to fall close to or below V_{dd} min. Frequent checking of the SVLD level must be done. Below the minimum V_{dd} level specified in table 16.3 and figure 29 minimum V_{DD} =f(RC oscillator) on page 44 , the functionality of the circuit is not guaranteed.

To distinguish between POR reset and all other types of reset, the **PORstatus** bit in **RegSysCntl2** is set on at every POR and is cleared by writing the **RegSysCntl1** register.

With metal option SVLD level9 for power check @ 1.85V can be selected at higher RC oscillator frequencies to guarantee proper operation at higher frequencies.

Above mentioned levels and voltages are for 3V application which uses the internal voltage regulator. When the EM6682 is in low voltage mode the following levels apply. POR (with hysteresis) typically 1.0V at rising and 0.7V at falling Vreg voltage PowerCheck level (default) SVLD_level_9 is 1.1 V

4.2 Input Port A Reset

By writing the **PA[3/4]ResIn** in **RegFreqRst** registers the PA[3] or PA[4] input becomes dedicated for external reset. This bit is cleared by POR only. Which input is selected is set by **IrqPA[3l/4h]** bit from **RegPACntl2** register which is described in Chapter 6.

Bit **InResAH** in the **RegFreqRst** register selects the PA[3/4] reset function in Active and standby (Halt) mode. If set to '0' the PA[3/4] reset is inhibited. If Set to '1' than PA[3/4] input goes through a debouncer and needs to respect timing associated with the debounce clock selection made by **DebSel** bit in **RegPresc** register.

This **InResetAH** bit has no action in sleep mode, where a Hi pulse on PA[3/4] always immediately triggers a system reset.

Overview of control bits and possible reset from PA[3] or PA[4] is specified in table 4.2.1 below.

Table 4.2.1 Possible Reset from PA[3] or PA[4]

PA[3/4]ResIn	**InResAH**	**ACTIVE** or **STAND-BY** mode	**SLEEP** mode
0	**X**	NO reset from PA[3] or PA[4]	NO reset from PA[3] or PA[4]
1	**0**	NO reset from PA[3] or PA[4]	Reset with small analog filter
1	**1**	Debounce reset with debck of * Ck[14]/ Ck[11]/ Ck[8] needing 0.25 ms / 2 ms / 16ms Hi pulse typ.	Reset with small analog filter

***** Ck[14]/ Ck[11]/ Ck[8] are explained in chapter 5.2 Prescaler.

4.3 Digital Watchdog Timer Reset

The Digital Watchdog is a simple, non-programmable, 2-bit timer, that counts on each rising edge of Ck[1]. It will generate a system reset if it is not periodically cleared. The watchdog timer function can be inhibited by activating an inhibit digital watchdog bit (**NoWDtim**) located in **RegVLDCntl**. At power up, and after any system reset, the watchdog timer is activated.

If for any reason the CPU stops or stays in a loop where watchdog timer is not periodically cleared, it activates the system reset signal. This function can be used to detect program overrun, endless loops, etc. For normal operation, the watchdog timer must be reset periodically by software at least every 2.5 seconds (system clock = 32 KHz), or a system reset signal is generated.

The watchdog timer is reset by writing a '1' to the **WDReset** bit in the timer. This resets the timer to zero and timer operation restarts immediately. When a '0' is written to **WDReset** there is no effect. The watchdog timer also operates in standby mode and thus, to avoid a system reset, standby should not be active for more than 2.5 seconds.

From a System Reset state, the watchdog timer will become active after 3.5 seconds. However, if the watchdog timer is influenced from other sources (i.e. prescaler reset), then it could become active after just 2.5 seconds. It is therefore recommended to use the Prescaler **IRQHz1** interrupt to periodically reset the watchdog every second.

It is possible to read the current status of the watchdog timer in **RegSysCntl2**. After watchdog reset, the counting sequence is (on each rising edge of CK[1]) : '00', '01', '10', '11', {WDVal1 WDVal0}). When reaching the '11' state, the watchdog reset will be active within ½ second. The watchdog reset activates the system reset which in turn resets the watchdog. If the watchdog is inhibited it's timer is reset and therefore always reads '0'.

Table 4.3.1 Watchdog timer register **RegSysCntl2**

Bit	Name	Reset	R/W	Description
3	WDReset	0	W	Reset the Watchdog (The Read value is always '0') 1 → Resets the Logic Watchdog 0 → no action
2	*SleepEn*	*0*	*R/W*	*See Operating modes (sleep)*
1	WDVal1	0	R	Watchdog timer data 1/4 ck[1]
0	WDVal0	0	R	Watchdog timer data 1/2 ck[1]
3	PORstatus	1 P*	R	Power-On-Reset status

1 P* POR sets the PORstatus bit which is cleared by writing register **RegSysCntl1**

4.4 Sleep Counter Reset

To profit the most from Low Power Sleep Mode and still supervise the circuit surrounding, one can enable the Sleep Counter Reset which only runs in Sleep mode and periodically wakes up the EM6682. Four (4) different Wake-Up periods are possible as seen in table below.

Control bits **SleepCntDis** which is set to default '0'by POR enables the Sleep Counter when the circuit goes into Sleep mode. The **SCRsel1**, **SCRsel0** bits that are used to determine Wake-Up period are in the **RegSleepCR** register. To disable the Sleep Counter in Sleep mode **SleepCntDis** must be set to '1'.

Table 4.4.2 Register **RegSleepCR**

Bit	Name	Reset	R/W	Description
3	NoPullPA[4]	0 por	R/W	Remove pull-up/down from PA[4] input
2	SleepCntDis	0 por	R/W	Disable Sleep Reset Counter when Hi
1	SCRsel1	0 por	R/W	Selection bit 1 for Sleep RCWake-Up period
0	SCRsel0	0 por	R/W	Selection bit 0 for Sleep RCWake-Up period

Table 4.4.3 Wake-Up period from Sleep selection

	SCRsel1	**SCRsel0**	**Sleep Reset Counter period** (typ.)
	0	0	1.5 internal low speed RC clock periods
	0	1	15.5 internal low speed RC clock periods
	1	0	127.5 internal low speed RC clock periods
	1	1	1023.5 internal low speed RC clock periods

Refer to the electrical specification for the actual timings

Sleep Counter Reset (SCR) uses the same prescaler (see chapter 5.3) as the System Clock in Active and StandBy mode. Prescaler reset is made automatically just before going into Sleep mode if SCR is not disabled. This causes the Sleep Reset Counter to have its specified period.

4.5 Wake-Up on Change

By writing the **WUchEn[0/5]** and/or **WUchEn[3/4]** bit in **RegPaCntl2** registers the PA[0] or PA[5] and/or PA[3] or PA[4] can generate a reset from sleep on any change on a selected pin. The post selection is defined with bits **IRQPA[0l/5h]** and **IRQPA[3l/4h]**. See chapter 6 and Figure 10 for more details.

4.6 The CPU State after Reset

Reset initializes the CPU as shown in Table 4.6.1 below.

Table 4.6.1 Initial CPU value after Reset.

Name	Bits	Symbol	Initial Value
Program counter 0	12	PC0	$000 (as a result of Jump 0)
Program counter 1	12	PC1	Undefined
Program counter 2	12	PC2	Undefined
Stack pointer	2	SP	SP[0] selected
Index register	7	IX	Undefined
Carry flag	1	CY	Undefined
Zero flag	1	Z	Undefined
Halt	1	HALT	0
Instruction register	16	IR	Jump 0
Periphery registers	4	Reg.....	See peripheral memory map

5. Oscillator and Prescaler

5.1 RC Oscillator or external Clock

EM6682 can use the internal RC oscillator or external clock source for its operation.

The built-in RC oscillator without external components generates the system operating clock for the CPU and peripheral blocks. The RC oscillator is supplied by the regulated voltage in medium voltage version.

The RC oscillator can generate 2 basic frequencies selectable by metal option or by registers 512kHz or 800kHz selected by **RegMFP1[3]**.

In the output of the RC oscillator, a selectable divider allows generating 512kHz, 256kHz, 128kHz, 64kHz or 32kHz. If the basic frequency is 800kHz the divider can generate 800kHz, 400kHz, 200kHz, 100kHz or 50kHz. The division factor is given by the register **RegMFP1[2:0]** (see table 5.2.1). These frequencies can be used for the CPU clock (if the external clock is not selected). Another divider generates automatically **SysClk** as close as possible to 32kHz or 50kHz depending on the basic frequency selected. This clock is used by the 15 stages prescaler that generated clock for the peripherals.

For a full software compatibility with the EM6680 and EM6681, the division factor of the RC clock can be fix by metal option. It means that it is not necessary to set the RC frequency by software. **To get a good frequency stability over the supply in low voltage it is possible, by metal option, to select a 128kHz (or 200kHz) RC oscillator. In this case the division factor is fixed to 1 meaning that the CPU runs at 128kHz (or 200kHz) and SysClk at 32kHz (or 50kHz). It is not permitted to use the EM6682 at LV over 128kHz.**

Please note that $\mathbf{V_{dd}}$min must be higher when working with higher frequencies – see figure 30.

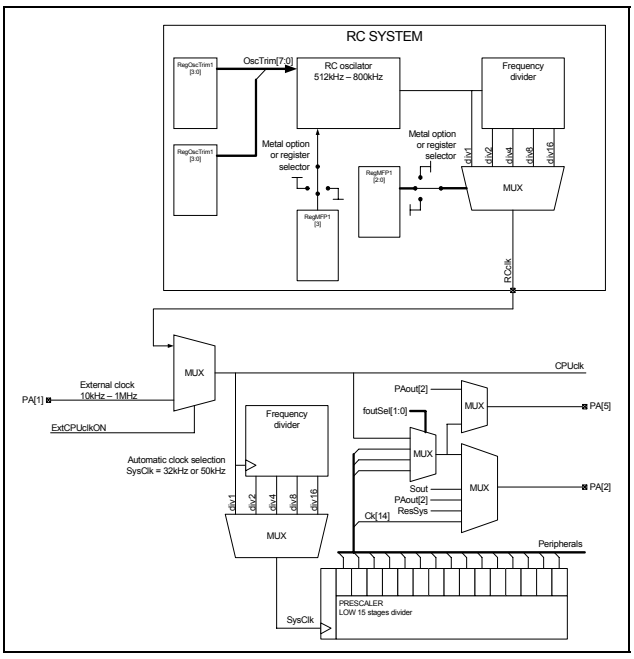
After POR the circuit always starts with the internal RC oscillator, but it can be switched to the external clock by setting the **ExtCPUclkON** bit in the register **RegPresc.** The external clock is input at PA[1] and must be in range from min. 10Khz to max. 1MHz. With this external frequency input all timing for peripherals change and the special 4 stage freq. divider **must** be adapted to best suit the applied external frequency to keep 32/*50*kHz System clock as close as possible. The system clock **must** be less than 64kHz. The external clock source must be a square wave with full amplitude from V_{ss} to V_{dd}. See Table 5.2.2 for advised special divisions depending on the external clock frequency.

Switching from internal RC oscillator to External clock or back from External clock to RC oscillator is made without generating a glitch on the internal clock. Once the circuit is running on the external Clock one can disable the RC oscillator by setting the **RCoscOff** bit in **RegSCntl2** to '1'.

In sleep mode the oscillator is stopped. It can be stopped also by setting the **RCoscOff** bit. This bit can be set only if **ExtClkOn** was set before, indicating that the CPUck was switched from the internal RC oscillator to the external clock which MUST be present. If the External Clock stops without going into Sleep mode first the EM6682 can block and only POR can reset it.

Figure 8 below shows the connection of the RC oscillator and external clock and generation of CPUclk and System clock = SysClk which is divided by the special 4 stage Freq. Divider if needed as described in 5.2 and prescaler described in 5.3.

Figure 8. Clock source for CPU or system peripherals



5.2 Special 4 stage Frequency Divider

If an internal RC clock or external frequency higher than 32 kHz or *50* kHz is selected, then the special 4 stage Frequency Divider must be used to select a frequency close to 32 kHz or *50* kHz for the SysClk - system clock used by the Prescaler. This operation is done automatically depending on RegMFP1[2:0].
Separate external clock and RC clock for explanation.

Table 5.2.1 Division factor to generate SysClk

Ext. clock	RC frequency		RC frequency or External freq. MUST be divided by	RegMFP1[2:0]	Typical SysClk Min. typ.Max. [kHz]
	(1)base RegMFP1[3] = '0'	(2) base RegNMFP1[3] = '1'			
10 kHz – 50 kHz	**32**	***50***	No Division to SysClk	000	10 – 32 – 50
55 kHz – 100 kHz	**64**	***100***	Divided by **2**	001	27.5 – 32 – 50
110 kHz – 200 kHz	**128**	***200***	Divided by **4**	010	27.5 – 32 – 50
220 kHz – 400 kHz	**256**	***400***	Divided by **8**	011	27.5 – 32 – 50
400 kHz – 1 MHz	**512**	***800***	Divided by **16**	100	10 – 32 – 62.5

Table 5.2.1 CPU and System clock frequency selection. **RegMFP1[3:0]**

RegMFP1[3] Opt[7]	RegMFP1[2] Opt[6]	RegMFP1[1] Opt[5]	RegMFP1[0] Opt[4]	CPU clock frequency	System clock frequency	Unit
0	0	0	0	32	32	kHz
0	0	0	1	64	32	kHz
0	0	1	0	128	32	kHz
0	0	1	1	256	32	kHz
0	1	0	0	512	32	kHz
1	0	0	0	50	50	kHz
1	0	0	1	100	50	kHz
1	0	1	0	200	50	kHz
1	0	1	1	400	50	kHz
1	1	0	0	800	50	kHz

The RC oscillator can be trimmed in production on 8bits. The registers **RegOscTrim1[3:0]** and **RegOscTrim2[3:0]** are loaded with the trimming value at each reset. It is possible to change this value by software at any time.

RC trimming registers	**8bits trimming word**
RegOscTrim1[3]	RegOscTrim[7] (MSB)
RegOscTrim1[2]	RegOscTrim[7]
RegOscTrim1[1]	RegOscTrim[7]
RegOscTrim1[0]	RegOscTrim[7]
RegOscTrim2[3]	RegOscTrim[7]
RegOscTrim2[2]	RegOscTrim[7]
RegOscTrim2[1]	RegOscTrim[7]
RegOscTrim2[0]	RegOscTrim[7] (LSB)

5.3 Prescaler

The prescaler consists of a fifteen elements divider chain which delivers clock signals for the peripheral circuits such as timer/counter, debouncer and edge detectors, as well as generating prescaler interrupts. The input to the prescaler is the system clock signal closest to 32 kHz or *50* kHz which comes from the RC oscillator or external clock as divided by the preceding divider. Power on initializes the prescaler to Hex(0001).

Table 5.3.1 Prescaler Clock Name Definition

Function	Name	32 KHz SysClk	*50* KHz SysClk
System clock	Ck[16]	32768 Hz	*50000* Hz
System clock / 2	Ck[15]	16384 Hz	*25000* Hz
System clock / 4	Ck[14]	8192 Hz	*12500* Hz
System clock / 8	Ck[13]	4096 Hz	*6250* Hz
System clock/ 16	Ck[12]	2048 Hz	*3125* Hz
System clock / 32	Ck[11]	1024 Hz	*1562* Hz
System clock / 64	Ck[10]	512 Hz	*781* Hz
System clock / 128	ck [9]	256 Hz	*390* Hz

Function	Name	32 KHz SysClk	*50* KHz SysClk
System clock / 256	Ck[8]	128 Hz	*195* Hz
System clock / 512	Ck[7]	64 Hz	*97* Hz
System clock / 1024	Ck[6]	32 Hz	*49* Hz
System clock / 2048	Ck[5]	16 Hz	*24* Hz
System clock / 4096	Ck[4]	8 Hz	*12* Hz
System clock / 8192	Ck[3]	4 Hz	*6* Hz
System clock / 16384	Ck[2]	2 Hz	*3* Hz
System clock / 32768	Ck[1]	1 Hz	*1.5* Hz

Figure 9. Prescaler Frequency Timing

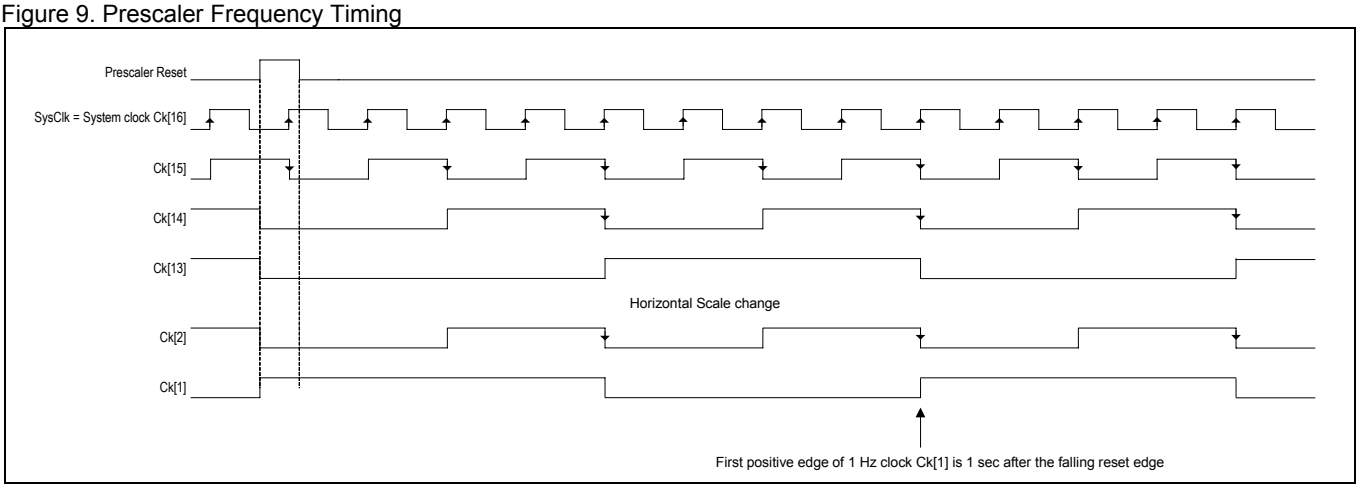


Table 5.3.2 Control of Prescaler Register **RegPresc**

Bit	Name	Reset	R/W	Description
3	ExtCPUclkON	*p*	R/W	Ext. Clock selection instead of RCosc.
2	ResPresc	0	R/W	Write Reset prescaler **1** → Reset the divider chain from Ck[14] to Ck[2], sets Ck[1]. **0** → No action. The Read value is always '0'
1	PrIntSel	0	R/W	Interrupt select. **0** → Interrupt from Ck[4] (typ. 8/*12* Hz) **1** → Interrupt from Ck[7] (typ. 64/*97* Hz)
0	DebSel	0	R/W	Debounce clock select. **0** → Debouncer with Ck[8] **1** → Debouncer with Ck[11] or Ck[14]

With DebSel = 1 one may choose either the Ck[11] or Ck[14] debouncer frequency by selecting the corresponding metal mask option or by register **RegMFP0 Opt[3]** when this register is at '1', the debouncer use Ck[14]. Relative to 32kHz the corresponding max. debouncer times are then 2 ms or 0.25 ms. For the metal mask selection refer to chapter 14.1.3

Switching the **PrIntSel** may generate an interrupt request. Avoid it with **MaskIRQ64/8** = 0 selection during the switching operation.

The prescaler contains 2 interrupt sources:
- IRQ64/8 ; this is Ck[7] or Ck[4] positive edge interrupt, the selection is depending on bit **PrIntSel.**
- IRQHz1 ; this is Ck[1] positive edge interrupt

There is no interrupt generation on reset.

The first IRQHz1 Interrupt occurs typ. 1 sec (if SysClk = 32kHz) after reset. (*0.65 sec if SysClk is 50kHz*).

NOTE: If not written explicitly all timing in peripherals is calculated for 32 kHz System Clock !

6. Input and Output port A

The EM6682 has:
- one 4-bit input/output port (port A[3:0])
- one 1 bit input port. (port PA[4])
- one optional 1 bit input/output (port PA[5]) available only in die form or SO14

Pull-up and Pull-down resistors can be added to all these ports with metal and/or register options.

6.1 Input / Output Port Overview

Table 6.1.1 Input and Output port overview

	PA[0]	PA[1]	PA[2]	PA[3]	PA[4]	*PA[5]**
Pin in 8pin package	1	2	3	4	6	NC*
General I/O	**I/O**	**I/O**	**I/O**	**I/O**	**I**	**I/O**
Serial interface	Sin **I**	Sclk **I/O**	Sout **O**	Rdy/CS **O**	--	--
WakeUp on change	yes* **I**	--	--	yes* **I**	yes* **I**	yes* **I**
Softw. pullUp/Down	yes	yes	yes	yes	yes	yes
Metal option & Softw. pullUp/Down	--	--	--	--	yes	--
Timer input	--	yes **I**	--	yes* **I**	yes* **I**	--
Irq debounce & edge select.	yes* **I**	--	--	yes* **I**	yes* **I**	yes* **I**
CPU soft. variable input	yes* **I**	--	--	yes* **I**	yes* **I**	yes* **I**
Analogue compare Input	--	--	--	--	yes **I**	--
External reset input	--	--	--	yes* **I**	yes* **I**	--
External CPU clock input	--	yes **I**	--	--	--	--
PWM timer out	yes **O**	yes **O**	--	--	--	--
freq. Output (RC, 2kHz, 1Hz)	--	--	yes* **O**	--	--	yes* **O**
CPU reset condition	--	--	yes **O**	--	--	--

NC* – Pad PA[5] is Not Connected in 8-pin package, available only in die form or SO14

Yes* ; The function is software selectable on one of PA[0], PA[5] or PA[3], PA[4], depending on the IrqPA[0l/5h] and IrqPA[3l/4h] settings.

As shown in Figure 10, Logic for the Wake up on change reset which is possible only from Sleep mode, Debounce and IRQ function on Rising or falling edge are implemented only twice but can be attached and configured by registers to 4 different pads when used as inputs.

Ports PA[0] and PA[5] can be configured to have wake up on Change, and debounced or non-debounced IRQ on the falling or rising edge. The same function is available on ports PA[3] or PA[4] which in addition can be dedicated to input reset . Registers **RegPACntl1** and **RegPACntl2** make this selection.

Table 6.1.2 Register **RegPACntl1**

Bit	Name	POR	R/W	Description
3	DebounceNoPA[3/4]	0	R/W	Debounce on when Low for PA[3/4] input
2	DebounceNoPA[0/5]	0	R/W	Debounce on when Low for PA[0/5] input
1	EdgeFallingPA[3/4]	0	R/W	IRQ edge selector for interrupt from PA[3/4] input
0	EdgeFallingPA[0/5]	0	R/W	IRQ edge selector for interrupt from PA[0/5] input

* Default is debouncer On and Rising edge for IRQ

Table 6.1.3 Register **RegPACntl2**

Bit	Name	POR	R/W	Description
3	WUchEnPA[3/4]	0	R/W	Wake/Up on change EN on PA[3] or PA[4]
2	WUchEnPA[0/5]	0	R/W	Wake/Up on change EN on PA[0] or PA[5]
1	IrqPA[3l/4h]	0	R/W	PA[3] if Low / PA[4] if High for IRQ source
0	IrqPA[0l/5h]	0	R/W	PA[0] if Low / PA[5] if High for IRQ source

* Default: No wake Up on change and IRQ source, or reset and timer input, would be PA[3], PA[0]

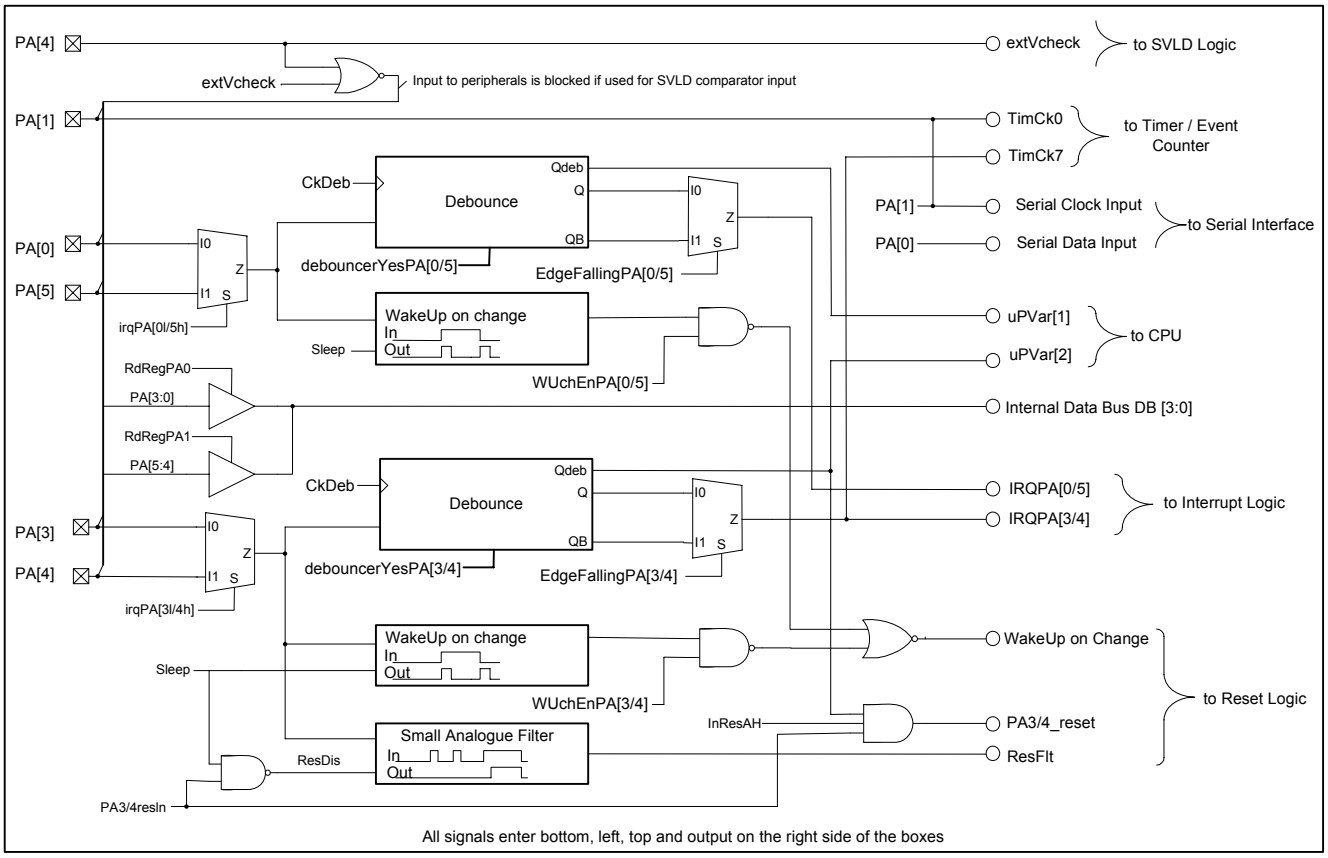
6.2 PortA as Input and its Multiplexing

The EM6682 can have up to 5 (6* in Die form) 1-bit general purpose CMOS input ports. The port A input can be read at any time, pull-up or pull-down resistors can be chosen by software and metal options for PA[3:0] and PA[5] if available.

PA[4] has pull-up or pull-down resistor selectable by metal option or **RegMFP0[0]** (pull-down if 0, pull-up if 1).

Figure 10 explains how the inputs are treated with control signals and how they are distributed to different peripherals and the CPU. This is also listed in Table 6.1.1 Input and Output ports overview.

Figure 10. EM6682 Multiplexed Inputs diagram

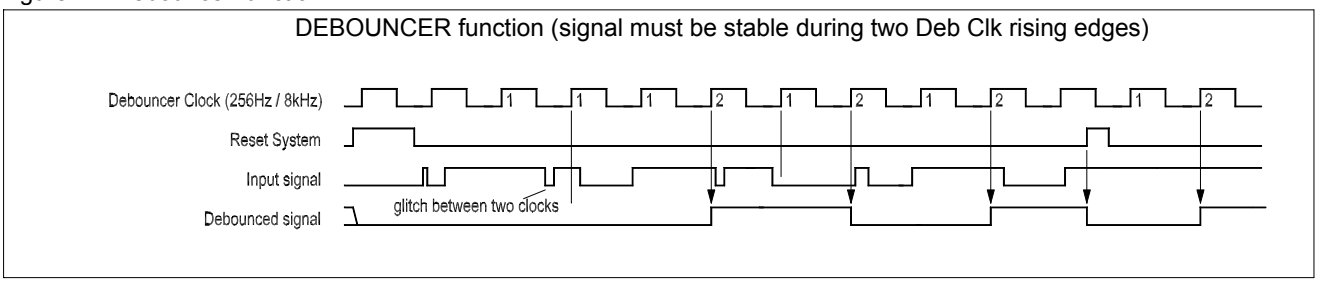


Some Input functions are explained below.

6.2.1 Debouncer

The debouncer is clocked with one of the possible debounce clocks (Ck[14] / Ck[11] / Ck[8] and can be used only in Active or StandBy mode (as only in these two modes clocks are running). The input signal has to be stable on two successive debouncer rising clock edges and must not change between them.

Figure 11. Debouncer function



6.2.2 IRQ on Port A

For interrupt request generation (IRQ) one can choose direct or debounced input and rising or falling edge IRQ triggering. With the debouncer selected **debounceYesPA[x/y]**, the input must be stable for two rising edges of the selected debouncer clock CkDeb. This means a worst case of 16ms(default) or 2ms (0.25ms by metal mask) with a system clock of 32kHz.

Either a rising or falling edge on the port A inputs - with or without debouncing - can generate an interrupt request. This selection is done by **edgeFallingPA[x/y].**
PortA can generate max 2 different interrupt requests. Each has its own interrupt mask bit in the **RegIRQMask1** register. When an IRQ occurs, inspection of the **RegIRQ1** and **RegIRQ2** registers allow the interrupt to be identified and treated.
At power on or after any reset the **RegIRQMask1** is set to 0, thus disabling any input interrupt. A new interrupt is only stored with the next active edge after the corresponding interrupt mask is cleared. See also the interrupt chapter 9.
It is recommended to mask the port A IRQ's while one changes the selected IRQ edge. Otherwise one may generate an unwanted IRQ (Software IRQ). I.e. if a bit PA[0/5] is '0' then changing from positive to negative edge selection on PA[0/5] will immediately trigger an **IRQPA[0/5]** if the IRQ was not masked.

6.2.3 Pull-up/down

On Each terminal of PA[3:0] and PA[5] an internal pull-up (metal mask MAPU[n]) and pull-down (metal mask MAPD[n]) resistor can be connected per metal mask option. By default the two resistors are in place. In this case one can choose by software to have either a pull-up, a pull-down or no resistor. See below for better understanding.
With the mask option in place, the default pull value is Pull-Down (initialized by POR). Once the software up and running this may be changed to pull-up if needed.

If the port is used also as output please check Chapter 6.3.1 CMOS / Nch. Open Drain Output.
PA[4] can have only strong Pull-up or Pull-down resistor which can be removed by software in **RegSleepCR** register bit **NoPull[4].**

Pull up or down direction is given by the metal mask selection **OPT[0]** in the register **RegMFP0**.

For Metal mask selection and available resistor values refer to chapter 15.

Pull-down ON: MAPD[n] must be in place , with n=0, 1, 2, 3, 5
AND bit **NoPdPA[n]** must be '0' .

Pull-down OFF: MAPD[n] is not in place,
OR if MAPD[n] is in place **NoPdPA[n]** = '1' cuts off the pull-down.
OR selecting **NchOpDrPA[n]** = '1' cuts off the pull-down.

Pull-up ON * : MAPU[n] must be in place,
AND bit **NchOpDrPA[n]** must be '1' ,
AND (bit **OEnPA[n]** = '0' (input mode) **OR** if **OEnPA[n]** = '1' while **PAData[n]** = 1.)

Pull-up OFF* : MAPU[n] is not in place,
OR if MAPU[n] is in place **NchOpDrPA[n]** = '0' cuts off the pull-up,
OR if MAPU[n] is in place and if **NchOpDrPA[n]** = '1' then **PAData[n]** = 0 cuts off the pull-up.

Never pull-up and pull-down can be active at the same time.

Any port A input must never be left open (high impedance state, not connected, etc.) unless the internal pull resistor is in place (mask option) and switched on (register selection). Any open input may draw a significant cross current which adds to the total chip consumption.

Note: *The mask settings_MAPU[n]) and MAPD[n] do not define the default pull direction, but the pull possibilities. It is the software which defines the pull direction (pull-up or pull-down). The only exception is on PA[4] where the direction can be forced by metal option or by register RegMFP0[0]. If metal option solution is chosen, the selected pull direction will always be valid unless the software disconnects the pull resistor.*

6.2.4 Software test variables

As shown in Figure 10 PA[0/5] or PA[3/4] are also used as input conditions for conditional software branches. These CPU inputs are always debounced and non-inverted.

- debounced PA[0/5] is connected to CPU TestVar1
- debounced PA[3/4] is connected to CPU TestVar2

CPU TestVar3 is connected to V_{SS} and can not be used in Software.

6.2.5 Port A for 10-Bit Counter

The PA[1] and PA[3/4] inputs can be used as the clock input terminal for the 10 bit counter in "event count" mode.

- PA[1] is direct input only for timer clock source #0 (no debouncer is possible).
- PA[3/4] is as for the IRQ generation debounced or input directly and non-inverted or inverted. This is defined with the register **RegPaCntl1**. Debouncing the input is always recommended.

6.2.6 Port A Wake-Up on change

In sleep mode if configured port PA[0/5] or PA[3/4] inputs are continuously monitored to wake up on change, which will immediately wake up the EM6682.

6.2.7 Port A for Serial Interface

When the serial interface is used in slave mode, PA[0] is used for serial data input and PA[1] for the serial clock.

6.2.8 Port A for External Reset

In Active and Stand-by (Halt) mode a positive debounced pulse on PA[3/4] can be the source of a reset when **PA[3/4]ResIn** and **InResAH** are set at '1'. When **IrqPA[3l/4h]** is '0' than PA[3] is selected for Reset source and when **IrqPA[3l/4h]** is '1' than PA[4] is selected for Reset source.

6.2.9 Port PA[4] as Comparator Input

When using the PA[4] as an input to the internal SVLD comparator NO pull-up resistor should be connected on this terminal. Otherwise the device may draw excessive current.

First PA[4] pull-up/down resistor should be disconnected by software and the **ExtVcheck** bit can be set to '1'. This dedicates PA[4] as SVLD resistor divider input to the SVLD comparator.

At this point the measurements respect the same timing as any other SVLD measurements as explained in Chapter Supply Voltage Detector. It can also generate an IRQ if the input voltage is lower as Comparator level. Thus configured a direct read of PA[4] will result in reading '0'.

6.2.10 Reset and Sleep on Port A

During circuit initialization, all Control registers specifically marked to be initialized by POR are reset. PA[5] and PA[3:0] are input mode with pulldown resistors (if mask present). PA[4] is in input mode , pull-up or pulldown resistor is defined by the metal mask settings.
During Sleep mode, the circuit retains its register values. As such the PA configurations remain active also during Sleep.
Sleep mode is cancelled with any Reset. However the Reset State does not reset the registers bits which are specifically marked to be initialized by POR only. (Pull, Nch Open drain, Freq out, etc configurations).
Sleep mode is cancelled with a Reset, all system register which are not specifically initialized by POR only will be initialized at this point.

6.2.11 Port A Blocked Inputs

In sleep mode if PortA inputs are not used and prepared for Wake-Up on Change or Reset these inputs are blocked. At that time port can be undefined from external and this will not generate an over-consumption.

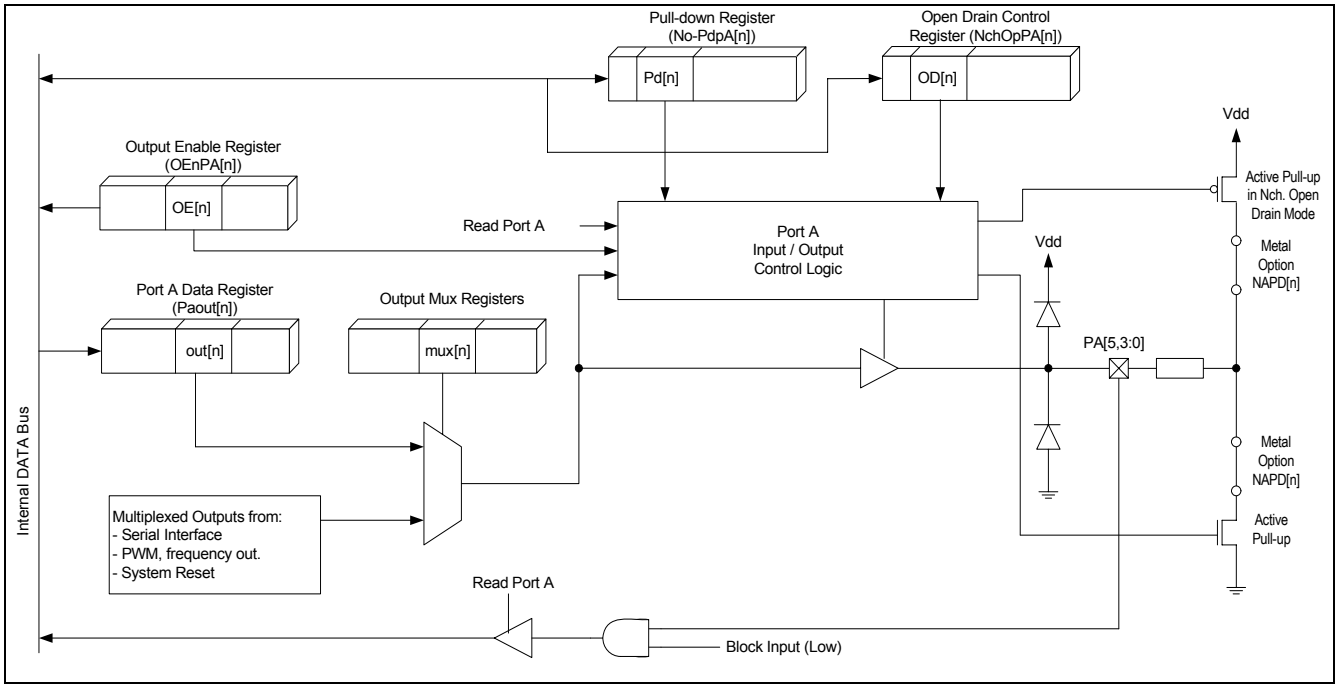
PA[0] : Blocked if Sleep bit set and no IRQ or Wake-up defined on this input
PA[1] : Blocked if Sleep bit set
PA[2] : Blocked if Sleep bit set
PA[3] : Blocked if Sleep bit set and no IRQ or Wake-up defined on this input
PA[4] : Blocked if Sleep bit set and no IRQ or Wake-up defined on this input
Also blocked if External VLD check enabled
PA[5] : Never blocked

6.3 PortA as Output and its Multiplexing

The EM6682 can have up to 4 (5 in Die form or 14-pin package) bit general purpose CMOS or N-channel Open Drain Output ports. Table 6.1.1 Input and Output ports overview shows all the possibilities. Figure 12 shows the output architecture and possible output signals together with software controlled pull-up and pull-down resistors which are disconnected when the port is an output and in a defined state, to preclude additional consumption.

The output multiplexing registers are **RegPACntl3** and **RegPACntl4**.

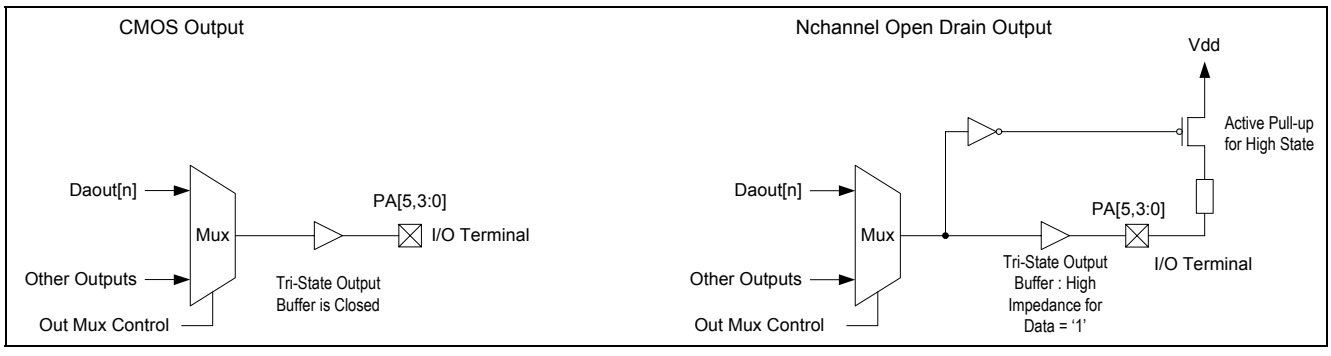
Figure 12. Port A Architecture (Outputs)



6.3.1 CMOS / Nch. Open Drain Output

The port A outputs can be configured as either CMOS or Nch. open drain outputs. In CMOS both logic '1' and '0' are driven out on the terminal. In Nch. Open Drain only the logic '0' is driven on the terminal, the logic '1' value is defined by the internal pull-up resistor (if implemented), or high impedance.

Figure 13. CMOS or Nch. Open Drain Outputs



NOTE: State of I/O pads may not be defined until V_{reg} reaches typ. 0.8V and Power-On-Reset logic supplied by V_{reg} clears them to Inputs.
This time depends on how fast capacitor on V_{reg} is charged and typ. it can be in range of couple of ms.

6.4 Port A registers

The two Control registers for Input control, **RegPACntl1** and **RegPACntl2,** were already shown in chapter 6; Input / Output Ports Overview.

Table 6.4.1 Register **RegPA0**

Bit	Name	Reset	R/W	Description
3	PAData[3]	0	R* /W	PA[3] input and PAout[3] output
2	PAData[2]	0	R* /W	PA[2] input and PAout[2] output
1	PAData[1]	0	R* /W	PA[1] input and PAout[1] output
0	PAData[0]	0	R* /W	PA[0] input and PAout[0] output

* Direct read on Port A terminals

Table 6.4.2 Register **RegPa0OE**

Bit	Name	Reset	R/W	Description
3	OEnPA[3]	0	R/W	I/O control for PA[3] , output when OEnPA[3] = Hi
2	OEnPA[2]	***0*** P**	R/W	I/O control for PA[2] , output when OEnPA[2] = Hi
1	OEnPA[1]	0	R/W	I/O control for PA[1] , output when OEnPA[1] = Hi
0	OEnPA[0]	0	R/W	I/O control for PA[0] , output when OEnPA[0] = Hi

P** On Reset PA[2] is forced to output if (PA[0]='0', PA[1]='1', PA[4]='1', Sout/RstPA[2]='1' and freqOutPA[2]='1') until System reset is finished. Refer also to table **Error! Reference source not found.**.
After Reset is finished and circuit starts to execute instructions PA[2] becomes tri-state input with pull-down.
Bit OEnPA[2] is reset to '0' with every Reset.

Table 6.4.3 Register **Pa0noPDown**

Bit	Name	POR*	R/W	Description
3	NoPdPA[3]	0	R/W	No pull-down on PA[3]
2	NoPdPA[2]	0	R/W	No pull-down on PA[2]
1	NoPdPA[1]	0	R/W	No pull-down on PA[1]
0	NoPdPA[0]	0	R/W	No pull-down on PA[0]

POR* Reset only with Power On Reset

Table 6.4.4 Register **Pa0NchOpenDr**

Bit	Name	POR*	R/W	Description
3	NchOpDrPA[3]	0	R/W	Nch. Open Drain on PA[3]
2	NchOpDrPA[2]	0	R/W	Nch. Open Drain on PA[2]
1	NchOpDrPA[1]	0	R/W	Nch. Open Drain on PA[1]
0	NchOpDrPA[0]	0	R/W	Nch. Open Drain on PA[0]

* Reset only with Power On Reset, Default "0" is: CMOS on PA[3..0]

Table 6.4.5 Register **RegPA1**

Bit	Name	Reset	R/W	Description
3	NchOpDrPA[5]	p**	R* /W	Nch. Open Drain on PA[5]
2	OEnPA[5]	0	R* /W	I/O control for PA[5] , output when OEnPA[5] = Hi
1	PAData[5]	0	R* /W	PA[5] input and PAout[5] output
0	PAData[4]*	0	R*	PA[4] input

* Direct read on Port A terminals p** reset to '0' by POR only

Table 6.4.6 Register **RegFreqRst**

Bit	Name	POR	R/W	Description
3	InResAH	p	R/W	Input reset On in Active and StandBy mode
2	PA3/4resIn	p	R/W	PA3/4 dedicated for Input reset when set at '1'
1	foutSel[1]	x	R/W	Output Frequency selection (foutSel[1:0])
0	foutSel[0]	x	R/W	(11) CPUClk, (10) SysClk, (01) 2kHz, (00) 1Hz

Interrupt PortA Control bits **MaskIRQPA[0/5]** and **MaskIRQPA[3/4]** used to enable (Mask) the Interrupt ReQuest IRQ from PortA are in register **RegIRQMask1**.

Interrupt status bits **IRQPA[0/5]** and **IRQPA[3/4]** used to signal the Interrupt from PortA are in register **RegIRQ1**. They are both shown in Chapter Interrupt Controller.

Note: CPUClk = RCClk if no external clock used. In case of external clock, CPUClk is equal to the PA[1] input clock.

Output multiplexing registers are shown below.

Table 6.4.7 Register **RegPACntl3**

Bit	Name	POR	R/W	Description
3	SerialStPA[3]	0	R/W	Output selection for PA[3] when output
2	SerialCkPA[1]	0	R/W	Output selection for PA[1] when output
1	PWMoutPA[1]	0	R/W	Output selection for PA[1] when output
0	PWMoutPA[0]	0	R/W	Output selection for PA[0] when output

Table 6.4.8 Register **RegPACntl4**

Bit	Name	POR	R/W	Description
3	NoPdPA[5]	0	R/W	No pull-down on PA[5]
2	freqOutPA[5]	0	R/W	Output selection for PA[5] when output
1	Sout/rstPA[2]	1	R/W	Output selection for PA[2] when output
0	freqOutPA[2]	1	R/W	Output selection for PA[2] when output

Table 6.4.9 PA[0] I/O status depending on its **RegPACntl3** and **RegPa0OE** registers

OEnPA[0]	PWMoutPA[0]		**Description of PA[0] terminal**
0	**X**		Input
1	**0**		PAout[0] general Output
1	**1**		PWM Output from the 10-Bit Counter

Table 6.4.10 PA[1] I/O status depending on its **RegPACntl3** and **RegPa0OE** registers

OEnPA[1]	**SerialCkPA[1]**	**PWMoutPA[1]**	**Description of PA[1] terminal**
0	**X**	**X**	Input
1	**0**	**0**	PAout[1] general Output
1	**0**	**1**	PWM Output from the 10-Bit Counter
1	**1**	**X**	Sclk (Serial interface clock output)

Table 6.4.11 PA[2] I/O status depending on its **RegPACntl4** and **RegPa0OE** registers

OEnPA[2]	**Sout/rstPA[2]**	**freqOutPA[2]**	**Description of PA[2] terminal**
0	X	X	Input
1	0	0	PAout[2] general Output
1	0	1	Freq. Output (CPUClk, SysClk, 2kHz, 1Hz)
1	1	0	Sout (Serial interface data output)
1	1	1	High level '1' during Reset state output 8kHz frequency output while out of reset state Low level '0' output during sleep
0 PA[0] = '1' PA[4] = '1' PA[1] = '0'	1	1	Output: high level during Reset state Input: out of reset state and during sleep

Frequency output is selected in 6.4.6 Register **RegFreqRst**

Table 6.4.12 PA[3] I/O status depending on its **RegPACntl3** and **RegPa0OE** registers

OEnPA[3]	**SerialStPA[3]**		**Description of PA[3] terminal**
0	**X**		Input
1	**0**		PAout[3] general Output
1	**1**		Rdy/CS (Serial interface status output)

Table 6.4.13 PA[5] I/O status depending on its **RegPACntl4** and **RegPA1** registers

OEnPA[5]	**freqOutPA[5]**		**Description of PA[5] terminal**
0	**X**		Input
1	**0**		PAout[5] general Output
1	**1**		Freq. Output (CPUClk, SysClk, 2kHz, 1Hz)

Frequency output is selected in 6.4.6 Register

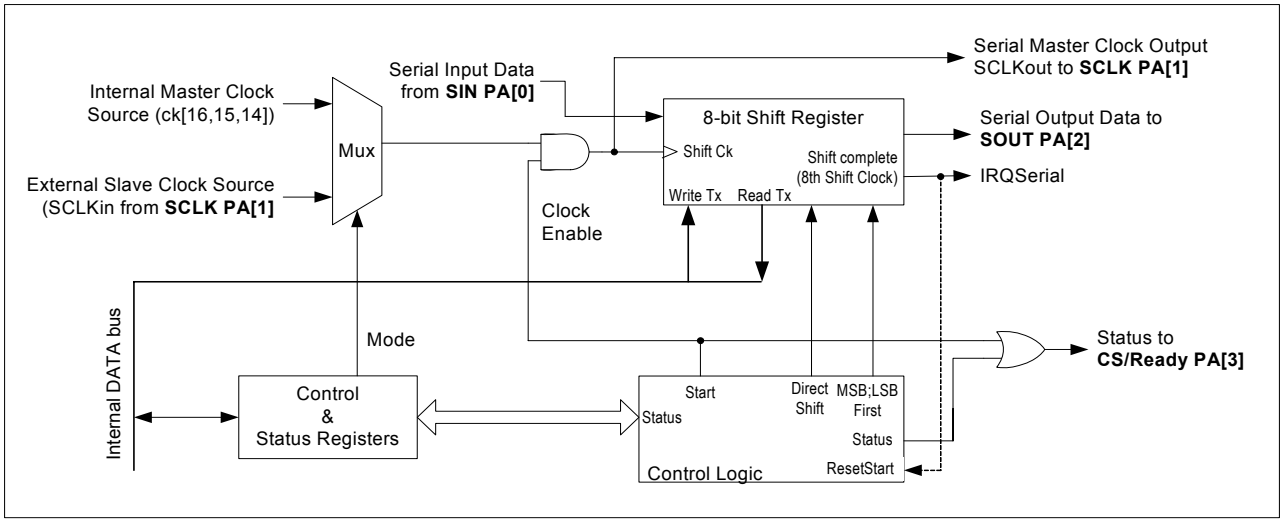
Note: CPUClk = RCClk if no external clock used. In case of external clock, CPUClk is equal to the PA[1] input clock.

7. Serial Port

The EM6682 contains a simple, half duplex three wire synchronous type serial interface., which can be used to program or read an external EEPROM, ADC, ... etc. Its I/O are multiplexed on Port A.

For data reception, a shift-register converts the serial input data on the SIN(PA[0]) terminal to a parallel format, which is subsequently read by the CPU in registers **RegSDataL** and **RegSDataH** for low and high nibble. To transmit data, the CPU loads data into the shift register, which then serializes it on the SOUT(PA[2]) terminal. It is possible for the shift register to simultaneously shift data out on the SOUT terminal and shift data on the SIN terminal. In Master mode, the shifting clock is supplied internally by the Prescaler : one of three prescaler frequencies are available, Ck[16] or external clock (metal option to select between, Ck[15] or Ck[14]. In Slave mode, the shifting clock is supplied externally on the SCLKIn(PA[1]) terminal. In either mode, it is possible to program : the shifting edge, shift MSB first or LSB first and direct shift output. All these selection are done in register **RegSCntl1** and **RegSCntl2**.

Figure 14. Serial Interface Architecture



The PA[3..0] terminal configuration is shown in Figure 10 and 12. When the Serial Interface is used then care should be taken not to use inputs and outputs needed for Serial Interface for other peripherals !:

- PA[0] {SIN} must be dedicated to Serial input if needed and can not be used for IRQ, Software Variable jumps or Output. It can be still used for Wake-Up on Change
- PA[1] {SCLK} is an output for Master mode {SCLKOut} and an input for Slave mode {SCLKIn}. But different functions can be Switched On/Off with care as they are needed.
- PA[2] {SOUT} must be dedicated to Serial Data Output if needed and can not be used for Analogue input, or other Output.
- PA[3] {CS / Ready} if used for serial Interface status output. When used for Serial Interface it can not be used for IRQ, Software Variable jumps or Output. It can be still used for Wake-Up on Change.

Note:
Before using the serial interface, the corresponding circuit terminals must be configured accordingly.

7.1 General Functional Description

After power on or after any reset the serial interface is in serial slave mode with **Start** and **Status** set to 0, LSB first, negative shift edge and all outputs are in high impedance state.
When the **Start** bit is set, the shift operation is enabled and the serial interface is ready to transmit or receive data, eight shift operations are performed: 8 serial data values are read from the data input terminal into the shift register and the previous loaded 8-bits are send out via the data output terminal. After the eight shift operation, an interrupt is generated, and the **Start** bit is reset.

Parallel to serial conversion procedure (master mode example).

Write to **RegSCntl1** serial control (clock freq. in master mode, edge and MSB/LSB select).
Write to **RegSDataL** and **RegSDataH** (shift out data values).
Write to **RegSCntl2** (Start=1, mode select, status). → Starts the shift out
After the eighth clock an interrupt is generated, **Start** becomes low. Then, interrupt handling

Serial to parallel conversion procedure (slave mode example).

Write to **RegSCntl1** (slave mode, edge and MSB/LSB select).
Write to **RegSCntl2** (Start=1, mode select, status).
After eight serial clocks an interrupt is generated, **Start** becomes low.
Interrupt handling.
Shift register **RegSDataL** and **RegSDataH** read.
A new shift operation can be authorized.

7.2 Detailed Functional Description

Master or Slave mode is selected in the control register **RegSCntl1.**
In Slave mode, the serial clock comes from an external device and is input via the PA[1] terminal as a synchronous clock (SCLKIn) to the serial interface. The serial clock is ignored as long as the **Start** bit is not set. After setting **Start,** only the eight following active edges of the serial clock input PA[1] are used to shift the serial data in and out. After eight serial clock edges the **Start** bit is reset. The PA[3] terminal is a copy of the (**Start OR Status)** bit values, it can be used to indicate to the external master, that the interface is ready to operate or it can be used as a chip select signal in case of an external slave.

In Master mode, the synchronous serial clock is generated internally from the system clock. The frequency is selected from one out of three sources (**MS0** and **MS1** bits in **RegSCntl1**) **.** The serial shifting clock is only generated during **Start** = high and is output to the SCLK terminal as the Master Clock (SCLKOut). When **Start** is low, the serial clock output on PA[1] is 0.

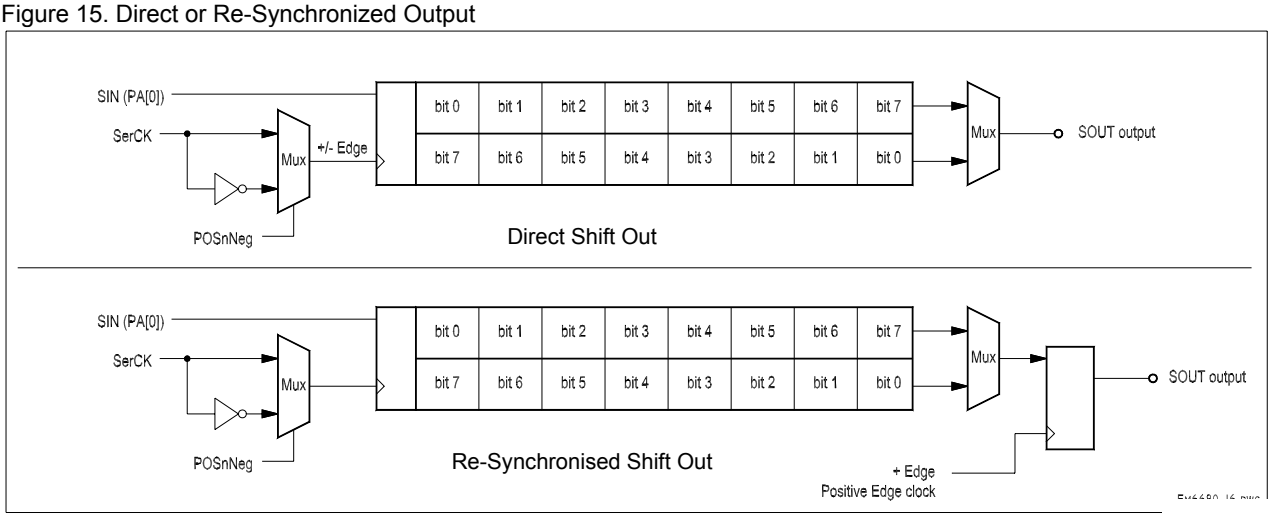
An interrupt request **IRQSerial** is generated after the eight shift operations are done. This signal is set by the last negative edge of the serial interface clock on PA[1] (master or slave mode) and is reset to 0 by the next write of **Start** or by any reset. This interrupt can be masked with register **RegIRQMask2.** For more details about the interrupt handling see chapter 11.

Serial data input on PA[0] is sampled by the positive or negative serial shifting clock edge, as selected by the Control Register **POSnNeg** bit**.** Serial data input is shifted in LSB first or MSB first, as selected by the Control Register **MSBnLSB** bit**.**

7.2.1 Output Modes

Serial data output is given out in two different ways. Refer also to Figures 15 and 16.

Figure 15. Direct or Re-Synchronized Output



- **OM[0]** = 0 :

The serial output data is generated with the selected shift register clock (**POSnNeg**). The first data bit is available directly after the **Start** bit is set.

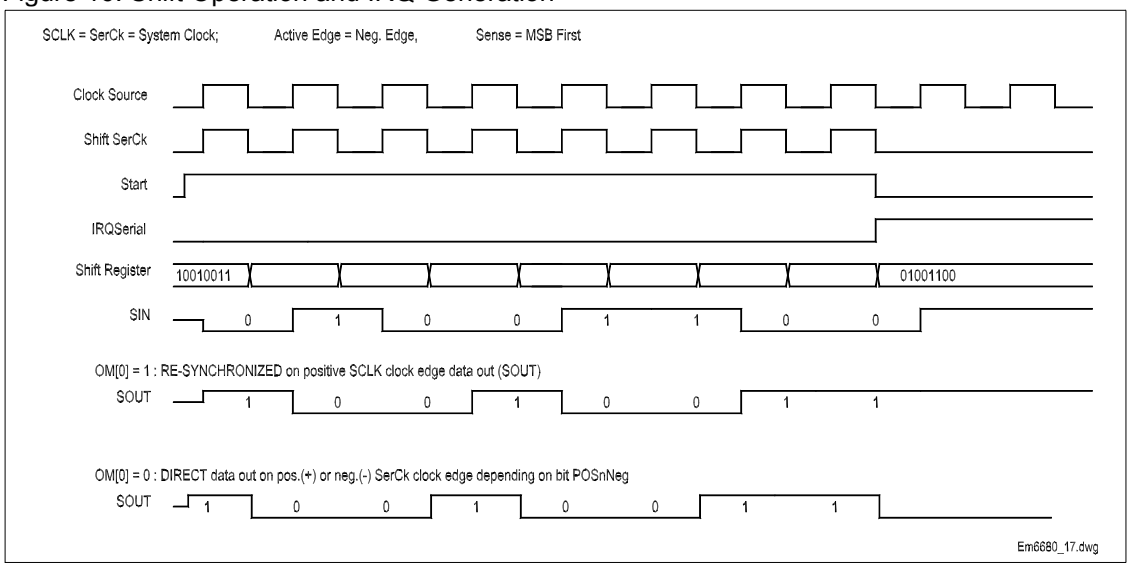
- **OM[0]** = 1 :

The serial output data is re-synchronized by the positive serial interface clock edge, independent of the selected clock shifting edge. The first data bit is available on the first positive serial interface clock edge after Start='1'.

Table 7.2.1 Output Mode Selection in **RegSCntl2**

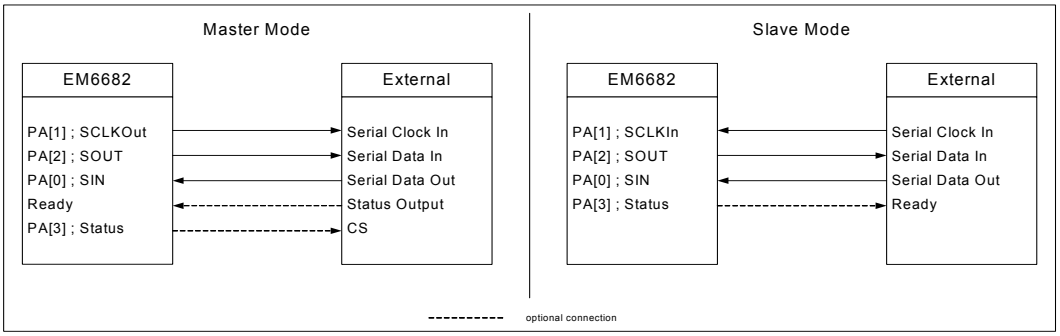
OM[0]	Output mode	Description
0	Serial-Direct	Direct shift pos. or neg. edge data out
1	Serial-Synchronized	Re-synchronized positive edge data shift out

Figure 16. Shift Operation and IRQ Generation



Note : A write operation in the control registers or in the data registers while **Start** is high will change internal values and may cause an error condition. The user must take care of the serial interface status before writing internal registers. In order to read the correct values on the data registers, the shift operation must be halted during the read accesses.

Figure 17. Example of Basic Serial Port Connections



7.3 Serial Interface Registers

Table 7.3.1 Register **RegSCntl1**

Bit	Name	Reset	R/W	Description
3	MS1	0	R/W	Frequency selection
2	MS0	0	R/W	Frequency selection
1	POSnNeg	0	R/W	Positive or negative clock edge selection for shift operation
0	MSBnLSB	0	R/W	Shift MSB or LSB value first (0=LSB first)

Default "0" is: Slave mode external clock, negative edge, LSB first

Table 7.3.2 Frequency and Master Slave Mode Selection

MS1	MS0	Description
0	**0**	Slave mode: Clock from external
0	**1**	Master mode: ck[14], System clock / 4
1	**0**	Master mode: ck[15], System clock / 2
1	**1**	Master mode: ck[16], System clock

Table 7.3.3 Register **RegSCntl2**

Bit	Name	Reset	R/W	Description
3	Start	0	R/W	Enabling the interface,
2	Status	0	R/W	Ready or Chip Select output on PA[3]
1	RCoscOff	0	R/W	RC oscillator off when set to ‘1’ and if ExtCPUclkON is ‘1’
0	OM[0]	0	R/W	Direct shift output when ‘0’ ; Output re-synchronised when ‘1’

Default "0" is: Interface disabled, status 0, direct shift output.

Table 7.3.4 Register **RegSDataL**

Bit	Name	Reset	R/W	Description
3	SerDataL[3]	0	R/W	Serial data low nibble
2	SerDataL[2]	0	R/W	Serial data low nibble
1	SerDataL[1]	0	R/W	Serial data low nibble
0	SerDataL[0]	0	R/W	Serial data low nibble

Default "0" is: Data equal 0.

Table 7.3.5 Register **RegSDataH**

Bit	Name	Reset	R/W	Description
3	SerDataH[3]	0	R/W	Serial data high nibble
2	SerDataH[2]	0	R/W	Serial data high nibble
1	SerDataH[1]	0	R/W	Serial data high nibble
0	SerDataH[0]	0	R/W	Serial data high nibble

Default "0" is: Data equal 0.

8. 10-bit Counter

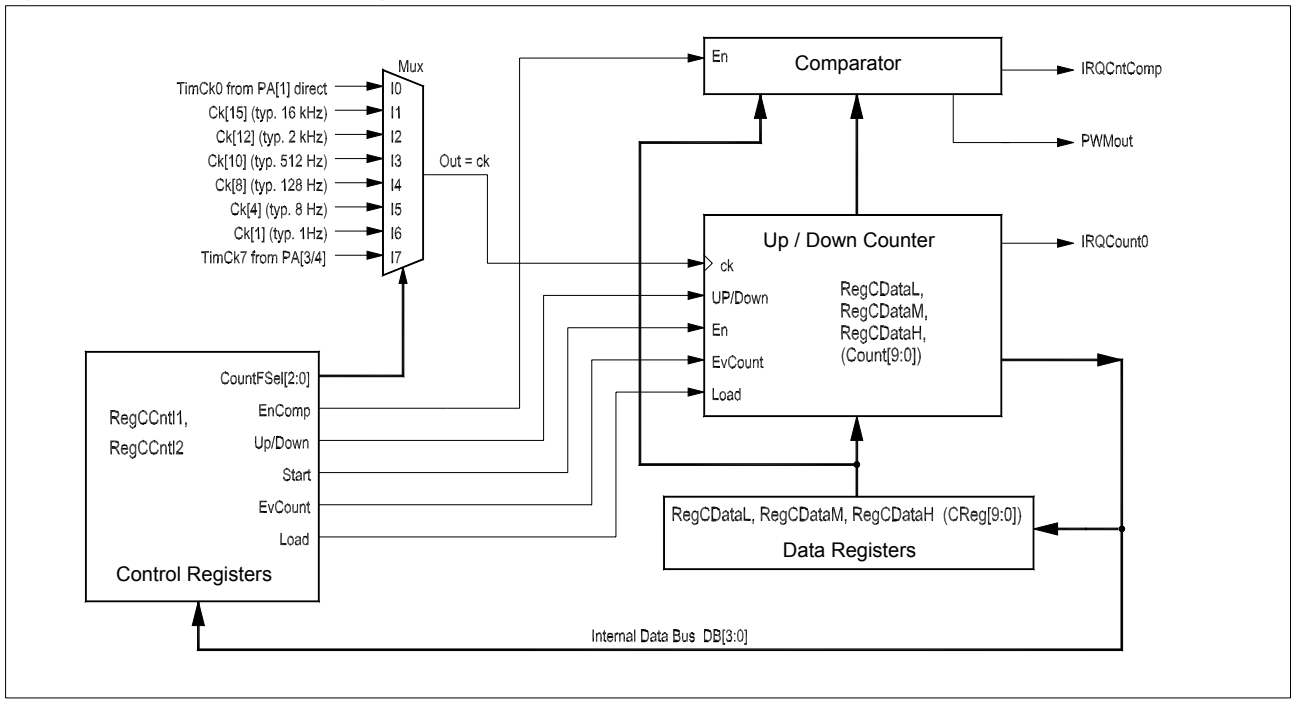
The EM6682 has a built-in universal cyclic counter. It can be configured as 10, 8, 6 or 4-bit counter. If 10-bits are selected we call that full bit counting, if 8, 6 or 4-bits are selected we call that limited bit counting.
The counter works in up- or down count mode. Eight clocks can be used as the input clock source, six of them are prescaler frequencies and two are coming from the input pads PA[1] (direct only) and PA[3/4] (direct or debounced). In this case the counter can be used as an event counter.

The counter generates an interrupt request **IRQCount0** every time it reaches 0 in down count mode or 3FF in up count mode. Another interrupt request **IRQCntComp** is generated in compare mode whenever the counter value matches the compare data register value. Each of this interrupt requests can be masked (default). See section 9 for more information about the interrupt handling.

A 10-bit data register **CReg[9:0]** is used to initialize the counter at a specific value (load into **Count[9:0]**). This data register (**CReg[9:0]**) is also used to compare its value against **Count[9:0]** for equivalence.

A Pulse-Width-Modulation signal (PWM) can be generated and output on port B terminal PA[0] or PA[1].A special metal option **opt_LV_Bit0DontCare** is implemented which makes the bit0 of the counter a don't care bit. With this metal option in place the 10 bit counter becomes a 9 bit counter bit1 to bit9 and all PWM functions will be on either 9, 7, 5 or 3 bits. The counter bit0 remains R/W but is not used for counting nor Compare functions. Refer also to 14.1.9.

Figure 18. 10-bit Counter Block Diagram



8.1 Full and Limited Bit Counting

In Full Bit Counting mode the counter uses its maximum of 10-bits length (default). With the **BitSel[1,0]** bits in register **RegCDataH** one can lower the counter length, for IRQ generation, to 8, 6 or 4 bits. This means that actually the counter always uses all the 10-bits, but IRQCount0 generation is only performed on the number of selected bits. The unused counter bits may or may not be taken into account for the **IRQComp** generation depending on bit **SelIntFull**. Refer to chapter 8.4.

Table 8.1.1. Counter length selection

BitSel[1]	BitSel[0]	counter length
0	0	10-Bit
0	1	8-Bit
1	0	6-Bit
1	1	4-Bit

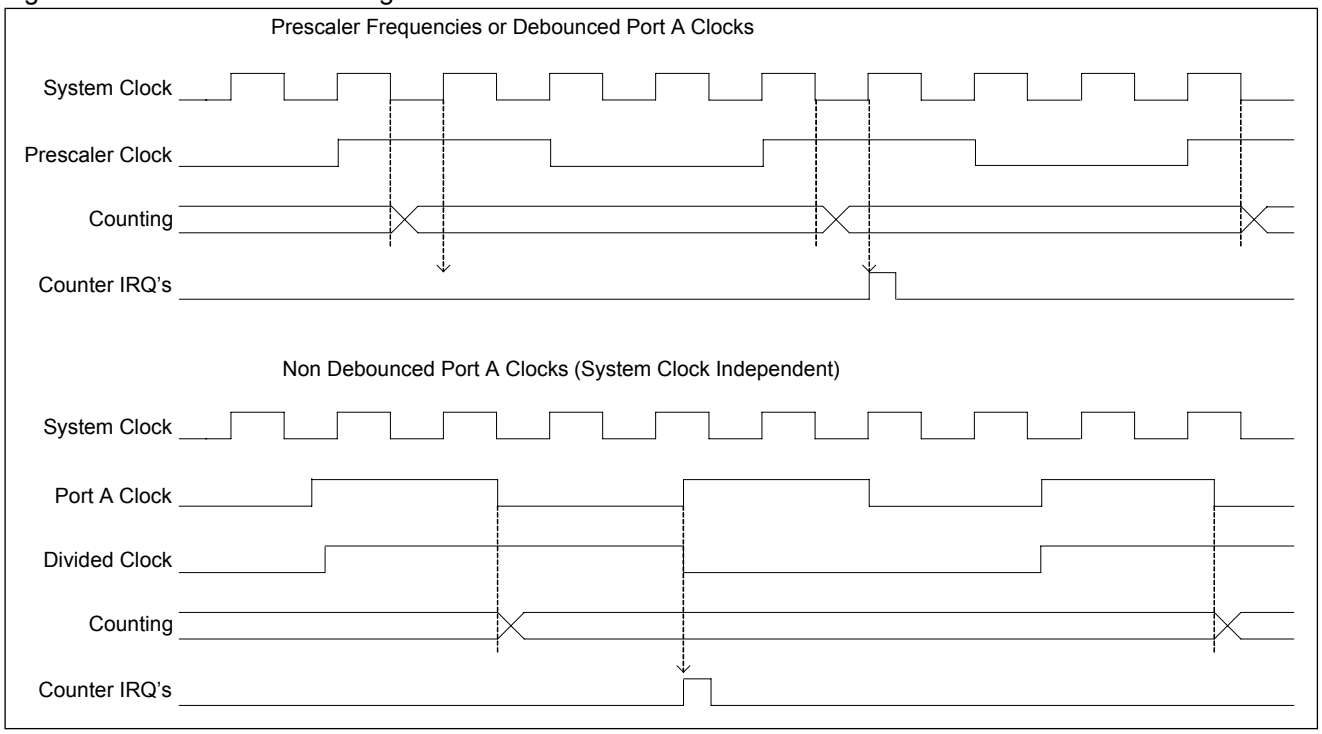
8.2 Frequency Select and Up/Down Counting

Eight (8) different input clocks can be selected to drive the Counter. The selection is done with bits **CountFSel2…0** in register **RegCCntl1**. Six (6) of this input clocks are coming from the prescaler. The maximum prescaler clock frequency for the counter is half the system clock SysClk and the lowest is 1Hz typ. Therefore a complete counter roll over can take as much as 17.07 minutes (1Hz clock, 10 bit length) or as little as 977 µs (Ck[15] typ 16.3kHz, 4 bit length). The **IRQCount0**, generated at each roll over, can be used for time bases, measurements length definitions, input polling, wake up from Halt mode, etc. The **IRQCount0** and **IRQComp** are generated with the system clock Ck[16] rising edge. IRQCount0 condition in up count mode is : reaching 3FF if 10-bit counter length (or FF, 3F, F in 8, 6, 4-bit counter length). In down count mode the condition is reaching '0'. The non-selected bits are 'don't care'. For IRQComp refer to section 8.4.

The metal option **CntF** or the register RegMFP0 Opt[1] allows selecting the CPU clock divided by 2 which replace the external clock coming from Port A at selection 7 if Opt[1] = '1'.

Note: The Prescaler and the Microprocessor clock's are usually non-synchronous, therefore time bases generated are max. n, min. n-1 clock cycles long (n being the selected counter start value in count down mode). However the prescaler clock can be synchronized with µP commands using for instance the prescaler reset function.

Figure 19. Counter Clock Timing



The two remaining clock sources are coming from the PA[1] or PA[3/4] terminals. Refer to Figure 10 on page 15 for details. Input PA[1] can be only direct non-debounce input, second PA[3/4] can be either debounce (Ck[11] or Ck[8]) or direct input, the input polarity can also be chosen. The outputs for Timer clock inputs are named TimCk0 and TimCk7 respectively. For the debouncer and input polarity selection refer to chapter 6.

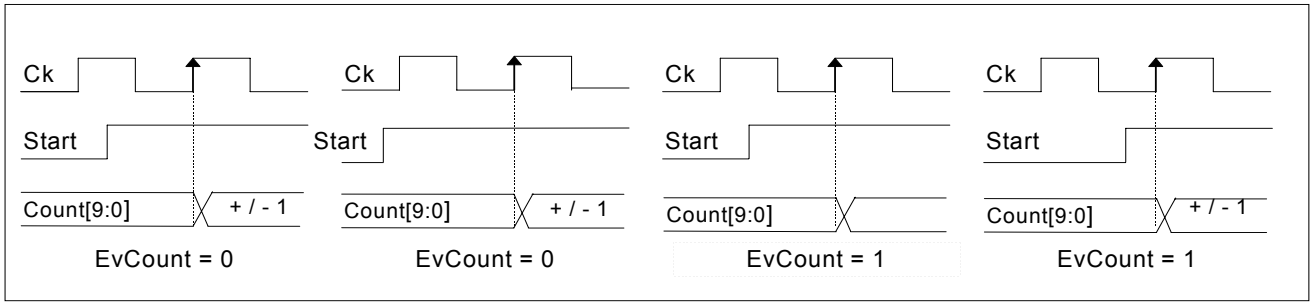
In the case of port A input clock without debouncer, the counting clock frequency will be half the input clock on port A. The counter advances on every odd numbered port A negative edge (divided clock is high level). **IRQCount0** and **IRQComp** will be generated on the rising PA[3/4] or PA[1] input clock edge. In this condition the EM6682 is able to count with a higher clock rate as the internal system clock (Hi-Frequency Input). Maximum port A input frequency is limited to 500kHz (@$V_{dd} \geq 1.5$ V). If higher frequencies are needed, please contact EM Microelectronic's.

In both, up or down count (default) mode, the counter is cyclic. The counting direction is chosen in register **RegCCntl1** bit **Up/Down** (default '0' is down count). The counter increases or decreases its value with each positive clock edge of the selected input clock source. Start up synchronization is necessary because one can not always know the clock status when enabling the counter. With EvCount=0, the counter will only start on the next positive clock edge after a previously latched negative edge, while the **Start** bit was already set to '1'. This synchronization is done differently if event count mode (bit **EvCount**) is chosen. Refer also to Figure 20. Internal Clock Synchronization.

8.3 Event Counting

The counter can be used in a special event count mode where a certain number of events (clocks) on the PA[1] (only non-debounced and only rising edge) or PA[3/4] input are counted. In this mode the counting will start directly on the next active clock edge on the selected port A input.

Figure 20. Internal Clock Synchronization



The Event Count mode is switched on by setting bit **EvCount** in the register **RegCCntl2** to '1'. PA[3] or PA[4] input depending on **IrqPA[3l/4h]** bit in **RegPaCntl1** can be inverted depending on **edgeFallingPA[3/4]** in register **RegPaCntl1** and should be debounced. The debouncer is switched on with **debounceNoPA[3/4]** at '0' in the same register. Its frequency depends on the bit **DebSel** from register **RegPresc** setting. Refer also to Figure 10 for PortA Inputs Function. As already said for other PA[1] input only possibility is to count rising non-debounced edges.

A previously loaded register value (**CReg[9:0]**) can be compared against the actual counter value (**Count[9:0]**). If the two are matching (equality) then an interrupt (**IRQComp**) is generated. The compare function is switched on with the bit **EnComp** in the register **RegCCntl2**. With **EnComp** = 0 no **IRQComp** is generated. Starting the counter with the same value as the compare register is possible, no IRQ is generated on start. Full or Limited bit compare are possible, defined by bit **SelIntFull** in register **RegSysCntl1**.
EnComp must be written after a load operation (**Load** = 1). Every load operation resets the bit EnComp.

1. **Full bit compare function.**

Bit **SelIntFull** is set to '1'. The function behaves as described above independent of the selected counter length. Limited bit counting together with full bit compare can be used to generate a certain amount of IRQCount0 interrupts until the counter generates the **IRQComp** interrupt. With ***PWMOn***='1' the counter would have automatically stopped after the **IRQComp**, with ***PWMOn***='0' it will continue until the software stops it. **EnComp** must be cleared before setting **SelIntFull** and before starting the counter again. Be careful, **PWMoutPA[0]** also redefines the port PA[0] or **PWMoutPA[1]** the PA[1] output data. (refer to section 0).
The signal PWMOn is acombination of **PWMOutPA[0], PWMOutPA[1], SerialCkPA[1]**

PWMOn = (PWMOutPA[0] **OR** PWMOutPA[1]) **AND NOT**(SeriaCktPA[1]))

2. **Limited bit compare**

With the bit **SelIntFull** set to '0' (default) the compare function will only take as many bits into account as defined by the counter length selection **BitSel[1:0]** (see chapter 6.3).

8.4 Pulse Width Modulation (PWM)

The PWM generator uses the behavior of the Compare function (see above) so **EnComp** must be set to activate the PWM function.. At each Roll Over or Compare Match the PWM state - which is output on port PA[0] or PA[1] - will toggle. The start value on PA[0] or PA[1] is forced while **EnComp** is 0 the value is depending on the up or down count mode. Every counter value load operation resets the bit **EnComp** and therefore the PWM start value is reinstalled.

One can output PWM signal to PA[0] or PA[1]. Setting **PWMoutPA[0]** to '1' in register **RegPaCntl3** routes the counter PWM output to PA[0]. Insure that PA[0] is set to output mode. Setting **PWMoutPA[1]** to '1' in register **RegPaCntl3** routes the counter PWM output to PA[1]. Insure that PA[1] is set to output mode. Refer to section 6.3 and 6.4 for the port A output setup.

The PWM signal generation is independent of the limited or full bit compare selection bit **SelIntFull.** However if **SelIntFull** = 1 (FULL) and the counter compare function is limited to lower than 10 bits one can generate a predefined number of output pulses. In this case, the number of output pulses is defined by the value of the unused counter bits. It will count from the start value until the IRQComp match.

One must not use a compare value of hex 0 in up count mode nor a value of hex 3FF (or FF,3F, F if limited bit compare) in down count mode.

For instance, loading the counter in up count mode with hex 000 and the comparator with hex C52 which will be identified as :

- bits[11:10] are limiting the counter to limits to 4 bits length, =03 (BitSel[1,0])
- bits [9:4] are the unused counter bits = hex 05 (bin 000101), (number of PWM pulses)
- bits [3:0] (comparator value = 2). (length of PWM pulse)

Thus after 5 PWM-pulses of 2 clocks cycles length the Counter generates an **IRQComp** and stops.
The same example with SelIntFull=0 (limited bit compare) will produce an unlimited number of PWM at a length of 2 clock cycles.

8.4.1 How the PWM Generator works.

For Up Count Mode; Setting the counter in up count and PWM mode the PA[0] or PA[1] PWM output is defined to be 0 (**EnComp**=0 forces the PWM output to 0 in upcount mode, 1 in downcount). Each Roll Over will set the output to '1' and each Compare Match will set it back to '0'. The Compare Match for PWM always only works on the defined counter length. This, independent of the **SelIntFull** setting which is valid only for the IRQ generation. Refer also to the compare setup in chapter 0.

In above example the PWM starts counting up on hex 0,
2 cycles later compare match → PWM to '0',
14 cycles later roll over → PWM to '1'
2 cycles later compare match → PWM to '0' , etc. until the completion of the 5 pulses.
The normal IRQ generation remains on during PWM output. If no IRQ's are wanted, the corresponding masks need to be set.

Figure 21. PWM Output in Up Count Mode

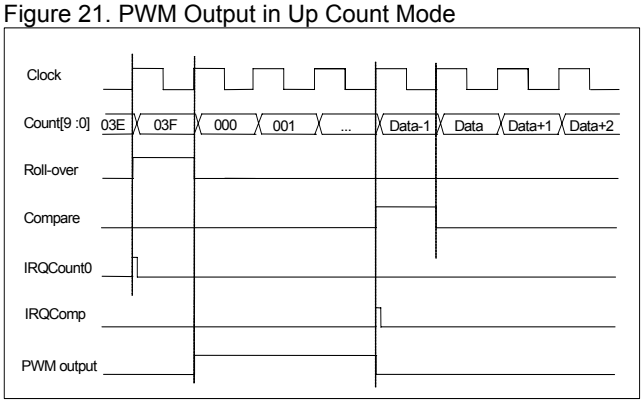
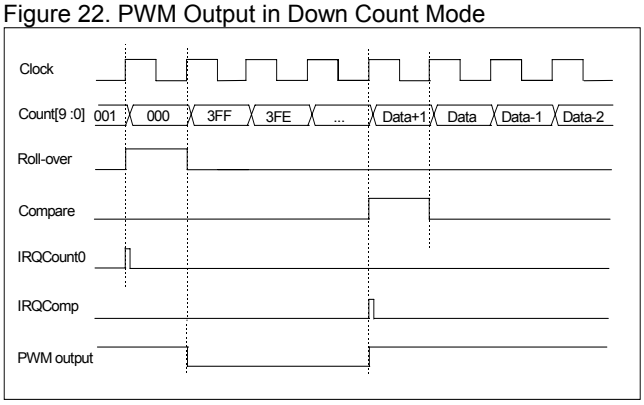


Figure 22. PWM Output in Down Count Mode



In Down Count Mode everything is inverted. The PWM output starts with the '1' value. Each Roll Over will set the output to '0' and each Compare Match will set it back to '1'. Due to this, the positive pulse length is always longer by 1 selected clock period compared to written value. Example: for 25% positive pulse duty cycle on 4 bit counter one must write 3 in counter if down-count instead of value 4 in case of up-count.

Note:
In downcount mode and limited pulse generation one must load the complementary pulse number value. I.e. for 5 pulses counting on 4 bits load bits[9 :4] with hex 3A (bin 111010).

8.4.2 PWM Characteristics

PWM resolution is : 10bits (1024 steps), 8bits (256 steps), 6bits (64 steps) or 4 bits (16 steps)
the minimal signal period is : 16 (4-bit) x Fmax* → 16 x 1/Ck[15] → 977 µs (32 KHz)
the maximum signal period is : 1024 x Fmin* → 1024 x 1/Ck[1] → 1024 s (32 KHz)
the minimal pulse width is : 1 bit → 1 x 1/Ck[15] → 61 µs (32 KHz)

* This values are for Fmax or Fmin derived from the internal system clock (32kHz). Much shorter (and longer) PWM pulses can be achieved by using the port A or RCClk as frequency input.

One must not use a compare value of hex 0 in up count mode nor a value of hex 3FF (or FF,3F, F if limited bit compare) in down-count mode.

8.4.3 PWM example

PWM on 4 bit setting and with option bit 0 don't care set.

PWM 4 bits

RegCDataL					PWM high level			
				compare	pwm in up count		PWM in down count	
3	2	1	0	value	(nbr_cycles / % high)		(nbr_cycles / % high)	
0	0	0	0	0	do not use		1	6.25
0	0	0	1	1	1	6.25	2	12.5
0	0	1	0	2	2	12.5	3	18.75
0	0	1	1	3	3	18.75	4	25
0	1	0	0	4	4	25	5	31.25
0	1	0	1	5	5	31.25	6	37.5
0	1	1	0	6	6	37.5	7	43.75
0	1	1	1	7	7	43.75	8	50
1	0	0	0	8	8	50	9	56.25
1	0	0	1	9	9	56.25	10	62.5
1	0	1	0	10	10	62.5	11	68.75
1	0	1	1	11	11	68.75	12	75
1	1	0	0	12	12	75	13	81.25
1	1	0	1	13	13	81.25	14	87.5
1	1	1	0	14	14	87.5	15	93.75
1	1	1	1	15	15	93.75	do not use	

PWM 4 bits (bit 0 don't care)

RegCDataL					PWM high level			
				compare	pwm in up count		PWM in down count	
3	2	1	0	value	(nbr_cycles / % high)		(nbr_cycles / % high)	
0	0	0	0	0	do not use		1	12.5
0	0	0	1	0	do not use		1	12.5
0	0	1	0	1	1	12.5	2	25
0	0	1	1	1	1	12.5	2	25
0	1	0	0	2	2	25	3	37.5
0	1	0	1	2	2	25	3	37.5
0	1	1	0	3	3	37.5	4	50
0	1	1	1	3	3	37.5	4	50
1	0	0	0	4	4	50	5	62.5
1	0	0	1	4	4	50	5	62.5
1	0	1	0	5	5	62.5	6	75
1	0	1	1	5	5	62.5	6	75
1	1	0	0	6	6	75	7	87.5
1	1	0	1	6	6	75	7	87.5
1	1	1	0	7	7	87.5	do not use	
1	1	1	1	7	7	87.5	do not use	

8.5 Counter Setup

RegCDataL[3:0], RegCDataM[3:0], RegCDataH[1:0] are used to store the initial count value called C_{Reg}**[9:0]** which is written into the count register bits **Count[9:0]** when writing the bit **Load** to '1' in **RegCCntl2**. This bit is automatically reset thereafter. The counter value **Count[9:0]** can be read out at any time, except when using non-debounced high frequency port A input clock. To maintain data integrity the lower nibble **Count[3:0]** must always be read first. The **ShCount[9:4]** values are shadow registers to the counter. To keep the data integrity during a counter read operation (3 reads), the counter values [9:4] are copied into these registers with the read of the count[3:0] register. If using non-debounced high frequency port A input the counter must be stopped while reading the **Count[3:0]** value to maintain the data integrity.
In down count mode an interrupt request **IRQCount0** is generated when the counter reaches 0. In up count mode, an interrupt request is generated when the counter reaches 3FF (or FF,3F,F if limited bit counting).

Never an interrupt request is generated by loading a value into the counter register.

When the counter is programmed from up into down mode or vice versa, the counter value **Count[9:0]** gets inverted. As a consequence, the initial value of the counter must be programmed after the **Up/Down** selection.

Loading the counter with hex 000 is equivalent to writing stop mode, the **Start** bit is reset, no interrupt request is generated.

How to use the counter;

If PWM output is required one has to decide first on which PA port to put it. After corresponding port Output Enable **OEnPA[n]** must be set **PWMoutPA[n]** = 1 in step 5. (n= 0 or 1)

1st, set the counter into stop mode (**Start**=0).
2nd, select the frequency and up- or down count mode in **RegCCntl1.**
3rd, write the data registers **RegCDataL, RegCDataM, RegCDataH** (counter start value and length)
4th, load the counter, **Load**=1, and choose the mode. (**EvCount**, **EnComp**=0)
5th, select bits **PWMoutPA[n]** in **RegPaCntl3** and **SelIntFull** in **RegSysCntl1**
6th, if compare mode desired , then write **RegCDataL, RegCDataM, RegCDataH** (compare value)
7th, set bit **Start** and select **EnComp** in **RegCCntl2**.

8.6 10-bit Counter Registers

Table 8.6.1. Register **RegCCntl1**

Bit	Name	Reset	R/W	Description
3	Up/Down	0	R/W	Up or down counting
2	CountFSel2	0	R/W	Input clock selection
1	CountFSel1	0	R/W	Input clock selection
0	CountFsel0	0	R/W	Input clock selection

Default : PA0 ,selected as input clock, Down counting

Table 8.6.2. Counter Input Frequency Selection with **CountFSel[2..0]**

CountFSel2	CountFSel1	CountFSel0	clock source selection
0	0	0	Port A PA[1] = non debounced only TimCk0
0	0	1	Prescaler Ck[15] typ. 16 kHz
0	1	0	Prescaler Ck[12] typ. 2 kHz
0	1	1	Prescaler Ck[10] typ. 512 Hz
1	0	0	Prescaler Ck[8] typ. 128 Hz
1	0	1	Prescaler Ck[4] typ. 8 Hz
1	1	0	Prescaler Ck[1] typ. 1 Hz
1	1	1	Port A PA[3/4]

Table 8.6.3. Register **RegCCntl2**

Bit	Name	Reset	R/W	Description
3	Start	0	R/W	Start/Stop control
2	EvCount	0	R/W	Event counter enable
1	EnComp	0	R/W	Enable comparator
0	Load	0	R/W	Write: load counter register; Read: always 0

Default : Stop, no event count, no comparator, no load

Table 8.6.4. System Control register **RegSysCntl1**

Bit	Name	Reset	R/W	Description
3	IntEn	0	R/W	*General interrupt enable*
2	Sleep	0	R/W	*Sleep mode*
1	SetIntFull	0	R/W	Compare Interrupt select (**note** 1)
0	***ChTmDis***	p 0*	R/W	Disable Test modes by setting it to 1 **(MUST be DONE)**

p 0* ***ChTmDis*** is cleared on POR to be able to enter test modes at EM.

Note:
At program start the user must write the **ChTmDis** bit to '1' to prevent from accidentally going into factory test mode. Setting this bit to '1' must be done after a minimum number of instructions, see table 8.6.5 below. Additionally the Port PA0 must not be declared as output before the same number of cycles are passed.
These precautions are necessary to guarantee proper factory circuit testing.

ChTmDis bit needs to be reconfirmed (write '1') at every access to register **RegSysCntl1**

Table 8.6.5. Number of instructions before cutting Test access

CPU frequency	Min Nb. of instructions before ChTmDis is set or PortPA[0] declared as an output
Basic frequency (32 kHz or 50 kHz)	4
Basic f. x 2 (64 kHz or 100 kHz)	8
Basic f. x 4 (128 kHz or 200 kHz)	16
Basic f. x 8 (256 kHz or 400 kHz)	32
Basic f. x 16 (512 kHz or 800 kHz)	64

By writing to **RegSysCntl1** – setting ChTmDis to 1 PORstatus will be cleared.
Test mode is totally disabled also if PortPA[0] is declared as an output. OenPA[0] = '1'
(**note** 1) Default : Interrupt on limited bit compare for Counter

Table 8.6.6. Register **RegCDataL**, Counter/Compare Low Data Nibble

Bit	Name	Reset	R/W	Description
3	CReg[3]	0	W	Counter data bit 3
2	CReg[2]	0	W	Counter data bit 2
1	CReg[1]	0	W	Counter data bit 1
0	CReg[0]	0	W	Counter data bit 0
3	Count[3]	0	R	Data register bit 3
2	Count[2]	0	R	Data register bit 2
1	Count[1]	0	R	Data register bit 1
0	Count[0]	0	R	Data register bit 0

Table 8.6.7. Register **RegCDataM**, Counter/Compare Middle Data Nibble

Bit	Name	Reset	R/W	Description
3	CReg[7]	0	W	Counter data bit 7
2	CReg[6]	0	W	Counter data bit 6
1	CReg[5]	0	W	Counter data bit 5
0	CReg[4]	0	W	Counter data bit 4
3	ShCount[7]	0	R	Data register bit 7
2	ShCount[6]	0	R	Data register bit 6
1	ShCount[5]	0	R	Data register bit 5
0	ShCount[4]	0	R	Data register bit 4

Table 8.6.8. Register **RegCDataH**, Counter/Compare High Data Nibble

Bit	Name	Reset	R/W	Description
3	BitSel[1]	0	R/W	Bit select for limited bit count/compare
2	BitSel[0]	0	R/W	Bit select for limited bit count/compare
1	CReg[9]	0	W	Counter data bit 9
0	CReg[8]	0	W	Counter data bit 8
1	ShCount[9]	0	R	Data register bit 9
0	ShCount[8]	0	R	Data register bit 8

Table 8.6.9. Counter Length Selection

	BitSel[1]	BitSel[0]	counter length
	0	0	10-Bit
	0	1	8-Bit
	1	0	6-Bit
	1	1	4-Bit

9. SVLD / 4-bit ADC

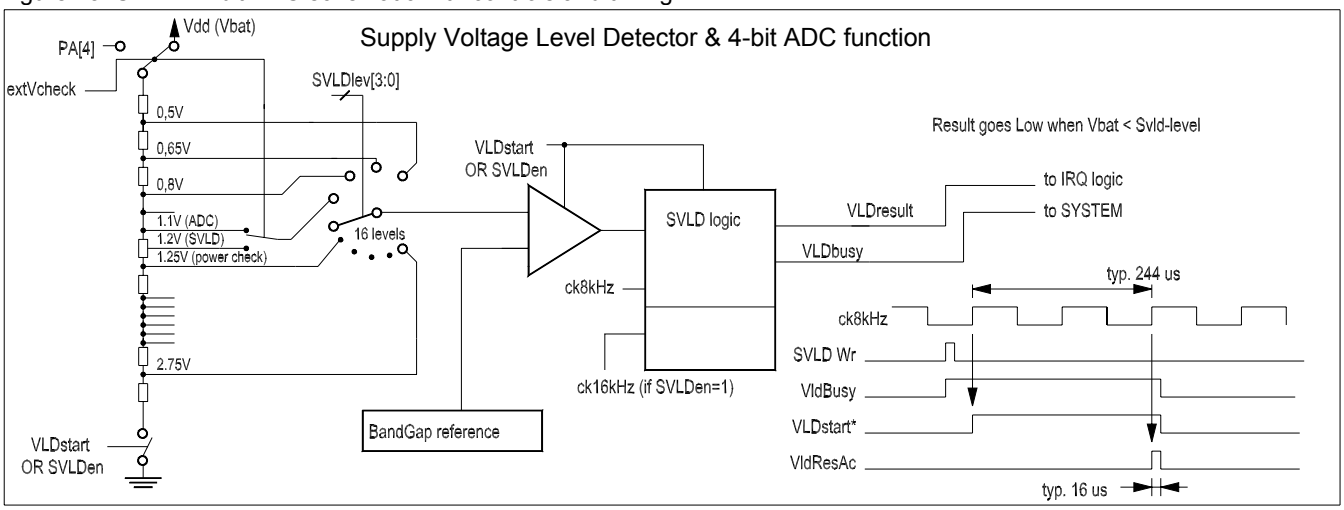
The EM6682 has a built-in circuitry made up of a comparator with band-gap reference and a resistor divider chain with 16 terminals to detect levels within the voltage supply range.

a. **S**upply **V**oltage **L**evel **D**etector (SVLD) to compare the positive power supply level V_{dd} against levels which are in the range of V_{ddmin} to V_{ddmax}. In this case **extVcheck** must be cleared to '0' (default).

b. Simple 4-bit **A**nalogue to **D**igital **C**onverter – ADC. Setting the **ExtVcheck** bit to '1' makes the PA[4] input an analog ADC input. PA[4] input voltage must not exceed V_{DD} + 0.3V

In Sleep mode both functions are disabled.

Figure 23. SLVD / 4-bit ADC schematic with controls and timing



SLVD level5 or SLVD level9 is used during Power On Reset for Power-Check to check the minimum operating voltage before the POR signal is released as described in Chapter 4.1.

When used as a SVLD the **ExtVCheck** bit in register **RegVldCntl** must be cleared to '0'. Then V_{dd} is selected as the input to the resistive divider which provides the comparator inputs. The SVLD level must be selected by writing the **RegSVLDlev** register. For proper operation only levels above Vdd min can be selected. Then the CPU activates the voltage comparison by writing the **VLDstart** bit to '1' in the register **RegVLDCntl**. The actual measurement starts on the next ck[14] (8kHz @ 32kHz SysClk) falling edge and lasts typ. 260 us. The busy flag **VldBusy** stays high from the time **VLDStart** is set to '1' until the measurement is finished. The worst case time until the result is available is 3.125 * ck[14] prescaler clock periods (32kHz → 382us). See figure 24 for details.

During the actual measurement (typ. 260us) the device will draw typically an additional 4µA of I_{VDD} current @ V_{dd}=1.5V. After the end of the measurement an interrupt request **IRQVLD** can be generated if V_{dd} is lower than the level which was selected. The interrupt is generated only if the mask **IRQSvld** bit is set to '1'. The result is available by inspection of the bit **VLDResult**. If the result is '0', then the power supply voltage was lower than the detection level value. If '1' the power supply voltage was higher than the detection level value. The value of **VLDResult** is not guaranteed while **VldBusy=1**.

An interrupt can be generated only if V_{dd} is lower than the selected level. **IRQSvld** bit is cleared by reading **RegIRQ2**.

Table 9.1 register **RegVldCntl**

Bit	Name	Reset	R/W	Description
3	ExtVcheck	0	W	PA[4] as positive input of divider chain
3	VLDResult	0	R*	VLD result flag
2	VLDStart	0	W	VLD start command
2	VLDBusy	0	R	VLD busy flag is on Until compare is finished
1	SVLDen	0	R/W	SVLD comparator is On continuously
0	NoWDtim	P	R/W	No watchdog timer

R*; VLDResult is not guaranteed while VLDBusy=1

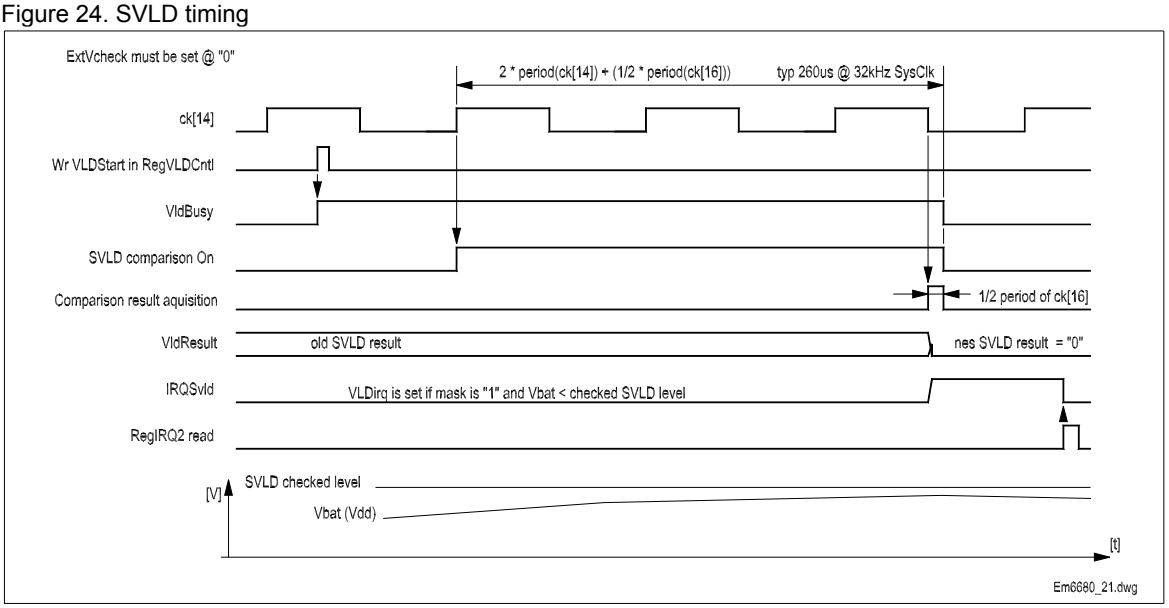
Note: The SVLD/ADC levels can be compatible with the low voltage specification. The metal option **opt_LV_SVLD_level allows choosing the low voltage levels when it is at 1.**

Low voltage mode: 16 levels between 0 and 1.8V.

Medium voltage mode: 16 levels between 0 and 3.0V.

Refer to electrical specifications.

Figure 24. SVLD timing



The **VLDresult** bit from the previous measurement stays in the register until the new measurements is finished.
For good measurements external noise or CPU activity should be as low as possible during the comparison.

Table 9.2 register **RegSVLDlev**

Bit	Name	POR	R/W	Description
3	SVLDlev[3]	1*	R/W	SVLD level select bit #3
2	SVLDlev[2]	0*	R/W	SVLD level select bit #2
1	SVLDlev[1]	0	R/W	SVLD level select bit #1
0	SVLDlev[0]	1	R/W	SVLD level select bit #0

SVLDlev[3:2]initialization depends on Metal option for Power-Check level **PClev**.

Level #9 is selected when **PClev** = '1' (as describe in table 9.2).

Level #5 is selected when **PClev** = '0'.

Table 9.3.1 SVLD level selection (typical values **V*SVLD*Nom**) ; medium voltage mode set by metal option

SVLDlev[3:0]				Nb.:	ADC	SVLD	Description of specialitis
MSB			LSB	Level #	ADCNom	SVLDNom	
0	0	0	0	0	0.5 V	Do not set	Do not use this level with SVLD
0	0	0	1	1	0.65 V	Do not set	Do not use this level with SVLD
0	0	1	0	2	0.80 V	Do not set	Do not use this level with SVLD
0	0	1	1	3	0.95 V	Do not set	Do not use this level with SVLD
0	1	0	0	4	**1.10 V**	**1.20 V**	Depends on **ExtVCheck** - ADC or SVLD
0	1	0	1	5	1.25 V	1.25 V	Default level after POR for Power Check
0	1	1	0	6	1.40 V	1.40 V	
0	1	1	1	7	1.55 V	1.55 V	
1	0	0	0	8	1.70 V	1.70 V	
1	0	0	1	9	1.85 V	1.85 V	Optional level after POR for Power Check
1	0	1	0	10	2.00 V	2.00 V	
1	0	1	1	11	2.15 V	2.15 V	
1	1	0	0	12	2.30 V	2.30 V	
1	1	0	1	13	2.45 V	2.45 V	
1	1	1	0	14	2.60 V	2.60 V	
1	1	1	1	15	2.75 V	2.75 V	Metal option or RegMFP2 Opt[8] allows selecting level 15 or 15b. Refer to chapter 15.
1	1	1	1	15b	3.00 V	3.00 V	

Table 9.3.2 ADC/SVLD level selection in low voltage mode (typical values V*SVLD*Nom)

SVLDlev[3:0]				Nb.:	ADC @1.5V	SVLD	Description of specialties
MSB			LSB	Level #	ADCNom	SVLDNom	
0	0	0	0	0	.35 V	-	Do not use this level with SVLD
0	0	0	1	1	.49 V	-	Do not use this level with SVLD
0	0	1	0	2	.49 V	-	Do not use this level with SVLD
0	0	1	1	3	0.58 V	-	Do not use this level with SVLD
0	1	0	0	4	0.67 V	-	Do not use this level with SVLD
0	1	0	1	5	0.77 V	-	Do not use this level with SVLD
0	1	1	0	6	0.85 V	-	Do not use this level with SVLD
0	1	1	1	7	0.94 V	0.922V	
1	0	0	0	8	1.04V	1.02V	
1	0	0	1	9	1.13 V	1.11V	Optional level after POR for Power Check
1	0	1	0	10	1.22 V	1.20V	
1	0	1	1	11	1.31 V	1.30V	
1	1	0	0	12	1.40 V	1.39V	
1	1	0	1	13	1.49 V	1.49V	
1	1	1	0	14	1.58 V	1.58V	
1	1	1	1	15	1.68 V	1.69V	

External source is coming from PA[4] as explained in Chapter 6.2 and shown on figure 10.

To implement a 4-bit ADC first **ExtVcheck** bit must be set to '1', that PA[4] input is connected to positive side of resistor divider chain. To find the level as fast as possible with successive approximation for instance it is advised to Set **SVLDen** bit to '1' to have comparator and resistive divider chain operational all the time when the PA[4] input is sampled with ck[15] (typ. 16kHz @ 32kHz SysClk) frequency. With SVLDlev[3:0] we can select one of 16 possible levels to check and by making max. 4 measurements at 4 different levels (if input PA[4] is stable) we have the result with successive approximation method.

In this case PA[4] input is blocked for all other functions, because its level can be in a zone where logic '0' or '1' are not well defined and this would generate an over consumption otherwise. So it is dedicated only to SVLD comparator input to be compared with internal band-gap reference. NoPullPA[4] must be set to '1' - Pull-UP/Down must be removed by register also.

In both cases if V_{dd} or PA[4] level is tested lower than the selected level an IRQ can be generated if enabled.

With **SVLDen** bit one can switch on the band-gap, resistive divider and Comparator continuously. Like that one can monitor V_{DD} or PA[4] level continuously, at higher frequency (ck[15]). Only at the beginning after setting the **SVLDen** at '1' one has to wait until **VLDbusy** drops to '0' indicating that system is powered up (band-gap reference and resistor divider are stabilized and comparator is ready to give proper result). This will increase power consumption by typ. 4µA @ V_{dd}=1.5V while used.

During continuously monitoring one can change **RegSVLDlev** register value on fly and the new result should be read only after about 1.5 * ck[15] to be sure it is a result of a new **SVLDlev** selection. Depending on CPUclk and divisions to obtained SysClk this can be 2 / 6 / 10 / 20 / 36 instruction after **RegSVLDlev** change for multiples by 1 / 2 / 4 / 8 / 16.

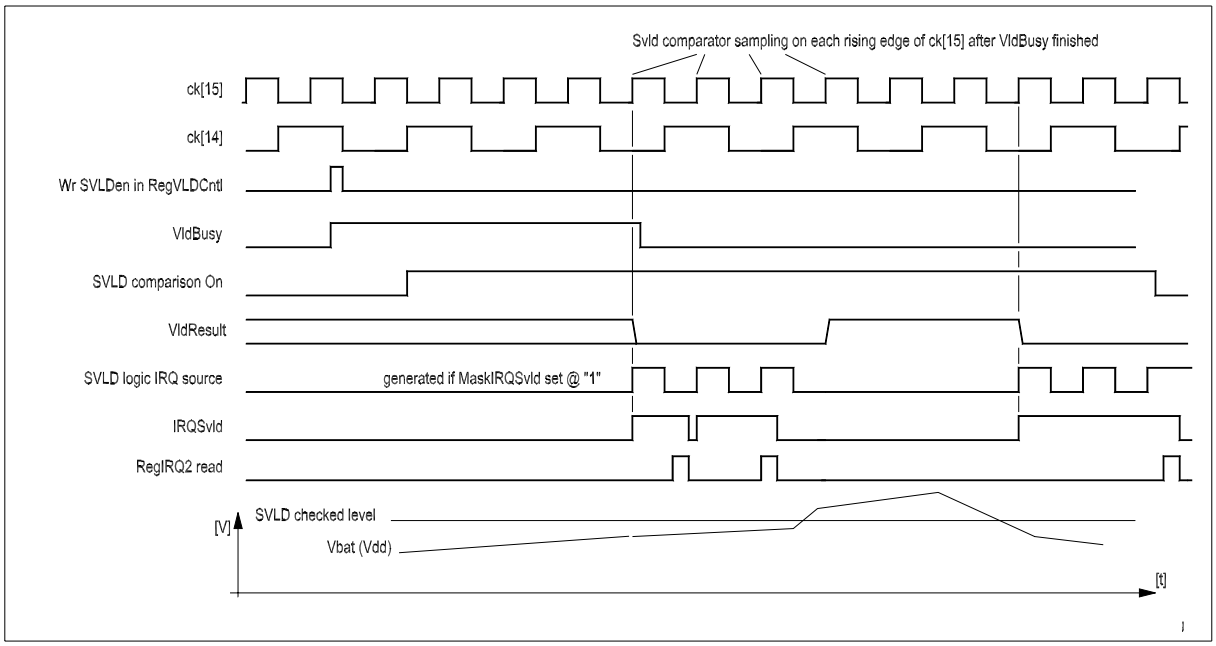
When fast monitoring is not necessary any more one can remove it by clearing **SVLDen** to '0'.

When SVLD logic is used for this fast monitoring IRQ can also be generated when checked level falls below its value.

9.1 SVLD trim:

A specific ADC or SVLD level can be factory trimmed to ±3%. Trimming will result in a specific use electrical specification for the intended ADC/SVLD levels and its usage. The trimming code is 4bits coded in **RegSVLDTrim**. (see memory map table in chapter 13). It is possible to modify by software this register. But after each POR its status will be refreshed with the factory trimming code automatically.

Figure 25. SVLD timing in “ADC” mode when SVLDen set @ “1”



Due to IRQSvld which can come very fast – with ck[15] there is danger that immediately after coming out from IRQ subroutine new IRQSvld which came during that time put uC back in IRQ subroutine and software can be stacked at this place until checked input is lower then SVLD level. Otherwise IntEn register must be cleared in IRQ subroutine already !! or even better to use this function by reading the SVLD result only and not setting the MaskIRQSvld

10. RAM

The EM6682 has one 80x4 bit static RAM built-in located on addresses hex 0 to 4F. All the RAM nibbles are direct addressable.

Figure 26. RAM Architecture

RAM 80 x 4 = direct addressable		
Adr [hex]	**RAM location**	**Read / Write**
4F	RAM_79	4 bit R/W
4E	RAM_78	4 bit R/W
4D	RAM_77	4 bit R/W
4B	RAM_76	4 bit R/W
. . . .	. . . .	. . . .
04	RAM_04	4 bit R/W
03	RAM_03	4 bit R/W
02	RAM_02	4 bit R/W
01	RAM_01	4 bit R/W
00	RAM_00	4 bit R/W

RAM Extension : Unused R/W Registers can often be used as possible RAM extension. Be careful not to use registers which start, stop, or reset some functions.

11. Interrupt Controller

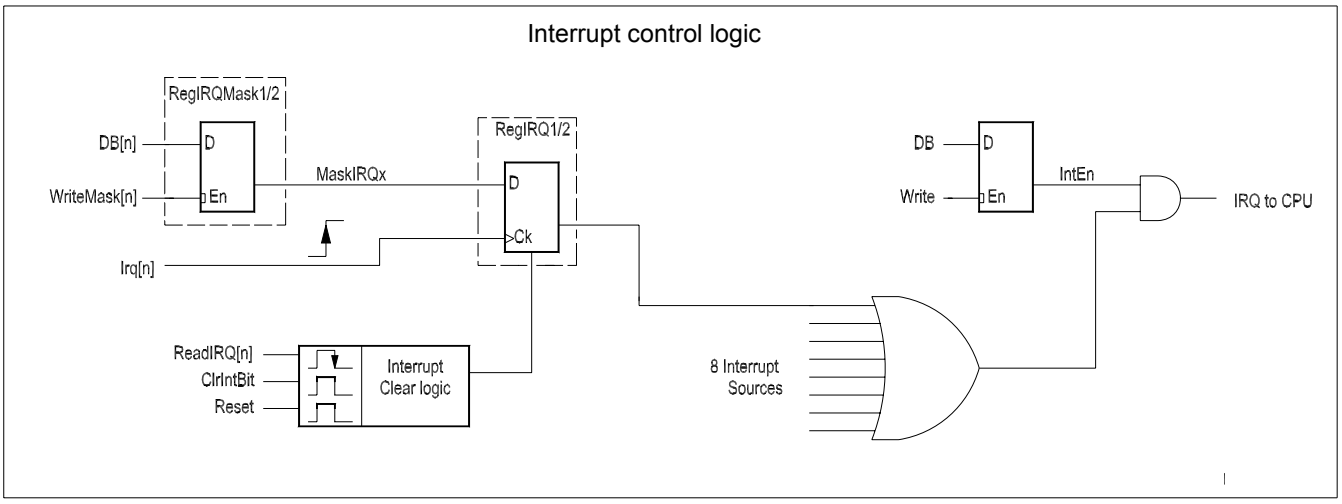
The EM6682 has 8 different interrupt request sources masked individually. These are:

External (2)	**- Port A,**	**PA[0/5] and PA[3/4] inputs**
	- Compare	**PA[4] input**
Internal (6)	**- Prescaler (2x)**	**ck[1], 64Hz/8Hz**
	- 10-bit Counter (2x)	**Count0, CountComp**
	- SVLD (1)	**End of measure when level is low**
	- Serial Interface (1)	**8 bit transfered**

The SVLD and the PA[4] level check share the same interrupt line.
Serial Interface could be put under Internal when Serial clock is coming form EM6682 or External when Serial clock is external.

To be able to send an interrupt to the CPU, at least one of the interrupt request flags must be set (**IRQxx**) and the general interrupt enable bit **IntEn** located in the register **RegSysCntl1** must be set to 1. The interrupt request flags can only be set by a positive edge of **IRQxx** with the corresponding mask register bit (**MaskIRQxx**) set to 1.

Figure 27. Interrupt control logic for generating and clearing interrupts



At power on or after any reset all interrupt request mask registers are cleared and therefore do not allow any interrupt request to be stored. Also the general interrupt enable **IntEn** is set to 0 (No IRQ to CPU) by reset.

After each read operation on the interrupt request registers **RegIRQ1** or **RegIRQ2** the contents of the addressed register are reset. Therefore one has to make a copy of the interrupt request register if there was more than one interrupt to treat. Each interrupt request flag may also be reset individually by writing 1 into it (ClrIntBit).

Interrupt handling priority must be resolved through software by deciding which register and which flag inside the register need to be serviced first.

Since the CPU has only one interrupt subroutine and because the **IRQxx** registers are cleared after reading, the CPU does not miss any interrupt request which comes during the interrupt service routine. If any occurs during this time a new interrupt will be generated as soon as the software comes out of the current interrupt subroutine.

Any interrupt request sent by a periphery cell while the corresponding mask is not set will not be stored in the interrupt request register. All interrupt requests are stored in their **IRQxx** registers depending only on their corresponding mask setting and not on the general interrupt enable status. Whenever the EM6682 goes into HALT Mode the **IntEn** bit is automatically set to 1, thus allowing to resume from Halt Mode with an interrupt.

11.1 Interrupt control registers

Table 11.1.1 Register **RegIRQ1**

Bit	Name	Reset	R/W	Description
3	IRQCount0	0	R/W*	Counter interrupt request when at 0
2	IRQCntComp	0	R/W*	Counter interrupt request when compare True
1	IRQPA[3/4]	0	R/W*	Port A PA[3/4] interrupt request
0	IRQPA[0/5]	0	R/W*	Port A PA[0/5] interrupt request

W*; Writing of 1 clears the corresponding bit.

Table 11.1.2 Register **RegIRQ2**

Bit	Name	Reset	R/W	Description
3	IRQHz1	0	R/W*	Prescaler interrupt request of 1Hz
2	IRQHz64/8	0	R/W*	Prescaler interrupt request of 64 Hz or 8 Hz
1	IRQSvld	0	R/W*	SVLD or Compare interrupt request
0	IRQSerial	0	R/W*	Serial interface interrupt request

W*; Writing of 1 clears the corresponding bit.

Table 11.1.3 Register **RegIRQMask1**

Bit	Name	Reset	R/W	Description
3	MaskIRQCount0	0	R/W	Counter when at 0 interrupt mask
2	MaskIRQCntComp	0	R/W	Counter compare True interrupt mask
1	MaskIRQPA[3/4]	0	R/W	Port A PA[3/4] interrupt mask
0	MaskIRQPA[0/5]	0	R/W	Port A PA[0/5] interrupt mask

Interrupt is not stored if the mask bit is 0.

Table 11.1.4 Register **RegIRQMask2**

Bit	Name	Reset	R/W	Description
3	MaskIRQHz1	0	R/W	Prescaler 1Hz interrupt mask
2	MaskIRQHz64/8	0	R/W	Prescaler 64 Hz or 8 Hz interrupt mask
1	MaskIRQSvld	0	R/W	SVLD or Compare interrupt mask
0	MaskIRQSerial	0	R/W	Serial interface interrupt mask

Interrupt is not stored if the mask bit is 0.

12. PERIPHERAL MEMORY MAP

Reset values are valid after power up or after every system reset.

Register Name	Add Hex	Add Dec.	Reset Value	Read Bits	Write Bits	Remarks
			b'3210	Read / Write Bits		
Ram1_0	00	0	xxxx	0: Data0 1: Data1 2: Data2 3: Data3		Direct addressable Ram 80 x 4 bit
Ram1_63	4F	79	xxxx	0: Data0 1: Data1 2: Data2 3: Data3		Direct addressable Ram 80 x 4 bit
RegPA0	50	80	0000	0: PA[0] 1: PA[1] 2: PA[2] 3: PA[3]	0: PAout[0] 1: PAout[1] 2: PAout[2] 3: PAout[3]	PortA [3:0] Direct input read, Output data register
RegPa0OE	51	81	0***0***00 ***0*** = after PORend	0: OEnPA[0] 1: OEnPA[1] 2: OEnPA[2] 3: OEnPA[3]		PortA [3:0] Output enable active Hi,
RegPaCntl1	52	82	pppp p = POR	0: EdgeFallingPA[0/5] 1: EdgeFallingPA[3/4] 2: debunceNoPA[0/5] 3: debunceNoPA[3/4]		PortA [3:0] control1 Debounce Yes/No & Faling / Rising edge
RegPaCntl2	53	83	pppp p = POR	0: IrqPA[0l/5h] 1: IrqPA[3l/4h] 2: WUchEnPA[0/5] 3: WUchEnPA[3/4]		PortA [3:0] control2 WakeUp on change enable & Irq source from PA select
Pa0noPDown	54	84	pppp p = POR	0: NoPdPA[0] 1: NoPdPA[1] 2: NoPdPA[2] 3: NoPdPA[3]		Option register Pull/down selection on PA[3:0] Default : pull-down ON
Pa0NchOpenDr	55	85	pppp p = POR	0: NchOpDrPA[0] 1: NchOpDrPA[1] 2: NchOpDrPA[2] 3: NchOpDrPA[3]		Option register N/channel Open Drain Output on PA[3:0] Default : CMOS output
RegFreqRst	56	86	ppxx	0: foutSel[0] 1: foutSel[1] 2: PA[3/4]resIn 3: InResAH		Output Frequency select and Input reset Control
RegSCntl1	57	87	0000	0: MSBnLSB 1: POSnNeg 2: MS0 3: MS1		Serial interface control 1
RegSCntl2	58	88	0000	0: OM[0] 1: RCoscOff 2: Status 3: Start		Serial interface control 2
RegSDataL	59	89	0000	0: SerDataL[0] 1: SerDataL[1] 2: SerDataL[2] 3: SerDataL[3]		Serial interface low data nibble
RegSDataH	5A	90	0000	0: SerDataH[0] 1: SerDataH[1] 2: SerDataH[2] 3: SerDataH[3]		Serial interface high data nibble
RegCCntl1	5B	91	0000	0: CountFSel0 1: CountFSel1 2: CountFSel2 3: Up/Down		10-bit counter control 1; frequency and up/down

Register Name	Add Hex	Add Dec.	Reset Value	Read Bits	Write Bits	Remarks
			b'3210	Read / Write Bits		
RegCCntl2	5C	92	0000	0: '0' 1: EnComp 2: EvCount 3: Start	0: Load 1: EnComp 2: EvCount 3: Start	10-bit counter control 2; comparison, event counter and start
RegCDataL	5D	93	0000	0: Count[0] 1: Count[1] 2: Count[2] 3: Count[3]	0: CReg[0] 1: CReg[1] 2: CReg[2] 3: CReg[3]	10-bit counter data low nibble
RegCDataM	5E	94	0000	0: Count[4] 1: Count[5] 2: Count[6] 3: Count[7]	0: CReg[4] 1: CReg[5] 2: CReg[6] 3: CReg[7]	10-bit counter data middle nibble
RegCDataH	5F	95	0000	0: Count[8] 1: Count[9] 2: BitSel[0] 3: BitSel[1]	0: CReg[8] 1: CReg[9] 2: BitSel[0] 3: BitSel[1]	10-bit counter data high bits
RegPA1	60	96	p000	0: PA[4] 1: PA[5] 2: OEnPA[5] 3: NchOpDrPA[5]	0: -- 1: PAout[5] 2: OEnPA[5] 3: NchOpDrPA[5]	PortA [5:4] Direct input read, Output data register with Output enable active Hi
RegPaCntl3	61	97	pppp	0: PWMoutPA[0] 1: PWMoutPA[1] 2: SerialCkPA[1] 3: SerialStPA[3]		PortA Control3 Output distribution on PA[0], PA[1] and PA[3]
RegPaCntl4	62	98	ppPP	0: freqOutPA[2] 1: Sout/rstPA[2] 2: : freqOutPA[5] 3: NoPdPA[5]		PortA Control4 Output distribution on PA[2] and PA[5]
RegIRQMask1	65	101	0000	0: MaskIRQPA[0/5] 1: MaskIRQPA[3/4] 2: MaskIRQCntComp 3: MaskIRQCount0		Port A & Counter interrupt mask; masking active 0
RegIRQMask2	66	102	0000	0: MaskIRQSerial 1: MaskIRQSvld 2: MaskIRQHz64/8 3: MaskIRQHz1		Prescaler, SVLD & serial interf. interrupt mask; masking active low
RegIRQ1	67	103	0000	0: IRQPA[0/5] 1: IRQPA[3/4] 2: IRQCntComp 3: IRQCount0	0:RIRQPA[0/5] 1:RIRQPA[3/4] 2:RIRQCntComp 3:RIRQCount0	Read: port A & Counter interrupt Write: Reset IRQ if data bit = 1.
REgIRQ2	68	104	0000	0: IRQSerial 1: IRQSvld 2: IRQHz64/8 3: IRQHz1	0:RIRQSerial 1:RIRQSvld 2:RIRQHz64/8 3:RIRQHz1	Read: Prescaler, SVLD & serial interface interrupt. Write: Reset IRQ if data bit = 1
RegSysCntl1	69	105	000p p = POR	*0: ChTmDis* 1: SelIntFull 2: '0' 3: IntEn	*0: ChTmDis* 1: SelIntFull 2: Sleep 3: IntEn	System control 1; *ChTmDis only usable only for EM test modes*
RegSysCntl2	6A	106	Pp00 p = POR	0: WDVal0 1: WDVal1 2: SleepEn 3: PORstatus	0: -- 1: -- 2: SleepEn 3: WDReset	System control 2; watchdog value and periodical reset, enable sleep mode
RegSleepCR	6B	107	pppp p = POR	0: SCRsel0 1: SCRsel1 2: SleepCntDis 3: NoPullPA[4]		Sleep Counter reset control

Register Name	Add Hex	Add Dec.	Reset Value	Read Bits	Write Bits	Remarks
			b'3210	Read / Write Bits		
RegPresc	6C	108	0000	0: DebSel 1: PrIntSel 2: '0' 3: ExtCPUclkON	0: DebSel 1: PrIntSel 2: ResPresc 3: ExtCPUclkON	Prescaler control; Debouncer, prescaler interrupt select and reset, External CPU clock enable
IXLow	6E	110	xxxx	0: IXLow[0] 1: IXLow[1] 2: IXLow[2] 3: IXLow[3]		Internal µP index register low nibble; for µP indexed addressing
IXHigh	6F	111	xxxx	0: IXHigh[4] 1: IXHigh[5] 2: IXHigh[6] 3: '0'	0: IXHigh[4] 1: IXHigh[5] 2: IXHigh[6] 3: --	Internal µP index register high nibble; for µP indexed addressing
RegVldCntl	73	115	000p	0: NoWDtim 1: SVLDen 2: VldBusy 3: VldResult	0: NoWDtim 1: SVLDen 2: VldStart 3: ExtVcheck	Voltage level detector & RC osc. control
RegSVLDlev	74	116	pPpp	0: SVLDlev[0] 1: SVLDlev[1] 2: SVLDlev[2] 3: SVLDlev[3]		SVLD test voltage level select
RegOscTrim1	75	117	0111*	0: RegOscTrim[4] 1: RegOscTrim[5] 2: RegOscTrim[6] 3: RegOscTrim[7]		Oscillator trimming word, MSB
RegOscTrim2	76	118	1111*	0: RegOscTrim[0] 1: RegOscTrim[1] 2: RegOscTrim[2] 3: RegOscTrim[3]		Oscillator trimming word, LSB
RegSVLDTrim	77	119	1000*	0: RegSVLDTrim[0] 1: RegSVLDTrim[1] 2: RegSVLDTrim[2] 3: RegSVLDTrim[3]		SVLD trimming word
RegMFP0	79	121	pppp	0:Opt[0] 1:Opt[1] 2:Opt[2] 3:Opt[3]		PA4 pull up/down selection Counter clock option Serial Interface clock Debouncer clock
RegMFP1	7A	122	pppp	0:Opt[4] 1:Opt[5] 2:Opt[6] 3:Opt[7]		RC frequency base selection RC frequency selection RC frequency selection RC frequency selection
RegMFP2	7B	123	pppp	0:Opt[8] 1: 2: 3:		ADC / SVLD level #5 selection Not used Not used Not used
RegTestEM1	7E	126	pppp	0: Tmsel[0] 1: Tmsel[1] 2: Tmsel[2] 3: disablePOR		For EM test only
RegTestEM2	7F	127	pppp	0: OeTm0 1: OeTm1 2: TestResSys 3: TestPOR		For EM test only

p = defined by POR at '0' (power on reset) only
P = defined by POR at '1' (power on reset) only
x = undefined state by reset (register must be written before used)
RegMFP0, RegMFP1 and **RegMFP2** can be forced to 1 or 0 by metal option. (See metal option chapter 15).

RegTestEm1 and **RegTestEm2** can be written only if ***ChTmDis*** in **RegSysCntl1** is '0'. They are used for EM test only and are Write only. At program start the user must write the **ChTmDis** bit to '1' to prevent from accidentally going into factory test mode.
Setting this bit to '1' must be done after a minimum number of instructions, see table 8.6.5 below. Additionally the Port PA0 must not be declared as output before the same number of cycles are passed.
These precautions are necessary to guarantee proper factory circuit testing.

ChTmDis bit needs to be reconfirmed (write '1') at every access to register **RegSysCntl1**

Table 11.1.5. Number of instructions before cutting Test access

CPU frequency	**Min Nb. of instructions before ChTmDis is set or PortPA[0] declared as an output**
Basic frequency (32 kHz or 50 kHz)	4
Basic f. x 2 (64 kHz or 100 kHz)	8
Basic f. x 4 (128 kHz or 200 kHz)	16
Basic f. x 8 (256 kHz or 400 kHz)	32
Basic f. x 16 (512 kHz or 800 kHz)	64

13. Active Supply Current test

For this purpose, five instructions at the end of the ROM will be added. This will be done at EM Marin.
User can use only up to 1499 Instructions (the rest – 37 instructions are used for EM tests).

```
TESTLOOP :  STI     00H,    0AH             ;TEST LOOP
            LDR     1BH
            NORX    FFH
            JPZ     TESTLOOP
            JMP     0
```

To stay in the testloop, these values must be written in the corresponding addresses before jumping in the loop:

1BH:	0101b
32H:	1010b
6EH:	0010b
6FH:	0011b

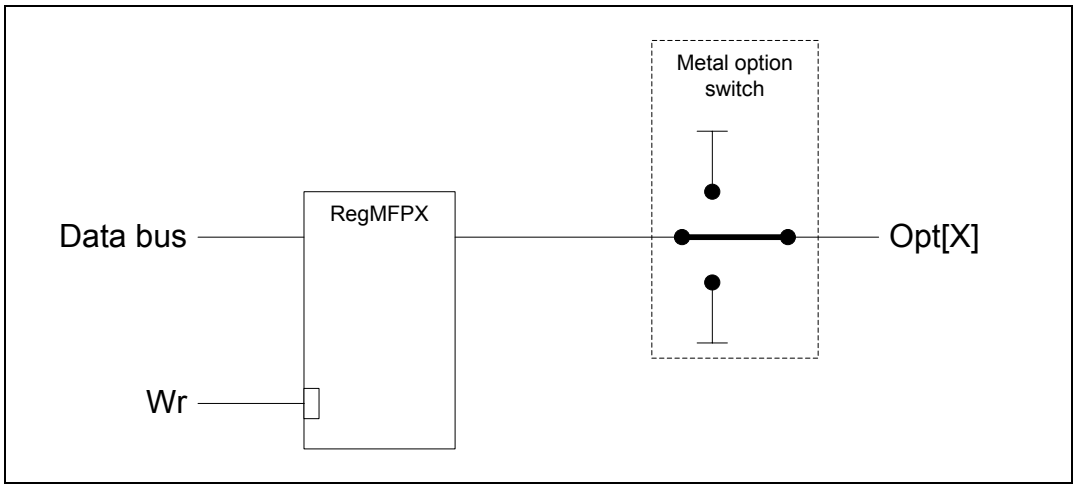
Free space after last instruction: JMP 00H (0000)

Remark: empty space within the program are filled with NOP (FOFF).

14. Mask Options

Most options which in many µControllers are realized as metal mask options and directly user selectable with the control registers, therefore allowing a maximum freedom of choice. Some of these metal options can be set by registers. As describe in the following figures. It allows forcing the option to 1, 0 or to the related register. Maks option has priority against register settings, see figure 28.

Figure 28. Metal option or register selection.



The following options can be selected at the time of programming the metal mask ROM.

14.1 Input / Output Ports

14.1.1 Port A Metal Options

The portA5 and portA[3:0] inputs can have Pull-up or no pull-up and Pull-down or no pull-down. The pull-up is only active in Nch. open drain mode. Concerning portA4, it is possible to select pull-up or pull-down by metal option but a register is also available in **RegMFP0[0]**.

The total pull value (pull-up or pull-down) is a series resistance out of the resistance R1 (in range from 0 – 110 kΩ) and the switching transistor. As a switching transistor the user can choose between a high impedance (weak) or a low impedance (strong) switch. Weak , strong or none must be chosen. The default is strong. The default resistor R1 value is 100 kΩ.

Figure 29. PA[5], PA[3:0] metal option architecture

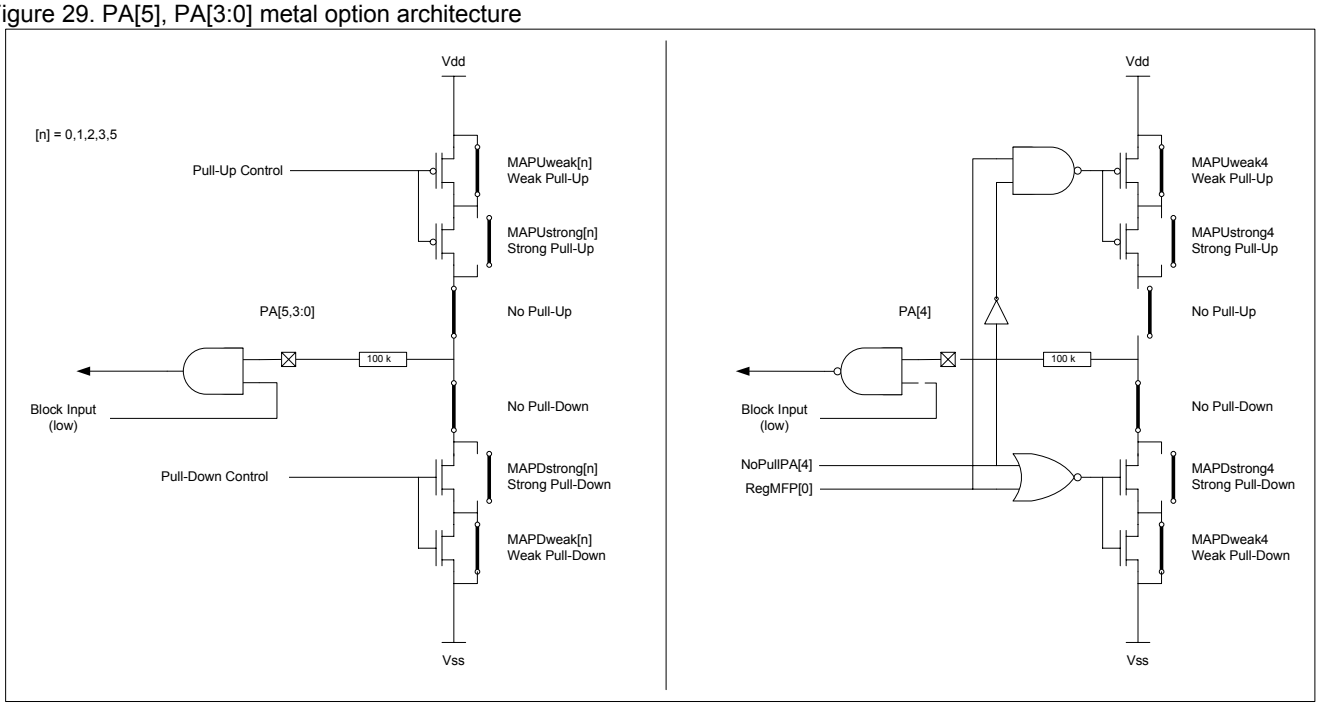


Table 14.1.1 Pull-down Metal mask Options

	Description	Strong Pull-down	Weak Pull-down	R1 Value Typ.100k	NO Pull-Down
Option Name		1	2	3	4
MAPD[5]	PA[5] input pull-down				
MAPD[4]	PA[4] input pull-down				
MAPD[3]	PA[3] input pull-down				
MAPD[2]	PA[2] input pull-down				
MAPD[1]	PA[1] input pull-down				
MAPD[0]	PA[0] input pull-down				

To select an option put an **X** in column 1,2 and 4 and reconfirm the R1 value in column 3.

The default value is : strong pull-down with R1=100 kΩ
→ Total value of typ. 98 kΩ at V_{dd} =3.0V

Table 14.1.2 Pull-up Metal mask Options

	Description	Strong Pull-up	Weak Pull-up	R1 Value Typ.100k	NO Pull-up
Option Name		1	2	3	4
MAPU[5]	PA[5] input pull-up				
MAPU[4]	PA[4] input pull-up				
MAPU[3]	PA[3] input pull-up				
MAPU[2]	PA[2] input pull-up				
MAPU[1]	PA[1] input pull-up				
MAPU[0]	PA[0] input pull-up				

To select an option put an **X** in column 1,2 and 4 and reconfirm the R1 value in column 3.

The default value is : strong pull-up with R1=100 kΩ
→ Total value of typ. 99 kΩ at V_{dd} =3.0V

PA[4] can have Pull-Up OR Pull-Down option selectable by metal option. In this case, the selected pull has effect before the software runs. Otherwise if the metal option is connected to the register RegMFP0[0] (see figure 28), it is possible to select the direction by software. In this case, it is not possible to set the direction before the software runs.

.

14.1.2 RC oscillator Frequency Option

Option Name		Default Value	User Value
		A	B
RCfreq	RC osc Frequency	**32 kHz**	

By default the RC oscillator frequency is typ. **32 kHz** With option RCfreq. Other possibilities are: **64kHz**, **128kHz**, **256kHz** and **500kHz** or **50kHz**, **100kHz**, **200kHz**, **400kHz** or max. **800kHz**. It is possible to use the register **RegMFP1 Opt[7:4]** to set the RC frequency by writing ***reg*** in user value. In low power mode only **128kHz**, **64kHz** or **32kHz** and **200kHz**, **100kHz** or **50kHz** are available. Refer to chapter 5.2.

14.1.3 Debouncer Frequency Option

Option Name		Default Value	User Value
		A	B
MDeb	Debouncer freq.	**Ck[11]**	

By default the debouncer frequency is Ck[11]. The user may choose Ck[14] instead of Ck[11].
Ck[14]corresponds to maximum 0.25ms debouncer time in case of a 32kHz System Clock – SysClk. It is possible to use the register **RegMFP0 Opt[3]** to select the debouncer clock by writing ***reg*** in user value. Refer to chapter 5.3.

14.1.4 Power-Check Level Option

Option Name		Default Value	User Value
		A	B
PClev.	Power-Check level	**#5**	

Higher frequency can not work well if Voltage is too low. So this option must be selected with help of EM to guarantee proper operation. Possible options are SVLD#5 (default – to be used with “low” frequency) and SVLD#9 for “high” frequency. For the voltage level reference see the electrical parameters in chapter 18.5.

14.1.5 ADC/SVLD Voltage Level #15

Option Name		Default Value	User Value
		A	B
HisvldLev.	ADC/SVLD lev.#15	**#15**	

By default the highest ADC/SVLD Voltage Level is #15 but user can select also the level 15b. It is possible to use the register **RegMFP2 Opt[8]** to select the ADC/SVLD level #15 by writing ***reg*** in user value. When Opt[8] = ‘1’ the level 15b is selected. For the voltage level reference see the electrical parameters in chapter 18.5.

14.1.6 Counter Update option

Option Name		Default Value	User Value
		A	B
CntF	Counter clock source selector	**SysClk**	**RCclk**

By default the counter is updated by Sysclk (32 or 50kHz typ) and the highest counter frequency is Sysclk/2 (16 or 25kHz Typ). The other possibility is to select CPUclk/2 for counter update freq. Which gives a possibility to replace port A input at selection 7 by CPU clock divided by 2. It is possible to use the register **RegMFP0 Opt[1]** to select the counter update clock source by writing ***reg*** in user value. If **DebouncerNoPA[3/4]** in **RegPACntl[1]** is ‘1’ then the resulting clock on timer selection 7 is CPUClk divided by 4. If **DebouncerNoPA[3/4]** is ‘0’ then the resulting clock is CpuClk divided by 2. Refer to chapter 8.2.

Note: when the option **opt_LV_CntFrc1** is on RC, the CPUClk is not divided by two and when **DebouncerNoPA[3/4]** is ‘1’ (debouncer off) the resulting clock is CPUClk divided by 2 instead of 4.

Note: CPUClk = RCClk if no external clock used. In case of external clock, CPUClk is equal to the PA[1] input clock.

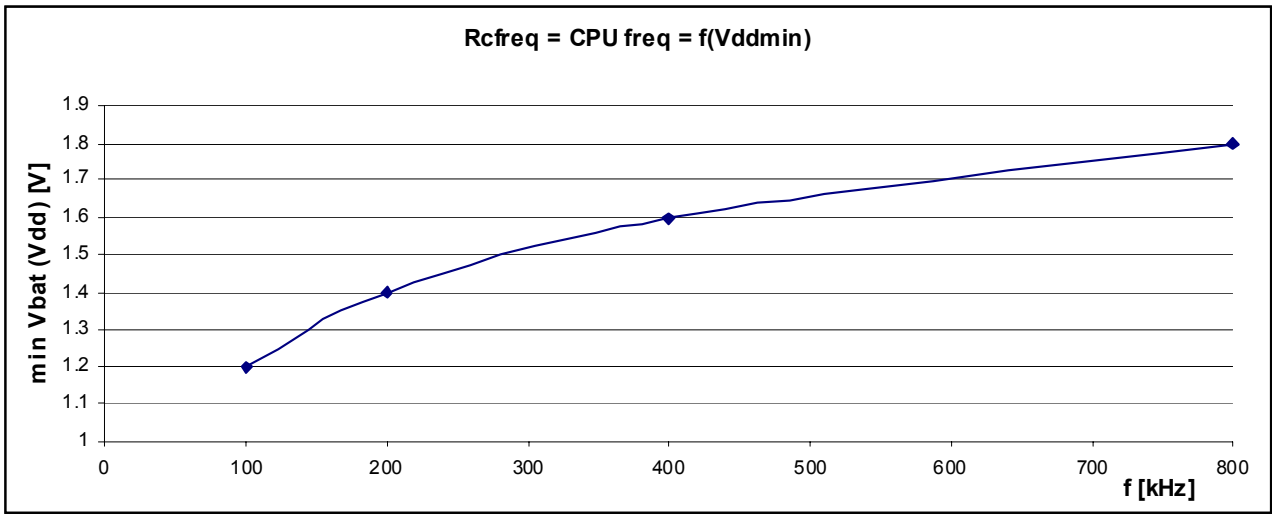
14.1.7 No regulator option

Option Name		Default Value	User Value
		A	B
NoReg	Voltage regulator disable	Enable	

By default the regulator voltage is enable in the 6682. It possible to clamp it to Vdd with the option **NoReg** when Vdd goes below 1.5V. When 0.9 < Vdd < 1.8 the regulator must be off (Vreg connected to Vdd). When 1.5 < Vdd < 5.5, the regulator must be enable.

Note: The minimum voltage is also depending to the maximum working frequency. Below is recommended minimum V_{DD} voltage for different RC oscillator frequencies, which are CPU frequencies to guarantee proper operation. V_{DD} must be above this proposed line in graph for selected frequency. Regulator must be adapted consequently.
Please contact EM for proper selection. 3T (3 tresholds) must be used for frequencies above 300 kHz.

Figure 30. Minimum V_{DD} = f(RC oscillator)



14.1.8 SVLD level set

Option Name		Default Value	User Value
		A	B
opt_LV_SVLD_level	SVLD & ADC level set	MV	

By default the original medium voltage specification defines 16 voltage levels between 3V and VSS. The user may choose low voltage specification. In this case, the 16 levels are spread from 1.8V to VSS. See electrical chapter 18.5.

14.1.9 Bit 0 don't care

Option Name		Default Value	User Value
		A	B
opt_Bit0DontCare	Counter Reg. level	Disable	

By default this option is disabled and timer runs on 10bits. When it is enabled, the timer bit0 has no action anymore. In this configuration, the timer acts as it would be a 9 bits timer with PWM on 9, 7, 8 or 3 bits.

14.1.10 Counter clock source

Option Name		Default Value	User Value
		A	B
Opt_CntFrc1	Counter clock source option	RC/2	

This option has a sense only if option **CntF** is set to RC oscillator. In this case **Opt_CntFrc1** selects **RC/2** or **RC** as counter clock source.

14.1.11 Power check level init

Option Name		Default Value	User Value
		A	B
Opt_Sleep_force_PWRC	PWRC active after reset	Disable	

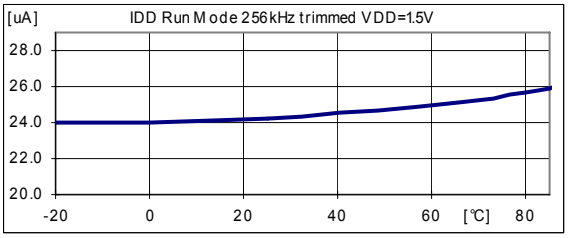
By default this option is disable and the power check is made only on the start-up of the chip. When this option is enable, after each reset, a power check is done compare with the last SVLD level selction before the reset.

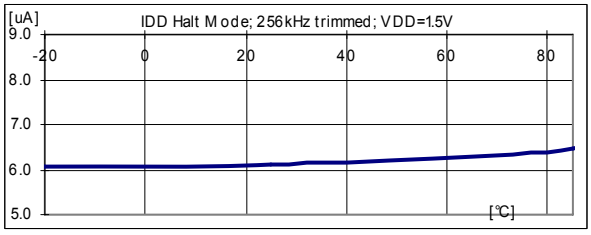
Note: To get out from the sleep mode, the chip must be reset then if this option is enable, after each sleep a power check is done with the SVLD level selected before going in sleep mode.

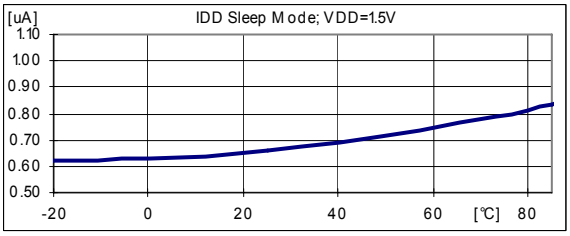
15. Typical Behaviour

Following graphics show the typical temperature and voltage behaviour of selected parameters. All measures were performed at EM on EM6681 qualification parts.

15.1 Temperature

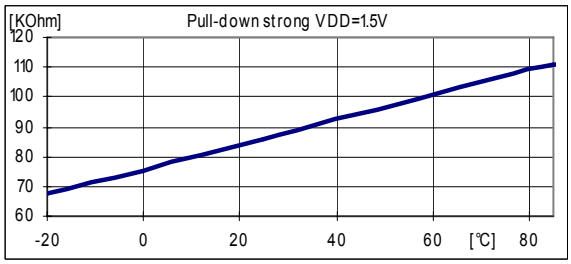


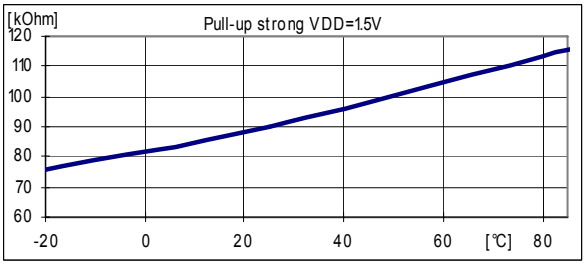




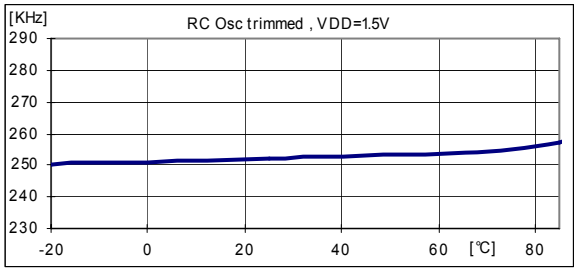
IVDD active mode, Standby mode, Sleep mode

Pull-up and Pulldown resistance

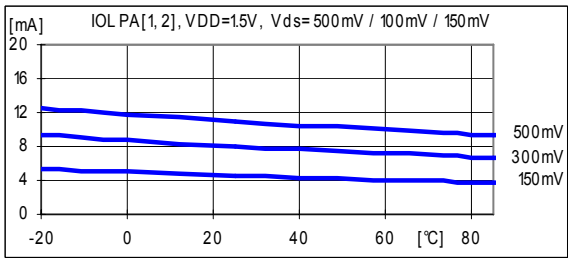


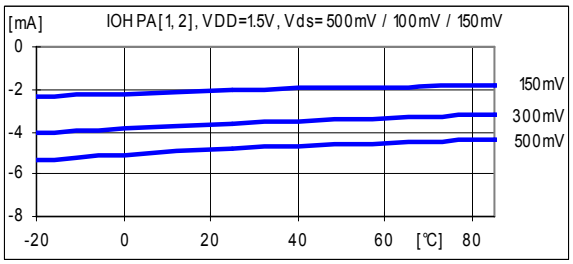


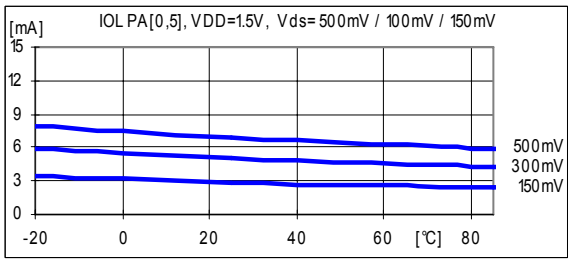
RC oscillation frequency

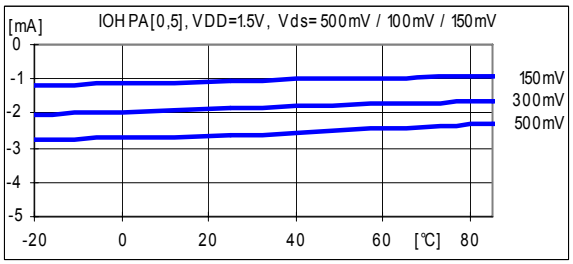


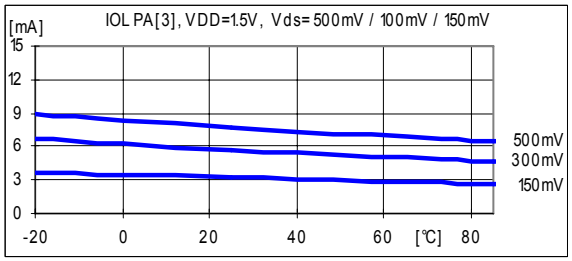
IOL on PA[2,1], IOL on PA[5,0], IOL on PA3, IOH on PA[2,1], IOH on PA[5,0], IOH on PA[3]

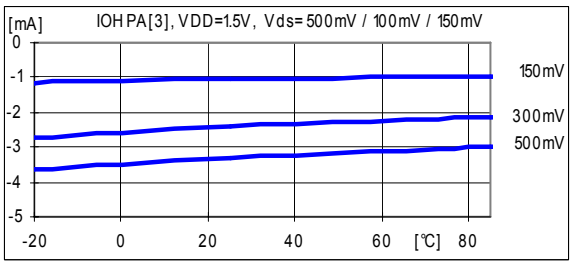






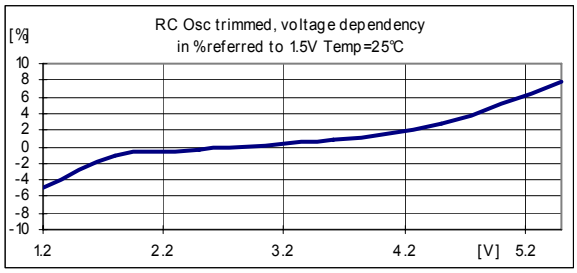




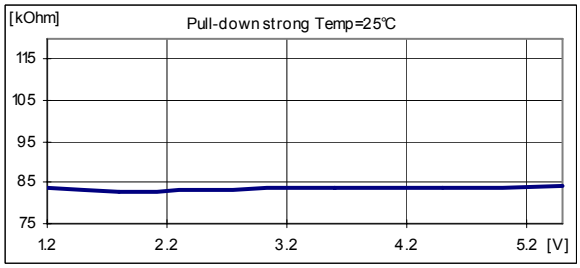


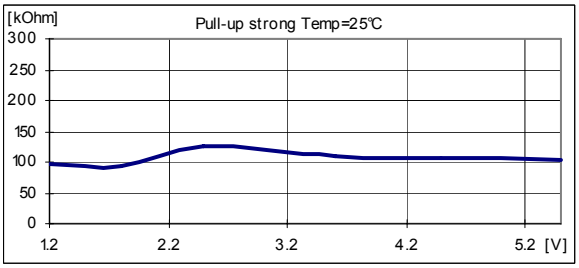
15.2 Voltage

RC frequency



Pulldown, Pullup resistances





16. Electrical Specification

16.1 Absolute Maximum Ratings

	Min.	Max.	Units
Power supply V_{DD}-V_{SS}	- 0.2	+ 5.5	V
Input voltage	V_{SS} – 0.2	V_{DD}+0.2	V
Storage temperature	- 40	+ 125	°C
Electrostatic discharge to Mil-Std-883C method 3015.7 with ref. to V_{SS}	-2000	+2000	V
Maximum soldering conditions for green mold and lead free packages	As per Jedec J-STD-020C		

Stresses above these listed maximum ratings may cause permanent damage to the device.
Exposure beyond specified electrical characteristics may affect device reliability or cause malfunction.

16.2 Handling Procedures

This device has built-in protection against high static voltages or electric fields; however, anti-static precautions should be taken as for any other CMOS component.
Unless otherwise specified, proper operation can only occur when all terminal voltages are kept within the supply voltage range.

16.3 Standard Operating Conditions

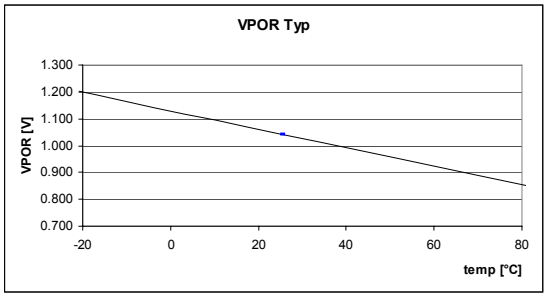
Parameter	MIN	TYP	MAX	Unit	Description
Temperature	-20	25	85	°C	
V_{dd} _Range1	1.4	3.0	5.5	V	with internal voltage regulator
V_{dd} _Range2	0.9	1.5	1.8	V	without internal voltage regulator
I_{vss} max			80	mA	Maximum current out of V_{ss} Pin
I_{vdd} max			80	mA	Maximum current into of V_{dd} Pin
V_{SS}		0		V	Reference terminal
C_{VDDCA} **(note 1)**	100			nF	regulated voltage capacitor
f_{RC}	30		800	kHz	Range of typ. RC frequency

Note 1: This capacitor filters switching noise from V_{dd} to keep it away from the internal logic cells.
In noisy systems the capacitor should be chosen bigger than minimum value.

16.4 DC Characteristics - Power Supply

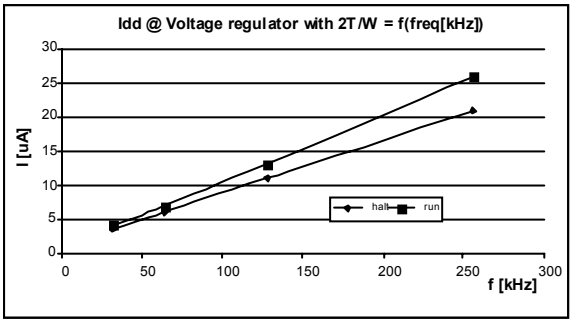
Conditions: V_{dd} =1.5V, T=25°C, RCfreq = 128 kHz .

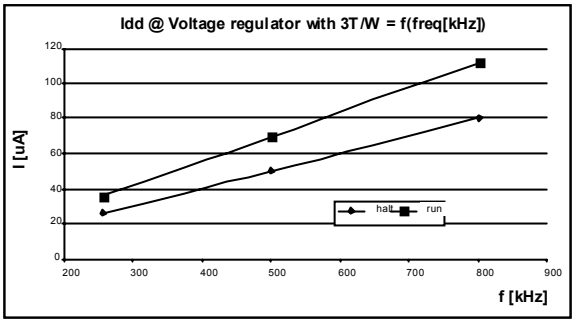
Parameter	Conditions	Symbol	Min.	Typ.	Max.	Unit
ACTIVE Supply Current		I_{VDDa1}		7.7	12	µA
ACTIVE Supply Current	-20 ... 85°C	I_{VDDa1}			12	µA
STANDBY Supply Current		I_{VDDh1}		1.7	3.5	µA
STANDBY Supply Current	-20 ... 85°C	I_{VDDh1}			3.5	µA
SLEEP Supply Current		I_{VDDs1}		0.62	0.8	µA
SLEEP Supply Current	-20 ... 85°C	I_{VDDs1}			2	µA
POR static level	-20 ... 85°C	VPOR		0.7	0.85	V
Power-Check level #5	-20 ... 85°C	VPC5		1.25	1.41	V
Power-Check level #9	-20 ... 85°C	VPC9		1.85	2.09	V
RAM data retention		Vrd1	0.7			V



Conditions: V_{dd} =3.0V, T=25°C, RCfreq = 256 kHz .

Parameter	Conditions	Symbol	Min.	Typ.	Max.	Unit
ACTIVE Supply Current		I_{VDDa2}		20	25	µA
ACTIVE Supply Current	-20 ... 85°C	I_{VDDa2}			30	µA
STANDBY Supply Current		I_{VDDh2}		5.5	9	µA
STANDBY Supply Current	-20 ... 85°C	I_{VDDh2}			10	µA
SLEEP Supply Current		I_{VDDs2}		0.6	0.8	µA
SLEEP Supply Current	-20 ... 85°C	I_{VDDs2}			2	µA
V_{reg}		V_{reg2}		1.67		V





16.5 ADC

ADC levels, here below, are specified with a rising voltage on PA[4].

Conditions: V_{DD}=3.0V, T=25°C, in medium voltage mode with internal voltage regulator (unless otherwise specified)
Devices trimmed

Parameter	Conditions	Symbol	Min.	Typ.	Max.	Unit
Temperature coefficient	0°C to 25°C		-0.046		0.046	%/°C
Temperature coefficient	25°C to 70°C		-0.030		0.030	%/°C
ADC voltage Level0	25°C	V_{VLD0}	0.489	0.515	0.541	V
ADC voltage Level1	25°C	V_{VLD1}	0.619	0.652	0.685	V
ADC voltage Level2	25°C	V_{VLD2}	0.763	0.803	0.843	V
ADC voltage Level3	25°C	V_{VLD3}	0.914	0.962	1.010	V
ADC voltage Level4	25°C	V_{VLD4}	1.074	1.107	1.140	V
ADC voltage Level5	25°C	V_{VLD5}	1.221	1.259	1.297	V
ADC voltage Level6	25°C	V_{VLD6}	1.377	1.420	1.463	V
ADC voltage Level7	25°C	V_{VLD7}	1.504	1.550	1.597	V
ADC voltage Level8	25°C	V_{VLD8}	1.656	1.707	1.758	V
ADC voltage Level9	25°C	V_{VLD9}	1.795	1.851	1.907	V
ADC voltage Level10	25°C	V_{VLD10}	1.946	2.006	2.066	V
ADC voltage Level11	25°C	V_{VLD11}	2.093	2.158	2.223	V
ADC voltage Level12	25°C	V_{VLD12}	2.239	2.308	2.377	V
ADC voltage Level13	25°C	V_{VLD13}	2.392	2.466	2.540	V
ADC voltage Level14	25°C	V_{VLD14}	2.540	2.619	2.698	V
ADC voltage Level15	25°C	V_{VLD15}	2.672	2.755	2.838	V
ADC voltage Level15b*	25°C	V_{VLD15b}	2.955	3.046	3.137	V

Conditions: V_{DD}=1.5V, T=25°C, in low voltage mode without internal voltage regulator (unless otherwise specified)
Devices trimmed

Parameter	Conditions	Symbol	Min.	Typ.	Max.	Unit
Temperature coefficient	0°C to 25°C		-0.046		0.046	%/°C
Temperature coefficient	25°C to 70°C		-0.030		0.030	%/°C
ADC voltage Level0	25°C	V_{VLD0}	0.489	0.515	0.541	V
ADC voltage Level1	25°C	V_{VLD1}	0.619	0.652	0.685	V
ADC voltage Level2	25°C	V_{VLD2}	0.763	0.803	0.843	V
ADC voltage Level3	25°C	V_{VLD3}	0.914	0.962	1.010	V
ADC voltage Level4	25°C	V_{VLD4}	1.074	1.107	1.140	V
ADC voltage Level5	25°C	V_{VLD5}	1.221	1.259	1.297	V
ADC voltage Level6	25°C	V_{VLD6}	1.377	1.420	1.463	V
ADC voltage Level7	25°C	V_{VLD7}	1.504	1.550	1.597	V
ADC voltage Level8	25°C	V_{VLD8}	1.656	1.707	1.758	V
ADC voltage Level9	25°C	V_{VLD9}	1.795	1.851	1.907	V
ADC voltage Level10	25°C	V_{VLD10}	1.946	2.006	2.066	V
ADC voltage Level11	25°C	V_{VLD11}	2.093	2.158	2.223	V
ADC voltage Level12	25°C	V_{VLD12}	2.239	2.308	2.377	V
ADC voltage Level13	25°C	V_{VLD13}	2.392	2.466	2.540	V
ADC voltage Level14	25°C	V_{VLD14}	2.540	2.619	2.698	V
ADC voltage Level15	25°C	V_{VLD15}	2.672	2.755	2.838	V
ADC voltage Level15b*	25°C	V_{VLD15b}	2.955	3.046	3.137	V

16.6 SVLD

SVLD levels, here below, are specified with a rising voltage on VDD.

Conditions: T=25°C, in medium voltage mode with internal voltage regulator (unless otherwise specified)
Devices trimmed

Parameter	Conditions	Symbol	Min.	Typ.	Max.	Unit
Temperature coefficient	0°C to 25°C		-0.046		0.046	%/°C
Temperature coefficient	25°C to 70°C		-0.030		0.030	%/°C
SVLD voltage Level4	25°C	V_{VLD4a}	1.074	1.107	1.140	V
SVLD voltage Level5	25°C	V_{VLD5}	1.221	1.259	1.297	V
SVLD voltage Level6	25°C	V_{VLD6}	1.377	1.420	1.463	V
SVLD voltage Level7	25°C	V_{VLD7}	1.504	1.550	1.597	V
SVLD voltage Level8	25°C	V_{VLD8}	1.656	1.707	1.758	V
SVLD voltage Level9	25°C	V_{VLD9}	1.795	1.851	1.907	V
SVLD voltage Level10	25°C	V_{VLD10}	1.946	2.006	2.066	V
SVLD voltage Level11	25°C	V_{VLD11}	2.093	2.158	2.223	V
SVLD voltage Level12	25°C	V_{VLD12}	2.239	2.308	2.377	V
SVLD voltage Level13	25°C	V_{VLD13}	2.392	2.466	2.540	V
SVLD voltage Level14	25°C	V_{VLD14}	2.540	2.619	2.698	V
SVLD voltage Level15	25°C	V_{VLD15}	2.672	2.755	2.838	V
SVLD voltage Level15b *	25°C	V_{VLD15b}	2.955	3.046	3.137	V

Conditions: T=25°C, in low voltage mode without internal voltage regulator (unless otherwise specified)
Devices trimmed

Parameter	Conditions	Symbol	Min.	Typ.	Max.	Unit
Temperature coefficient	0°C to 25°C		-0.046		0.046	%/°C
Temperature coefficient	25°C to 70°C		-0.030		0.030	%/°C
SVLD voltage Level4	25°C	V_{VLD4a}	1.074	1.107	1.140	V
SVLD voltage Level5	25°C	V_{VLD5}	1.221	1.259	1.297	V
SVLD voltage Level6	25°C	V_{VLD6}	1.377	1.420	1.463	V
SVLD voltage Level7	25°C	V_{VLD7}	1.504	1.550	1.597	V
SVLD voltage Level8	25°C	V_{VLD8}	1.656	1.707	1.758	V
SVLD voltage Level9	25°C	V_{VLD9}	1.795	1.851	1.907	V
SVLD voltage Level10	25°C	V_{VLD10}	1.946	2.006	2.066	V
SVLD voltage Level11	25°C	V_{VLD11}	2.093	2.158	2.223	V
SVLD voltage Level12	25°C	V_{VLD12}	2.239	2.308	2.377	V
SVLD voltage Level13	25°C	V_{VLD13}	2.392	2.466	2.540	V
SVLD voltage Level14	25°C	V_{VLD14}	2.540	2.619	2.698	V
SVLD voltage Level15	25°C	V_{VLD15}	2.672	2.755	2.838	V
SVLD voltage Level15b *	25°C	V_{VLD15b}	2.955	3.046	3.137	V

* SVLD Voltage Level 15 / 15b. For the highest ADC/SVLD level we have a metal option or RegMFP2 Opt[8] where user can select 2.75V typ. or 3.0V typ. This option does not have any influence on other ADC/SVLD levels. See chapter 15.1.5.

16.7 DC characteristics - I/O Pins

Conditions: T= -20 ... 85°C (unless otherwise specified)
V_{dd} =1.5V means; measures without voltage regulator
V_{dd} =3.0V means; measures with voltage regulator

Parameter	Conditions	Symb.	Min.	Typ.	Max.	Unit
Input Low voltage						
Port A[5:0]	V_{dd} < 1.5V	V_{IL}	V_{ss}		0.2 V_{dd}	V
Port A[5:0]	V_{dd} > 1.5V	V_{IL}	V_{ss}		0.3 V_{dd}	V
Input High voltage						
Port A[5:0]		V_{IH}	0.7 V_{dd}		V_{dd}	V
Input Pull-down	V_{dd} =1.5V, Pin at 1.5V, 25°C	R_{PD}	80k	107k	250k	Ω
PA[5:0] **(note 3)** weak	V_{dd} =3.0V, Pin at 3.0V, 25°C	R_{PD}	80k	123k	250k	Ω
Input Pull-up	V_{dd} =1.5V, Pin at 0.0V, 25°C	R_{PU}	300k	440k	900k	Ω
PA[5:0] **(note 3)** weak	V_{dd} =3.0V, Pin at 0.0V, 25°C	R_{PU}	100k	142k	220k	Ω
Input Pull-down	V_{dd} =1.5V, Pin at 1.5V, 25°C	R_{PD}	50k	81k	122k	Ω
PA[5:0] **(note 3)** strong	V_{dd} =3.0V, Pin at 3.0V, 25°C	R_{PD}	50k	81k	122k	Ω
Input Pull-up	V_{dd} =1.5V, Pin at 0.0V, 25°C	R_{PU}	81k	102k	127k	Ω
PA[5:0] **(note 3)** strong	V_{dd} =3.0V, Pin at 0.0V, 25°C	R_{PU}	81k	102k	127k	Ω
Output Low Current	V_{dd} =1.5V , V_{OL}=0.15V	I_{OL}		2.7		mA
PA[5,0]	V_{dd} =1.5V , V_{OL} =0.30V	I_{OL}		4.8		mA
	V_{dd} =1.5V , V_{OL} =0.50V	I_{OL}	4.0	7.3		mA
	V_{dd} =3.0V , V_{OL} =0.15V	I_{OL}		5.5		mA
	V_{dd} =3.0V , V_{OL} =0.30V	I_{OL}		9.9		mA
	V_{dd} =3.0V , V_{OL} =0.50V	I_{OL}	12.0	18.2		mA
	V_{dd} =3.0V , V_{OL} =1.00V	I_{OL}		29.1		mA
Output Low Current	V_{dd} =1.5V , V_{OL} =0.15V	I_{OL}		4.5		mA
PA[2,1]	V_{dd} =1.5V , V_{OL} =0.30V	I_{OL}		8.1		mA
	V_{dd} =1.5V , V_{OL} =0.50V	I_{OL}	7.0	11.5		mA
	V_{dd} =3.0V , V_{OL} =0.15V	I_{OL}		8.1		mA
	V_{dd} =3.0V , V_{OL} =0.30V	I_{OL}		15.8		mA
	V_{dd} =3.0V , V_{OL} =0.50V	I_{OL}	16.0	26.5		mA
	V_{dd} =3.0V , V_{OL} =1.00V	I_{OL}		44.5		mA
Output Low Current	V_{dd} =1.5V , V_{OL} =0.15V	I_{OL}		3.2		mA
PA[3]	V_{dd} =1.5V , V_{OL} =0.30V	I_{OL}		5.7		mA
	V_{dd} =1.5V , V_{OL} =0.50V	I_{OL}	5.4	8.0		mA
	V_{dd} =3.0V , V_{OL} =0.15V	I_{OL}		6.1		mA
	V_{dd} =3.0V , V_{OL} =0.30V	I_{OL}		11.8		mA
	V_{dd} =3.0V , V_{OL} =0.50V	I_{OL}	12.0	19.6		mA
	V_{dd} =3.0V , V_{OL} =1.00V	I_{OL}		32.4		mA

Note 3 : Weak or strong are standing for weak pull or strong pull transistor. Values are for R1=100kΩ

Parameter	Conditions	Symb.	Min.	Typ.	Max.	Unit
Output High Current	V_{dd} =1.5V, V_{OH}= V_{dd} -0.15V	I_{OH}		-1.1		mA
PA[5,0]	V_{dd} =1.5V, V_{OH} = V_{dd} -0.30V	I_{OH}		-1.8		mA
	V_{dd} =1.5V, V_{OH} = V_{dd} -0.50V	I_{OH}		-2.55	-1.5	mA
	V_{dd} =3.0V, V_{OH} = V_{dd} -0.15V	I_{OH}		-2.4		mA
	V_{dd} =3.0V , V_{OH} = V_{dd} -0.30V	I_{OH}		-4.6		mA
	V_{dd} =3.0V , V_{OH} = V_{dd} -0.50V	I_{OH}		-7.6	-2.5	mA
	V_{dd} =3.0V , V_{OH} = V_{dd} -1.00V	I_{OH}		-12.8		mA
Output High Current	V_{dd} =1.5V, V_{OH} = V_{dd} -0.15V	I_{OH}		-2.0		mA
PA[2,1]	V_{dd} =1.5V, V_{OH} = V_{dd} -0.30V	I_{OH}		-3.6		mA
	V_{dd} =1.5V, V_{OH} = V_{dd} -0.50V	I_{OH}		-5.0	-3.0	mA
	V_{dd} =3.0V, V_{OH} = V_{dd} -0.15V	I_{OH}		-4.4		mA
	V_{dd} =3.0V , V_{OH} = V_{dd} -0.30V	I_{OH}		-8.5		mA
	V_{dd} =3.0V , V_{OH} = V_{dd} -0.50V	I_{OH}		-14.7	-6.4	mA
	V_{dd} =3.0V , V_{OH} = V_{dd} -1.00V	I_{OH}		-23.8		mA
Output High Current	V_{dd} =1.5V, V_{OH} = V_{dd} -0.15V	I_{OH}		-1.4		mA
PA[3]	V_{dd} =1.5V, V_{OH} = V_{dd} -0.30V	I_{OH}		-2.4		mA
	V_{dd} =1.5V, V_{OH} = V_{dd} -0.50V	I_{OH}		-3.9	-2.0	mA
	V_{dd} =3.0V, V_{OH} = V_{dd} -0.15V	I_{OH}		-3.1		mA
	V_{dd} =3.0V , V_{OH} = V_{dd} -0.30V	I_{OH}		-5.9		mA
	V_{dd} =3.0V , V_{OH} = V_{dd} -0.50V	I_{OH}		-9.7	-3.2	mA
	V_{dd} =3.0V , V_{OH} = V_{dd} -1.00V	I_{OH}		-16.5		mA

16.8 RC oscillator frequency

Conditions: V_{dd} =3.0V, with internal voltage regulator. V_{dd} =1.5V, without internal voltage regulator. Untrimmed absolute RC frequency.

Parameter	Conditions	Symbol	Min.	Typ.	Max.	Unit
Voltage stability (note 4)	V_{dd} =1.8 – 3.0 V	df/f x dU		0.4	1.0	%/V
Voltage stability (note 5)	V_{dd} =1.4 – 1.6 V	df/f x dU			5.0	%/V
Basic 32 kHz	-20 to 85°C	fb1	-25%	32	+25%	kHz
Basic 32 kHz x 2	-20 to 85°C	fb1x2	-25%	64	+25%	kHz
Basic 32 kHz x 4	-20 to 85°C	fb1x4	-25%	128	+25%	kHz
Basic 32 kHz x 8	-20 to 85°C	fb1x8	-25%	256	+25%	kHz
Basic 32 kHz x 16	-20 to 85°C	fb1x16	-25%	500	+25%	kHz
Basic 50 kHz	-20 to 85°C	fb2	-25%	50	+25%	kHz
Basic 50 kHz x 2	-20 to 85°C	fb2x2	-25%	100	+25%	kHz
Basic 50 kHz x 4	-20 to 85°C	fb2x4	-25%	200	+25%	kHz
Basic 50 kHz x 8	-20 to 85°C	fb2x8	-25%	400	+25%	kHz
Basic 50 kHz x 16	-20 to 85°C	fb2x16	-25%	800	+25%	kHz

Note 4 : Applicable only for the versions with the internal voltage regulator
Note 5 : Applicable only for the versions without the internal voltage regulator.

Conditions: V_{dd} =3.0V, with internal voltage regulator. V_{dd} =1.5V, without internal voltage regulator. Untrimmed absolute RC frequency. T=25°C otherwise specified.

Parameter	Conditions	Symbol	Min.	Typ.	Max.	Unit
Basic 32 kHz	-10 to 70°C	fb1	-10%	32	-10%	kHz
Basic 32 kHz x 2	-10 to 70°C	fb1x2	-10%	64	-10%	kHz
Basic 32 kHz x 4	-10 to 70°C	fb1x4	-10%	128	-10%	kHz
Basic 32 kHz x 4, freq drift 1.5V to 0.9V (low volt.)	25°C	df/f		-6	-14	%
Basic 32 kHz x 8	-10 to 70°C	fb1x8	-10%	256	-10%	kHz
Basic 32 kHz x 16	-10 to 70°C	fb1x16	-10%	500	-10%	kHz
Basic 50 kHz	-10 to 70°C	fb2	-10%	50	-10%	kHz
Basic 50 kHz x 2	-10 to 70°C	fb2x2	-10%	100	-10%	kHz
Basic 50 kHz x 4	-10 to 70°C	fb2x4	-10%	200	-10%	kHz
Basic 50 kHz x 8	-10 to 70°C	fb2x8	-10%	400	-10%	kHz
Basic 50 kHz x 16	-10 to 70°C	fb2x16	-10%	800	-10%	kHz
Oscillator start voltage	Tstart < 10 ms	Ustart	V_{DDmin}			V
Oscillator start time	$V_{dd} > V_{DDMin}$	tdosc		0.1	5.0	ms
System start time (oscillator + cold-start + reset)	$V_{dd} > V_{DDMin}$	tdsys		0.5	6.0	ms

16.9 Sleep Counter Reset - SCR

Conditions: V_{dd} =3.0V, with internal voltage regulator. V_{dd} =1.5V, without internal voltage regulator.

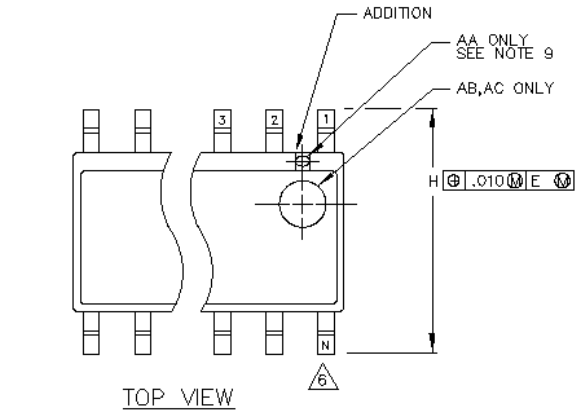
Parameter	Conditions	Symbol	Min.	Typ.	Max.	Unit
SCR timeout 0	-20 to 85°C	tSCR00		13		ms
SCR timeout 1	-20 to 85°C	tSCR01		130		ms
SCR timeout of 2	-20 to 85°C	tSCR10		1.1		s
SCR timeout of 3	-20 to 85°C	tSCR11		8.8		s

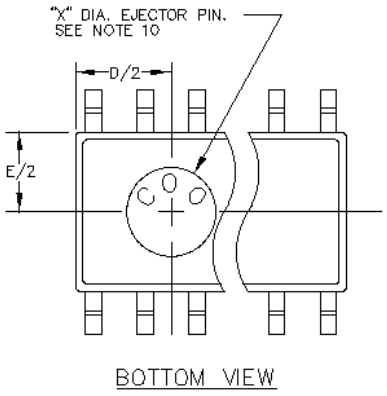
17. Die, Pad Location and Size

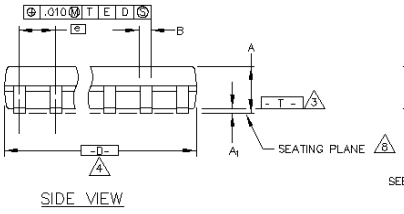
Information upon request to EM Microelectronic-Marin S.A.

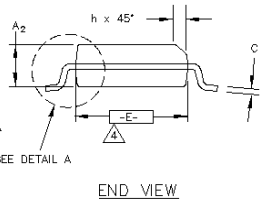
18. Package Dimensions

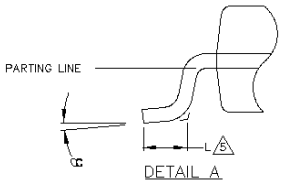
18.1 SO-8/14











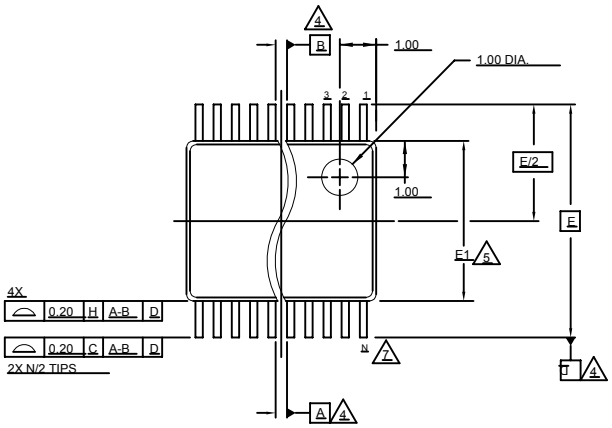
NOTES:

1. MAXIMUM DIE THICKNESS ALLOWABLE IS .015.
2. DIMENSIONING & TOLERANCES PER ANSI.Y14.5M - 1982.
3. "T" IS A REFERENCE DATUM.
4. "D" & "E" ARE REFERENCE DATUMS AND DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS, BUT DOES INCLUDE MOLD MISMATCH AND ARE MEASURED AT THE MOLD PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.006 INCHES AT END AND .010 INCHES AT WINDOW
5. "L" IS THE LENGTH OF TERMINAL FOR SOLDERING TO A SUBSTRATE.
6. "N" IS THE NUMBER OF TERMINAL POSITIONS.
7. TERMINAL POSITIONS ARE SHOWN FOR REFERENCE ONLY.
8. FORMED LEADS SHALL BE PLANAR WITH RESPECT TO ONE ANOTHER WITHIN .003 INCHES AT SEATING PLANE.
9. THE APPEARANCE OF PIN #1 I.D ON THE 8 LD IS OPTIONAL, ROUND TYPE ON SINGLE LEADFRAME AND RECTANGULAR TYPE ON MATRIX LEADFRAME.
10. COUNTRY OF ORIGIN LOCATION ON PACKAGE BOTTOM IS OPTIONAL AND DEPENDS ON ASSEMBLY LOCATION.
11. CONTROLLING DIMENSION: INCHES.
12. THIS PART IS COMPLIANT WITH JEDEC STANDARD MS-012, VARIATION AA, AB & AC.

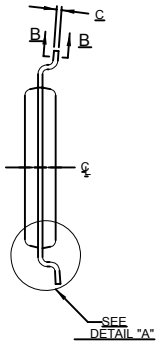
THIS TABLE IN MILLIMETERS

SYMBOL	COMMON DIMENSIONS			NOTE	NOTE	3			5
					VARI-	D			N
	MIN.	NOM.	MAX.		ATIONS	MIN.	NOM.	MAX.	
A	1.55	1.63	1.73		AA	4.80	4.93	4.98	8
A_1	0.127	0.15	0.25		AB	8.58	8.69	8.74	14
A_2	1.40	1.47	1.55		AC	9.80	9.93	9.98	16
B	0.35	0.41	0.49						
C	0.19	0.20	0.25						
D	SEE VARIATIONS			3					
E	3.81	3.94	3.99						
e	1.27 BSC								
H	5.84	5.99	6.20						
h	0.25	0.33	0.41						
L	0.41	0.64	0.89						
N	SEE VARIATIONS			5					
α	0°	5°	8°						
X	2.16	2.36	2.54						

18.2 TSSOP-8/14



TOP VIEW



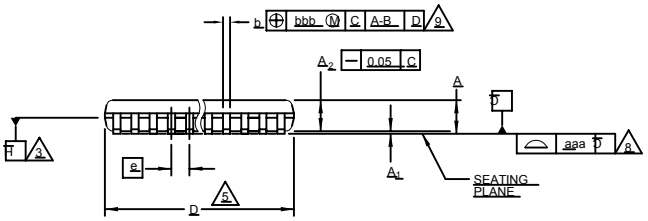
END VIEW

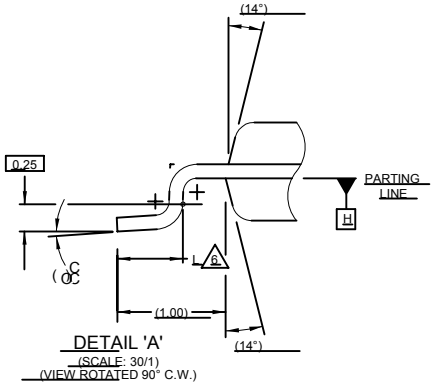
THIS TABLE FOR 0.65mm PITCH

SYMBOL	COMMON DIMENSIONS MIN.	NOM.	MAX.	NOTE
A	—	—	1.10	
A_1	0.05	—	0.15	
A_2	0.85	0.90	0.95	
aaa		0.076		
b	0.19	-	0.30	9
b1	0.19	0.22	0.25	
bbb		0.10		
c	0.09	-	0.20	
c1	0.09	0.127	0.16	
D	SEE VARIATIONS			5
E1	4.30	4.40	4.50	5
e		0.65 BSC		
E		6.40 BSC		
L	0.50	0.60	0.70	6
N	SEE VARIATIONS			7
P	SEE VARIATIONS			13
P1	SEE VARIATIONS			13
θ	0°	—	8°	

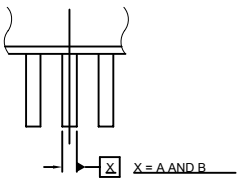
NOTE VARIATIONS	5 D	P MAX.	P1 MAX.	7 N
AA/AAT	3.00 BSC	2.2	3.2	8
AB-1/ABT	5.00 BSC	3.1	3.0	14
AB/ABT	5.00 BSC	3.0	3.0	16
AC/ACT	6.50 BSC	4.2	3.0	20
AD/ADT	7.80 BSC	5.5	3.0	24
AE/AET	9.70 BSC	5.5	3.0	28

- DESIGNED BUT NOT TOOLED

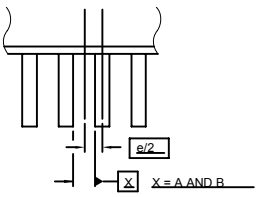




DETAIL 'A'
(SCALE: 30/1)
(VIEW ROTATED 90° C.W.)



ODD LEAD SIDES
TOPVIEW



EVEN LEAD SIDES
TOPVIEW

19. Ordering Information

Packaged Device:

EM6682 SO8 A - %%%

Package:
SO8 = 8 pin SOIC
TP8 = 8 pin TSSOP
DL8 = 8 pin DIP (note 1)
SO14 = 14 pin SOIC
TP14 = 14 pin TSSOP

Delivery Form:
A = Stick
B = Tape&Reel (for SO8 and TP8 only)

Customer Version:
customer-specific number
given by EM Microelectronic

Device in DIE Form:

EM6682 WS 11 - %%%

Die form:
WW = Wafer
WS = Sawn Wafer/Frame
WP = Waffle Pack

Thickness:
11 = 11 mils (280um), by default
27 = 27 mils (686um), not backlapped
(for other thickness, contact EM)

Customer Version:
customer-specific number
given by EM Microelectronic

Note 1: Please contact EM Microelectronic-Marin S.A. for availability of DIP package for engineering samples. In its package form, EM6682 is available in Green mold / lead free.

Ordering Part Number (selected examples)

Part Number	Package/Die Form	Delivery Form/ Thickness
EM6682SO8A-%%% +	8 pin SOIC	Stick
EM6682SO8B-%%% +	8 pin SOIC	Tape&Reel
EM6682SO14A-%%% +	14 pin SOIC	Stick
EM6682TP8A-%%%	8 pin TSSOP	Stick
EM6682TP8B-%%%	8 pin TSSOP	Tape&Reel
EM6682WS11-%%%	Sawn wafer	11 mils
EM6682WP11-%%%	Die in waffle pack	11 mils

Please make sure to give the complete Part Number when ordering, including the 3-digit customer version. The customer version is made of 3 numbers %%% (e.g. 008 , 012, 131, etc.)

19.1 Package Marking

8-pin SOIC marking:

First line:	6	6	8	2	%	%	%
Second line:	P	P	P	P	P	P	P
Third line:			C	C	C	Y	P

8-pin TSSOP marking:

	6	6	8	2
%	%	%	C	P

14-pin SOIC marking:

First line:	E	M	6	6	8	2	%	%
Second line:	P	P	P	P	P	P	P	P
Third line:	C	C	C	C	C	C	Y	P

14-pin TSSOP marking:

6	6	8	2	%	%	
P	P	P	P	P	P	
		P	P	P	Y	

Where: %%% or %% = customer version, specific number given by EM (e.g. 008, 012, 131, etc.)
PP…P = Production identification (date & lot number) of EM Microelectronic
Y = year of assembly
CC…C = Customer specific package marking on third line, selected by customer

19.2 Customer Marking

There are **3** digits available for customer marking on **SO8, 1** for **TSSOP8, 6** for **SO14** and **0** for **TSSOP14.**

Please specify the desired customer marking:
