SIEMENS

SDA 2112-2
TV PLL for 125 kHz Resolution

The SDA 2112-2 is fabricated in ASBC technology. In connection with a VCO (tuner) and a high-speed 1:64 divider, it forms a digitally programmable phase-locked loop for TV sets designed to use the PLL frequency sythesis tuning principle. The PLL enables crystal-controlled setting of the tuner oscillator frequency for a 125 kHz resolution in the frequency bands I/III, IV, and V.

A serial interface provides for simple connection to a microprocessor. The latter loads the programmable divider and the band-selection outputs with the appropriate information.

Features

- No external integrator necessary
- Internal buffer
- Microprocessor compatible

Maximum ratings

Supply voltage pin 18	V_{S1}	−0.3 to 7.5	V
Inputs			
Q 1, Q 2, F, $\overline{F}$ pin 1, 2, 15, 16	V_I	−0.3 to V_{S1} + 0.2	V
CPL, IFO, PLE pin 7, 8, 10	V_I	−0.3 to 5.5	V
Outputs			
UHF, VHF, Bd I/III pin 3, 4, 5	V_Q	−0.3 to 16	V
CLK (pin 6)	V_6	−0.3 to 16	V
	I_6	3	mA
$\overline{LDM}$ (pin 17)	V_{17}	−0.3 to 7.5	V
	I_{17}	3	mA
LOCK IND (pin 12)	V_{12}	−0.3 to V_{S1} + 0.2	V
PD (pin 14)	I_{14}	1	mA
V_D (pin 11)	V_{11}	−0.3 to 33	V
OSC (pin 13)	V_{13}	−0.3 to V_{S1} + 0.2	V
	I_{13}	8	mA
Junction temperature	T_j	140	°C
Storage temperature range	T_{stg}	−40 to 125	°C
Thermal resistance (system-air)	$R_{th\,SA}$	80	K/W

Operating range

Supply voltage range	V_{S1}	4.5 to 7.15	V
Input frequency	$f_{F,\overline{F}}$	16	MHz
Divider factor	N	256 to 8191	
Crystal frequency	f_Q	3	MHz
Tuning voltage	V_D	0.3 to 33	V
Ambient temperature	T_A	0 to 70	°C

Characteristics

$V_{S1} = 5$ V; $T_A = 25$ °C

		Test circuit	min	typ	max	
Supply current, pin 18	I_{S1}			20	35	mA
Oscillator output, pin 13	V_{13H}	4	4.5			V
$R_{L2} = 3.5$ kΩ						
OSC	V_{13L}	4			0.7	V
$R_{L2} = 3.5$ kΩ						
Signal inputs F/$\bar{F}$, pin 15, 16						
Input voltage	V_{15H}	1	4.1		$V_{S1}+0.2$	V
	V_{15L}	1	3.8		$V_{S1}-0.1$	V
Input current	I_{15}	1			50	µA
$V_{15} = 5$ V						
Input sensitivity (peak-to-peak)	$V_{15,16}$	1	300		1200	mV
Sine push-pull $f = 16$ MHz						
Bus inputs CPL, IFO, PLE, pin 7, 8, 10						
Upper threshold voltage	V_{7u}	2	1.0	1.3	1.6	V
Lower threshold voltage	V_{7l}	2	0.5	0.7	1.0	V
Hysteresis	ΔV_7	2		0.6		V
H input current	I_{7H}	2			8	µA
$V_{7H} = 5$ V						
L input current	I_{7L}	2	−50			µA
$V_{7L} = 0.4$ V						
Band selection outputs UHF, VHF, Bd I/III pins 3, 4, 5						
Reverse current	I_{3H}	3			10	µA
$V_{3H} = 15$ V						
Forward current (current drain)	I_{3L}	3	0.8		1.7	mA
$2V \leq V_3 \leq 15$ V						
Clock output CLK, pin 6						
H output voltage	V_{6H}	4	14			V
$V_{S3} = 15$ V						
L output voltage	V_{6L}	4			1.5	V
$R_{L1} = 6.8$ kΩ						
Tuning section V_D, PD, pins 11, 14						
Tuning voltage	V_{11}	5	0.3		32.5	V
$V_{S2} = 33$ V						
Charge-pump current	I_{14}	5	−150	±100	150	µA
PLL locked						
PLL unlocked	I_{14}	5	−450	±300	450	µA

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Characteristics (cont'd)
$V_{S1} = 15$ V; $T_A = 25$ °C

		Test circuit	min	typ	max	
Lock indication, pin 12						
H output voltage	$V_{12\,H}$	5	2.8			V
L output voltage	$V_{12\,L}$	5			0.4	V
Carry synchronous divider $\overline{\text{LDM}}$ Pin 17 (open collector)						
Reverse current $V_{17\,H} = 5$ V	I_{17}	1			10	µA
L output voltage $R_L = 5$ kΩ	$V_{17\,L}$				0.4	V
Switching times						
IFO, PLE						
Set-up time	t_S	2	2	1.5		µs
Hold time	t_H	2	2	1.5		µs
CLK						
H pulse width	t_{TH}	4		8.0		µs
L pulse width	t_{TL}	4		8.0		µs
HL transition time $R_{L1} = 6.8$ kΩ	t_{THL}	4	0		0.5	µs
LH transition time $C_{L1} = 50$ pF	t_{TLH}		0		1.5	µs
CPL						
H pulse width	t_{CH}	2	2	1.5		µs
L pulse width	t_{CLH}	2	2	1.5		µs
OSC						
H pulse width	t_{OH}	4	133			ns
L pulse width	t_{OL}	4			200	ns
HL transition time $R_{L2} = 3.5$ kΩ	t_{OHL}	4			20	ns
LH transition time $C_{L2} = 8$ pF	t_{OLH}	4			50	ns

Circuit description (refer to block diagram)

F, $\overline{F}$ A switchable 16/17 counter is triggered by the ECL signal inputs F/$\overline{F}$. The counter, in connection with a 4-bit and a 9-bit programmable, synchronous counter, forms a programmable, 13-bit synchronous divider using the dual-modulus technique, the 4-bit counter controlling the switchover from 16 to 17. Divider ratios of N = 256 to 8191 are possible. For test purposes the carry of the synchronous

$\overline{LDM}$ divider is available at the $\overline{LDM}$ output (open collector).

The 16-bit shift register and latch is subdivided into 13 bits for storing the divider

IFO ratio N and 3 bits for controlling the three band-selection outputs.

CPL The telegram is shifted in via the serial data input IFO with the HL edge of the

PLE shift clock CPL when the enable input PLE is also on high level. First the complement of the divider ratio N, beginning with the LSB, is inserted in binary code, followed by the three control bits for the band-selection switching (see truth table). The 16-bit latch takes the data from the shift register when the enable input PLE is on low level.

Q1, Q2 The IC includes a crystal-controlled, 3-MHz clock oscillator. The output signal is divided down to 1.953125 kHz (reference signal) by a 1/1536 reference divider.

OSC The oscillator frequency appears at the TTL output OSC.

CLK The clock of 62.5 kHz is available at the open-collector output CLK.

PD The divided input signal is compared with the reference signal in a digital phase detector. If the falling edge of the input signal appears prior to the falling edge of the reference signal, the DOWN output of the phase detector turns to high level for the duration of this phase difference. In the reverse case the UP output turns to high level. If the two signals are in phase, both outputs remain at low level. The UP/DOWN outputs control the two current sources I^+ und I^- (charge pump). If the two outputs are low (PLL locked), the charge-pump output PD will turn to the high-impedance state (TRISTATE).

LOCK An L signal appears at the LOCK IND output if frequency and phase are

IND synchronous. The current sources I^+ and I^- are then reduced from 300 to 100 µA.

V_D The current pulses generated by the charge pump are integrated to form the tuning voltage by means of an active lowpass filter (external pull-up resistor to supply V_{S2} and external RC circuitry). The dc output signal appears at V_D and serves as a tuning voltage for the VCO.

UHF The band-selection outputs (UHF, VHF, Bd I/III) contain current drains with open

VHF collectors. In this way PNP transistors working as band-selection switches can be

Bd I/III connected directly without current-limiting resistors (see application circuit).

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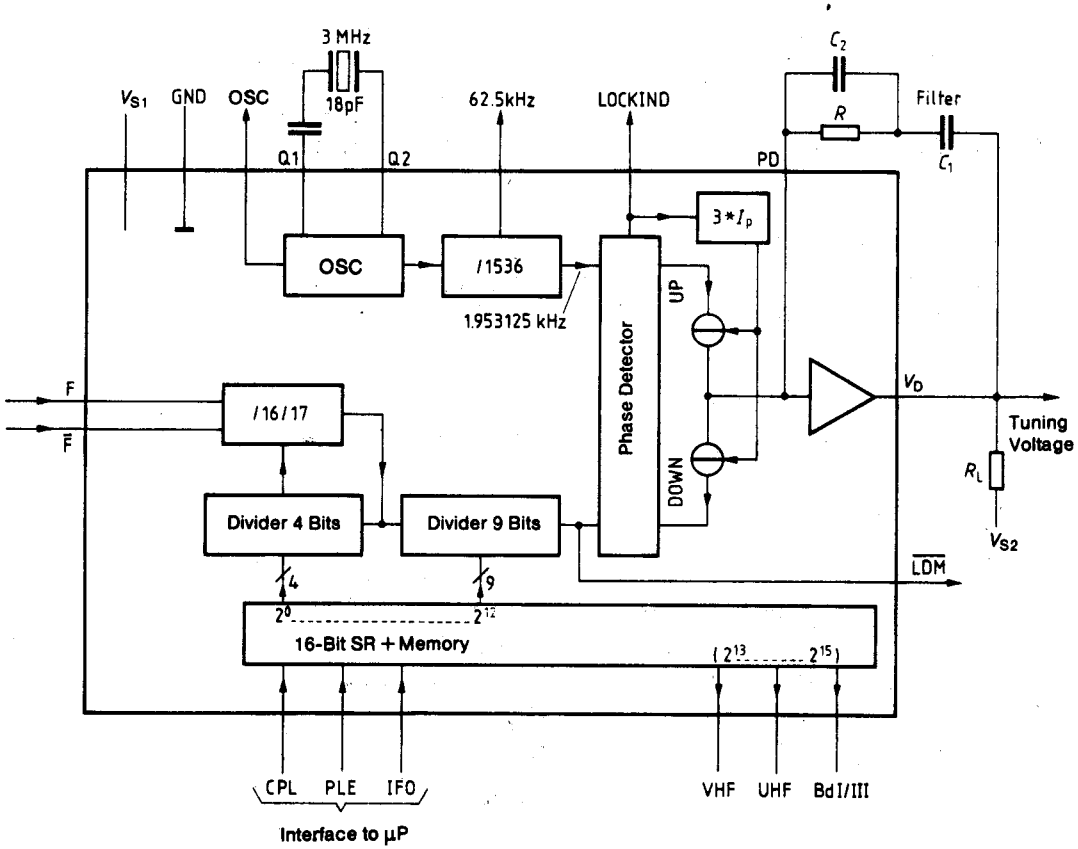
Pin description

Pin	Symbol	Function
1	Q 2	Crystal
2	Q 1	Crystal
3	UHF	} Band selection outputs
4	VHF	
5	Bd I/III	
6	CLK	Clock output
7	CPL	Clock input
8	IFO	Data input
9	GND	Ground
10	PLE	Shift register enable input
11	V_D	Tuning voltage
12	LOCK IND	Lock indication output
13	OSC	Oscillator output
14	V_{PD}	Phase detector voltage
15	$\overline{F}$	Inverted input
16	F	Input
17	$\overline{LDM}$	Carry
18	V_{S1}	Supply voltage

Block diagram



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Computation for loop filter

Loop bandwidth: $\omega_R = \sqrt{\frac{I_p \times K_{VCO}}{C_1 \times P \times N}}$

Attenuation: $\xi = 0.5 \times \omega_R \times R \times C_1$

P = Prescaler
N = Programmable divider
I_p = Pump current
K_{VCO} = Tuner slope
R, C_1 = Loop filter

Example for channel 47:

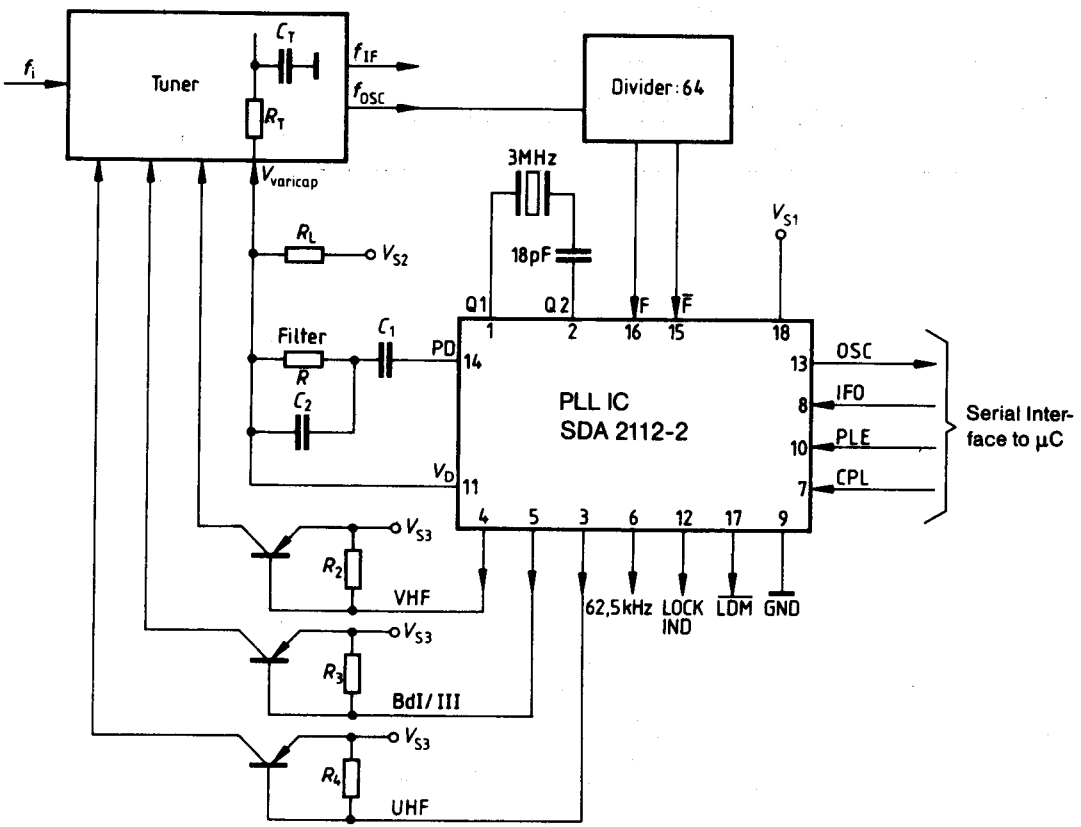
$P = 64$; $N = 5760$; $I_p = 100\ \mu A$; $K_{VCO} = 18.7$ MHz/V; $R = 33\ k\Omega$
$C_1 = 330$ nF; $\omega_R = 124$ Hz; $f_n = 20$ Hz; $\xi = 0.675$

Post filter: $R_t = 10\ k\Omega$; $C_t = 47$ nF

Standard dimensioning: $C_2 = C_{1/5}$

$V_{S1} = 5$ V; $V_{S2} = 33$ V; $V_{S3} = 12$ V; R_2 to $R_4 = 22\ k\Omega$; $R_L = 22\ k\Omega$

Application circuit

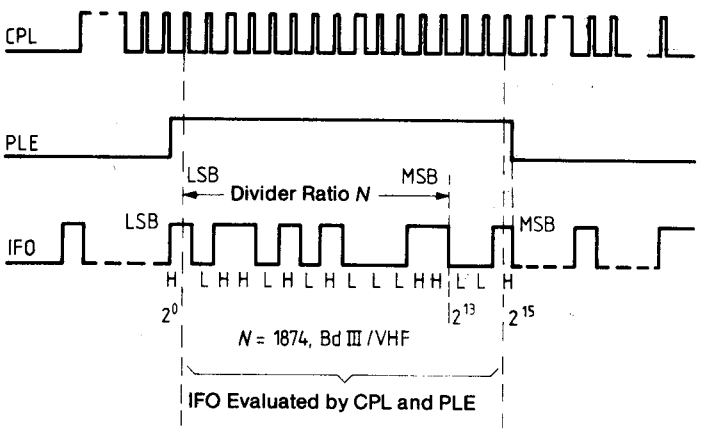


Truth table

Input "IFO" bit			Outputs			Meaning
2^{13}	2^{14}	2^{15}	Bd I/III	VHF	UHF	
H	H	L	H	H	L	"UHF"
H	L	H	H	L	H	"Bd I/VHF"
L	L	H	L	L	H	"Bd III/VHF"
L	H	H	L	H	H	"Bd III/VHF"

At positive logic, the "IFO" bits $2^0 \ldots 2^{12}$ complement the dual code from divider ratio *N*.

Pulse diagram



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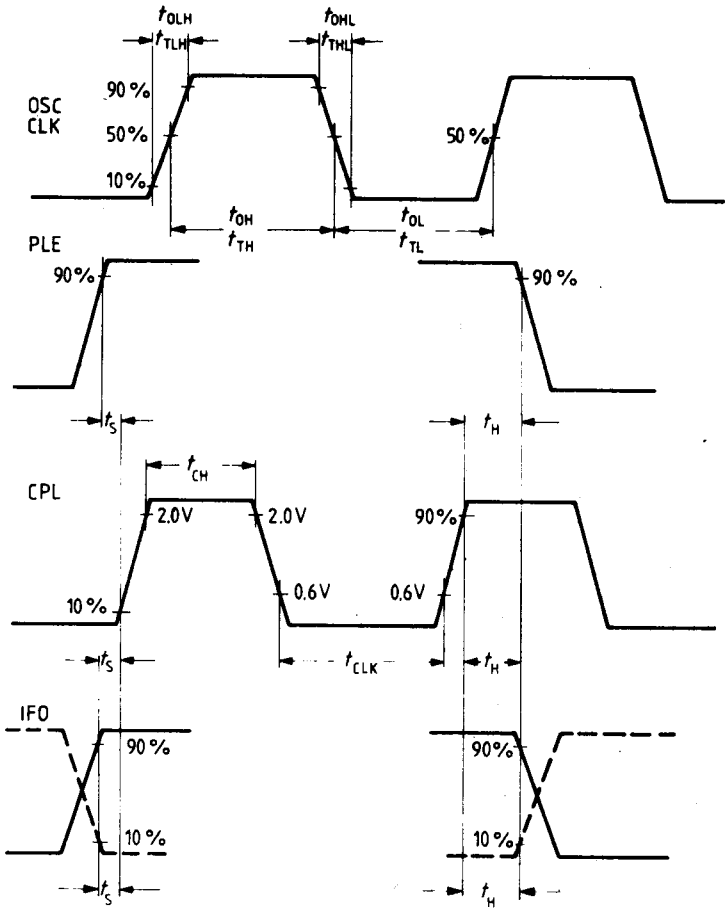
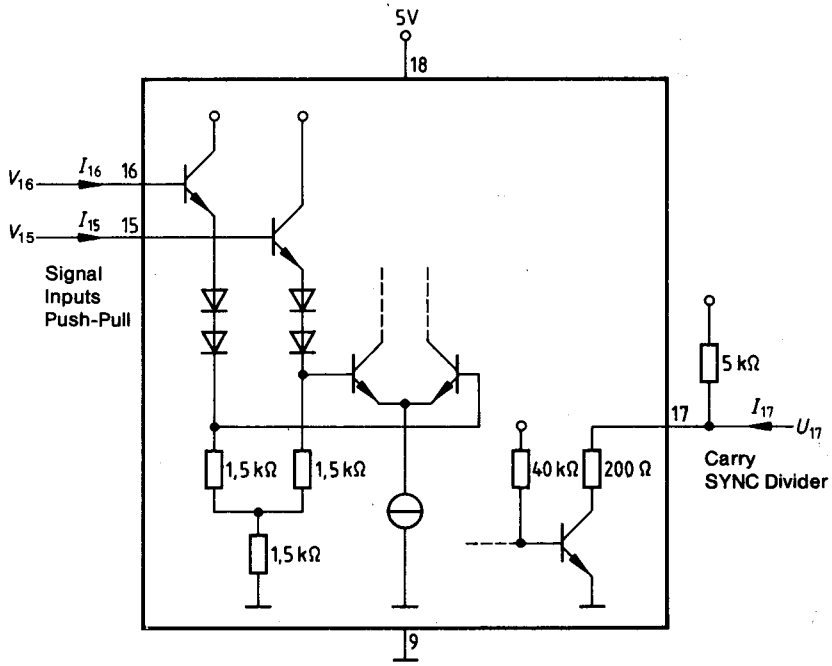
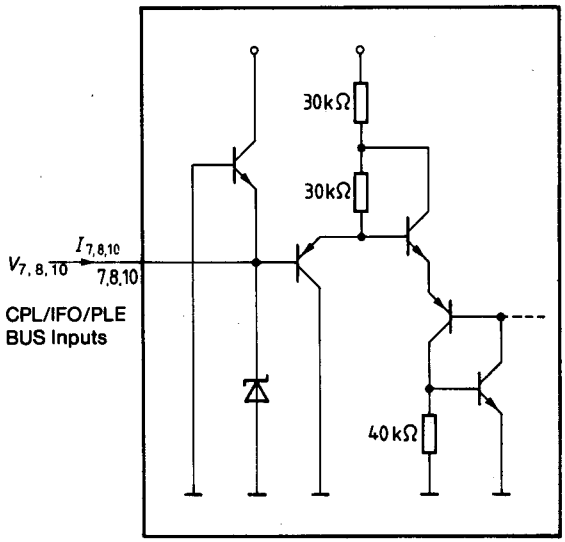
Pulse diagram



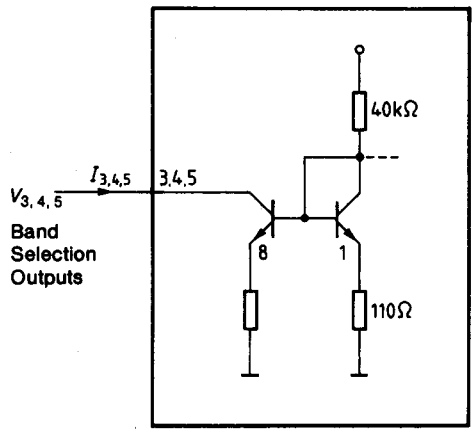
Test and measurement circuits



Test circuit 1

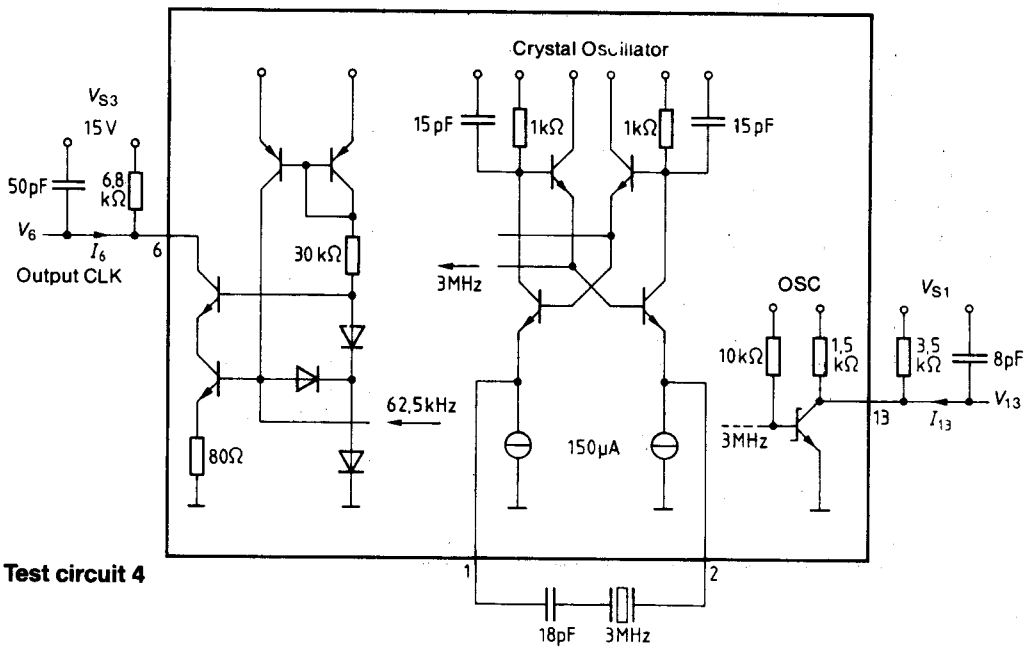


Test circuit 2

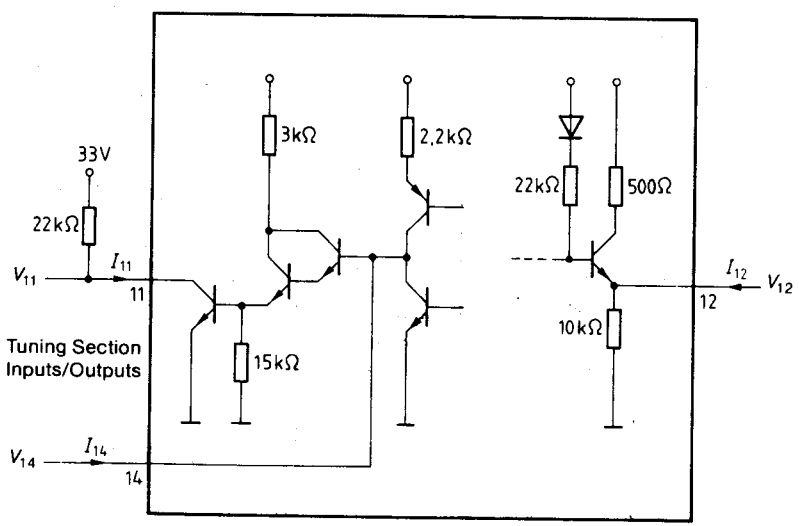


Test circuit 3

Test and measurement circuits



Test circuit 4



Test circuit 5