SIO1049

Super I/O with LPC Interface, with IrDA and Microsoft® Windows® MCE Consumer IR Support

PRODUCT FEATURES

Data Brief

- 3.3 Volt Operation (5V Tolerant)
- Programmable Wakeup Event Interface (IO_PME# Pin)
- SMI Support (IO_SMI# Pin)
- GPIOs (14)
- Two IRQ Input Pins
- XNOR Chain
- PC99a, PC2001
- ACPI 2.0 Compliant
- 64-pin STQFP Package
- Intelligent Auto Power Management
- Serial Ports
  - One Full Function Serial Port
  - High Speed 16C550A Compatible UART with Send/Receive 16-Byte FIFO
  - Supports 230k and 460k Baud
  - Programmable Baud Rate Generator
  - Modem Control Circuitry
- Infrared Communications Controllers
  - Two IR Ports
  - Multi-Protocol Serial Communications Controllers
  - One IrDA v1.2 (4Mbps), HPSIR, ASKIR, Consumer IR Support
  - One Consumer IR Port (CIRCC3) with Support for NEC PPM, Phillips RC5 and Microsoft CIR Protocols, and PME Wake-up Option; New Capability to Capture Carrier Frequency for Learn Mode
  - 4-Channel IR Emitter Transmit Capability (BIRCC)
  - Multiple Base I/O Address Options, 15 IRQ Options and 3 DMA Options
- Multi-Mode Parallel Port with ChiProtect™
  - Standard Mode IBM PC/XT®, PC/AT®, and PS/2™ Compatible Bidirectional Parallel Port
  - Enhanced Parallel Port (EPP) Compatible - EPP 1.7 and EPP 1.9 (IEEE 1284 Compliant)
  - IEEE 1284 Compliant Enhanced Capabilities Port (ECP)
  - ChiProtect Circuitry for Protection Against Damage Due to Printer Power-On
  - 192 Base I/O Address, 15 IRQ and 3 DMA Options
- LPC Bus Host Interface
  - Multiplexed Command, Address and Data Bus
  - 8-Bit I/O Transfers
  - 8-Bit DMA Transfers
  - 16-Bit Address Qualification
  - Serial IRQ Interface Compatible with Serialized IRQ Support for PCI Systems
  - PCI CLKRUN# Support
  - Power Management Event (IO_PME#) Interface Pin

ORDER NUMBER: SIO1049-JV FOR 64 PIN, STQN (STQFP ROHS COMPLIANT) PACKAGE

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General Description

The SMSC SIO1049 is a 3.3V PC 99, PC2001, and ACPI 2.0 compliant Super I/O Controller. The SIO1049 implements the LPC interface, a pin reduced ISA interface which provides the same or better performance as the ISA/X-bus with a substantial savings in pins used. The part also includes 14 GPIO pins.

The SIO1049 incorporates a 16C550A compatible UART and one Multi-Mode parallel port with ChiProtect™ circuitry plus EPP and ECP support. The SIO1049 does not require any external filter components, is easy to use and offers lower system cost and reduced board area.

The SIO1049 offers a full 16-bit internally decoded address bus, a Serial IRQ interface with PCI CLKRUN# support, relocatable configuration ports, and three DMA channel options.

The on-chip UART is compatible with the 16C550A. There is a dedicated Serial Infrared interface UART, which complies with IrDA v1.2 (Fast IR), HPSIR, and ASKIR formats (used by Sharp and other PDAs), as well as Consumer IR. There is a second IR port, which supports NEC, Phillips RC5 and Microsoft CIR protocols for waking from any Sleep level, as well as other Consumer IR protocols for normal data transfer, and is enhanced to allow measurement of an incoming carrier. In addition a third block (BIRCC: “Blaster” IR Communication Controller) is provided in order to be able to transmit control on up to four IR Emitter channels.

The parallel port is compatible with IBM PC/AT architectures, as well as IEEE 1284 EPP and ECP. The parallel port ChiProtect™ circuitry prevents damage caused by an attached powered printer when the SIO1049 is not powered.

The SIO1049 features Software Configurable Logic (SCL) for ease of use. SCL allows programmable system configuration of key functions such as the parallel port and UART.

The SIO1049 supports the ISA Plug-and-Play Standard register set (Version 1.0a) and provides the recommended functionality to support Windows operating systems, PC99, and PC2001. The I/O Address, DMA Channel, and Hardware IRQ of each device in the SIO1049 may be reprogrammed through the internal configuration registers. There are multiple I/O address location options, a Serialized IRQ interface, and three DMA channels.

Block Diagram

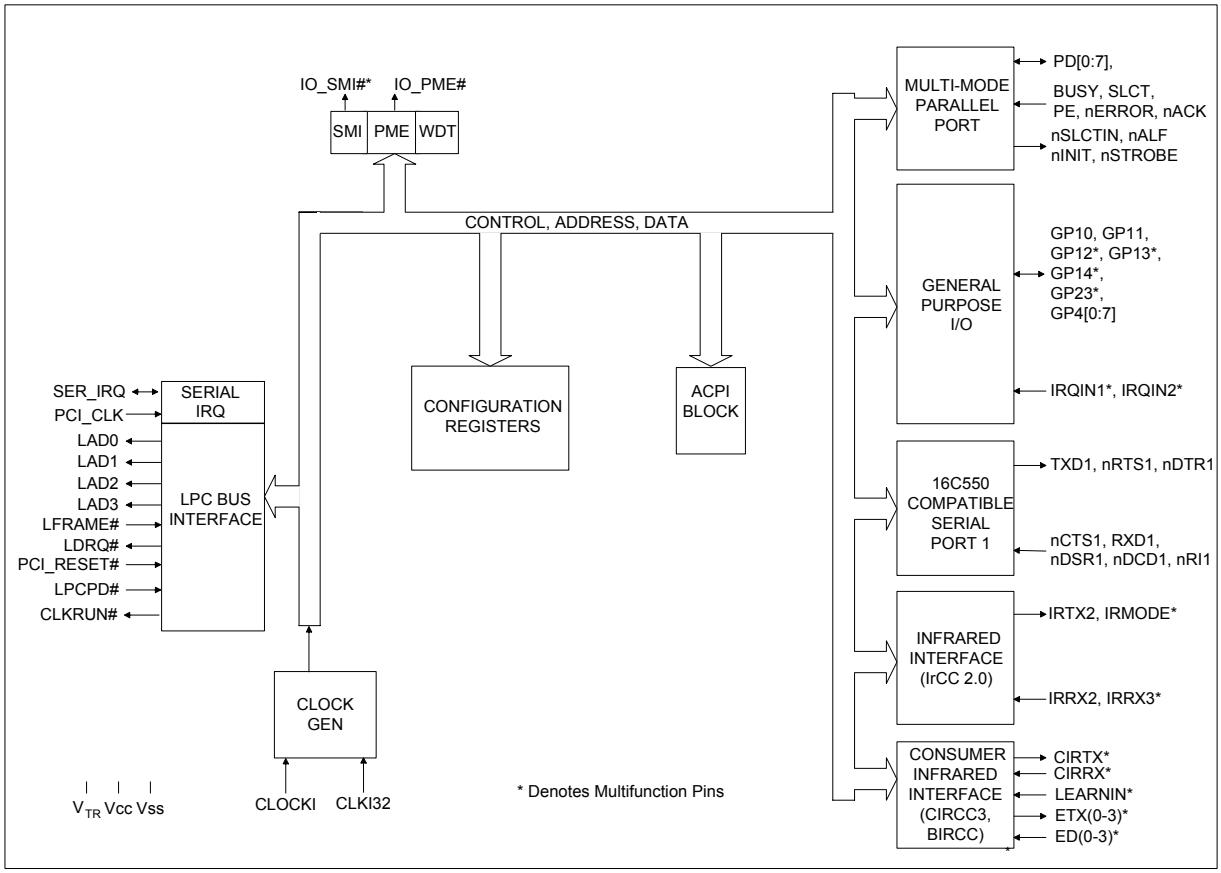

Figure 1 SIO1049 Block Diagram

PRODUCT PREVIEW

Pin Configuration

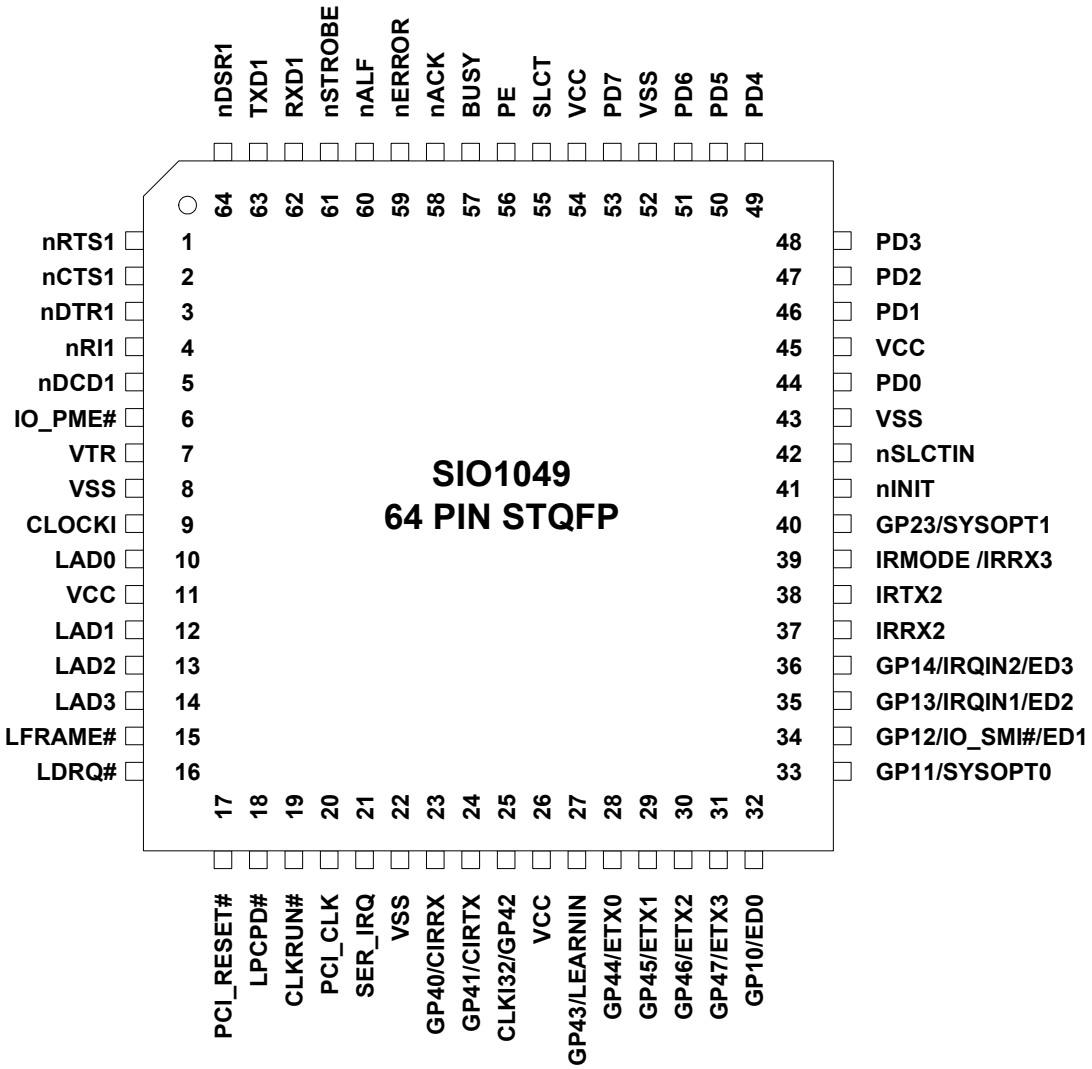

Figure 2 SIO1049 Pin Diagram

Package Outline

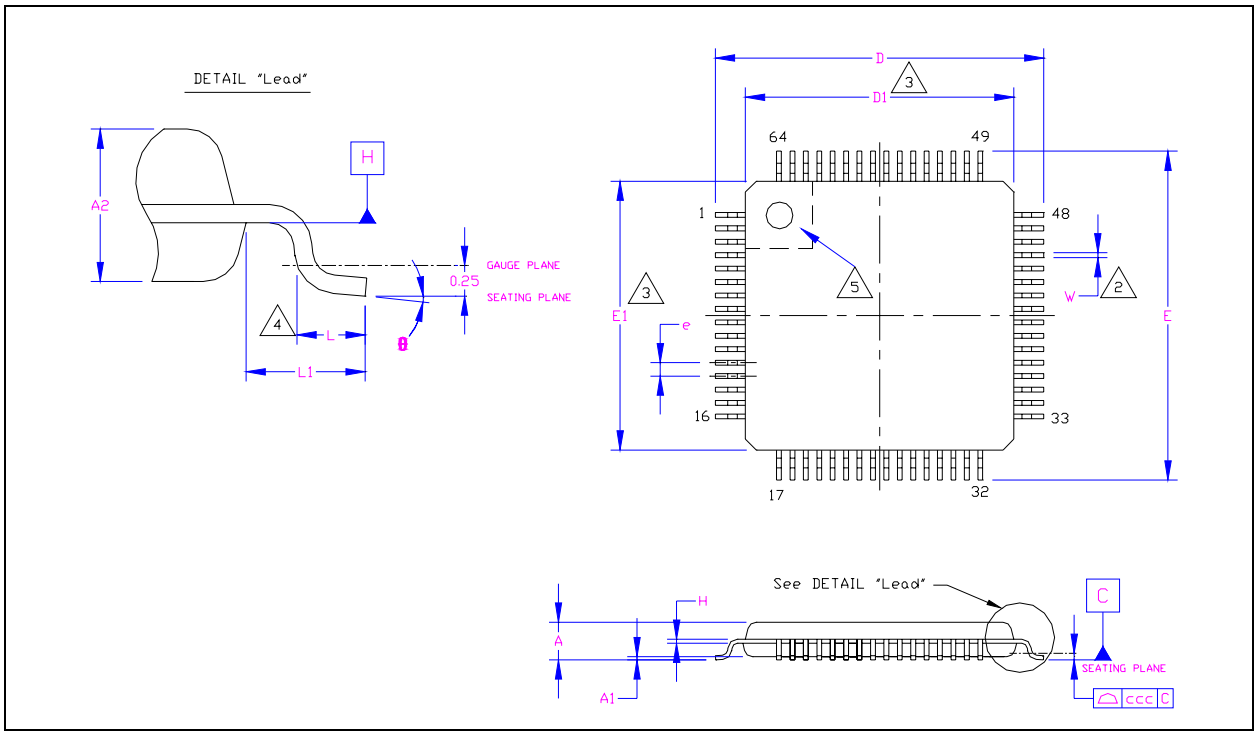

Figure 3 64 Pin STQFP Package Outline, 7X7X1.4 Body, 2 MM Footprint

Table 1 64 Pin STQFP Package Parameters

	MIN	NOMINAL	MAX	REMARKS
A	~	~	1.60	Overall Package Height
A1	0.05	~	0.15	Standoff
A2	1.35	1.40	1.45	Body Thickness
D	8.80	9.00	9.20	X Span
D1	6.80	7.00	7.20	X body Size
E	8.80	9.00	9.20	Y Span
E1	6.80	7.00	7.20	Y body Size
H	0.09	~	0.20	Lead Frame Thickness
L	0.45	0.60	0.75	Lead Foot Length
L1	~	1.00 REF.	~	Lead Length
e		0.40 Basic		Lead Pitch
	0^o	~	7^o	Lead Foot Angle
W	0.13	0.18	0.23	Lead Width
ccc	~	~	0.08	Coplanarity

Notes:
1. Controlling Unit: millimeter.
2. Tolerance on the true position of the leads is ± 0.035 mm maximum.
3. Package body dimensions D1 and E1 do not include the mold protrusion. Maximum mold protrusion is 0.25 mm per side. D1 and E1 dimensions determined at datum plane H.
4. Dimension for foot length L measured at the gauge plane 0.25 mm above the seating plane.
5. Details of pin 1 identifier are optional but must be located within the zone indicated.