Digitally Programmable 2, 4 and 8 Mux LCD Driver

Description

The V6116 is a universal low multiplex LCD driver. The 2, 4 and 8 way multiplex is digitally programmable by the command byte. The display refresh is handled on chip via 2 selectable 8 x 40 RAMs which holds the LCD content driven by the driver. LCD pixels (or segments) are addressed on a one to one basis with the 8 x 40 bit RAM (a set bit corresponds to an activated LCD pixel). Due to the very low driver impedance, the V6116 is designed to be proved in large pixel size applications. Using the TAB tools, the V6116 can be easily cascaded and it can be provided in very large display applications by using the column only driver command $\overline{COL}$. The very low current consumption, the extremely large voltage range and the extremely wide temperature range give the V6116 a real advantage for a wide range of applications.

Versions

- V6116 060 with internal bias resistor
- V6116 020 without internal bias resistor
- When using the version 020 (without internal bias resistor) in mux mode 4, V3 has to be connected to V_{SS}

Features

- V6116 mux mode 2 with 2 rows and 38 columns
- V6116 mux mode 4 with 4 rows and 36 columns
- V6116 mux mode 8 with 8 rows and 32 columns
- Low dynamic current, 250 µA max.
- Low standby current, 1 µA max. at +25°C
- Voltage bias and mux signal generation on chip
- 2 display RAMs addressable as 8 x 40 words
- Display refresh on chip, dual RAM for display storage: 2 x (2x38; 4x36; 8x32)
- Column driver only mode to have 40 column outputs Dual RAM for display storage: 2x (2; 4; 8x40)
- Crossfree cascadable for large LCD applications
- Separate logic and LCD supply voltage pins
- Wide power supply range: V_{DD}: 2 to 6V, V_{LCD}: 2 to 9V
- Blank function for LCD blanking by data, BLANK bit and STR signal (STR only if internal bias)
- All segments ON by data and SET bit
- Bit mapped
- Serial interface
- No busy state
- LCD updating synchronized to the LCD refresh signal
- TAB and bumped die form delivery. Other form delivery on request
- -40 to + 85 °C temperature range

Typical Operating Configuration

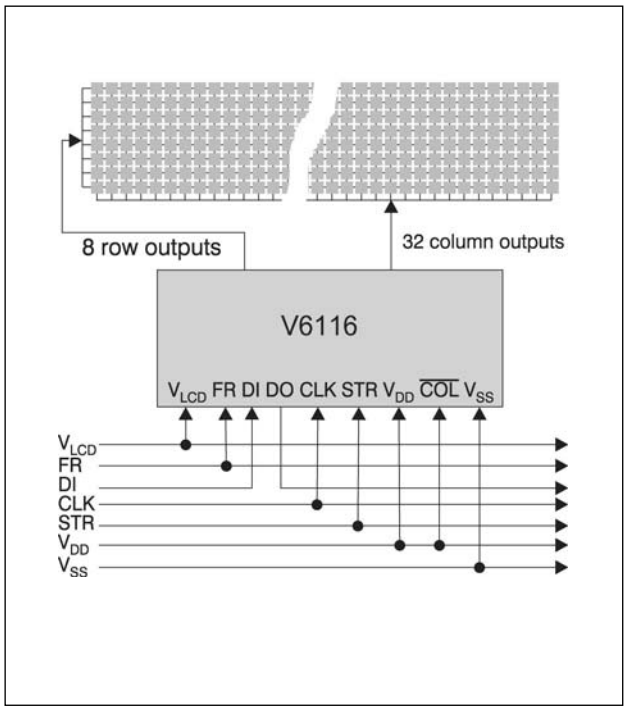
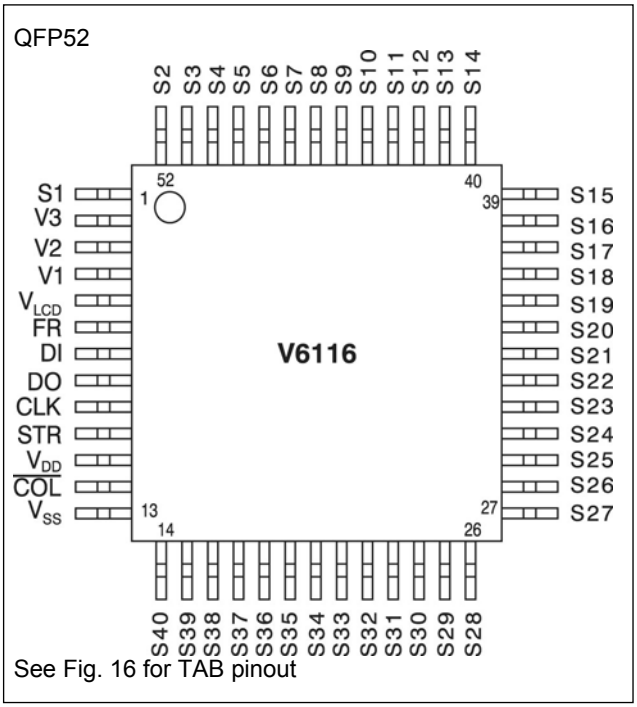


Fig. 1

Pad Assignment



See Fig. 16 for TAB pinout

Fig. 2

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Absolute Maximum Ratings

Parameter	Symbol	Conditions
Supply voltage range	V_{DD}	-0.3V to 9V
LCD supply voltage range	V_{LCD}	-0.3V to 9.5V
Voltage at DI, DO, CLK, STR, FR, $\overline{COL}$	V_{LOGIC}	-0.3V to V_{DD}+0.3V
Voltage at V1 to V3, S1 to S40	V_{DISP}	-0.3V to V_{LCD} + 0.3V
Storage temperature range	T_{STO}	-65 to +150°C
Electrostatic discharge max. to MIL-STD-883C method 3015.7 with ref. to V_{SS}	V_{Smax}	1000V
Maximum soldering conditions	T_{Smax}	290°C x 10s

Table 1

Stresses above these listed maximum ratings may cause permanent damages to the device. Exposure beyond specified operating conditions may affect device reliability or cause malfunction.

Handling Procedures

This device has built-in protection against high static voltages or electric fields; however, anti-static precautions must be taken as for any other CMOS component. Unless otherwise specified, proper operation can only occur when all terminal voltages are kept within the voltage range. Unused inputs must always be tied to a defined logic voltage level.

Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Operating Temperature	T_A	-40		+85	°C
Logic supply voltage	V_{DD}	2	5	6	V
LCD supply voltage	V_{LCD}	2	5	9	V

Table 2

Electrical Characteristics

V_{DD} = 5V ±10%, V_{LCD} = 2 to 7V and T_A = -40 to +85°C, unless otherwise specified

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Dynamic supply current	I_{LCD}	See note 1		150	250	µA
Dynamic supply current	I_{DD}	See note 1 at T_A = 25°C		0.1	1	µA
Dynamic supply current	I_{DD}	See note 1		3	12	µA
Dynamic supply current	I_{DD}	See note 2		200	250	µA
Standby supply current	I_{SS}	See note 3 at T_A = 25°C		0.1	1	µA
Control Signals DI, CLK, STR, FR and $\overline{COL}$						
Input leakage	I_{IN}	0 < V_{IN} < V_{DD}		1	1000	nA
Input capacitance	C_{IN}	at T_A = 25°C		8		pF
Low level input voltage	V_{IL}		0		0.8	V
High level input voltage for DI, STR, FR and $\overline{COL}$	V_{IH}		2.0		V_{DD}	V
High level input voltage for CLK	V_{IH}		3.0		V_{DD}	V
Data Output DO						
High level output voltage	V_{OH}	I_H = 4 mA	2.4			V
Low level output voltage	V_{OL}	I_L = 4 mA			0.4	V
Driver Outputs S1 … S40						
Driver impedance (note 4)	R_{OUT}	I_{OUT} = 10µA, V_{LCD} = 7V		1.0	1.5	kΩ
Driver impedance (note 4)	R_{OUT}	I_{OUT} = 10µA, V_{LCD} = 3V		2.6	3.5	kΩ
Driver impedance (note 4)	R_{OUT}	I_{OUT} = 10µA, V_{LCD} = 2V		7		kΩ
Bias impedance V1, V2, V3 (note 5)	R_{BIAS}	I_{OUT} = 10µA, V_{LCD} = 7V		18	24	kΩ
Bias impedance V1, V2, V3 (note 5)	R_{BIAS}	I_{OUT} = 10µA, V_{LCD} = 3V		20	27	kΩ
Bias impedance V1, V2, V3 (note 5)	R_{BIAS}	I_{OUT} = 10µA, V_{LCD} = 2V		24		kΩ
DC output component	± VDC	see Tables 4a & 4b, V_{LCD} = 5V		30	50	mV

Table 3

Note 1: All outputs open, STR at V_{SS}, FR = 400 Hz, all other inputs at V_{DD}.

Note 2: All outputs open, STR at V_{SS}, FR = 400 Hz, f_{CLK} = 1 MHz, all other inputs at V_{DD}.

Note 3: All outputs open, all inputs at V_{DD}.

Note 4: This is the impedance between of the voltage bias level pins (V1, V2 or V3) and the output pins S1 to S40 when a given voltage bias level is driving the outputs (S1 to S40)

Note 5: This is the impedance seen at the segment pin. Outputs measured one at a time.

Column Drivers

Outputs	FR Polarity	$\overline{COL}$	Column Data	Measured*	Guaranteed
S1 to S40	logic 1	logic 0	logic 1	$\lvert Sx^* - V_{SS} \rvert$	
S1 to S40	logic 0	logic 0	logic 1	$\lvert V_{LCD} - Sx^* \rvert$	$\lvert V_{LCD} - Sx^* \rvert = \lvert Sx^* - V_{SS} \rvert \pm 25$ mV
S1 to S40	logic 1	logic 0	logic 0	$\lvert V_{LCD} - Sx^* \rvert$	
S1 to S40	logic 0	logic 0	logic 0	$\lvert Sx^* - V_{SS} \rvert$	$\lvert V_{LCD} - Sx^* \rvert = \lvert Sx^* - V_{SS} \rvert \pm 25$ mV

Table 4a

*Sx = the output number (ie. S1 to S40)

Row Drivers

Outputs	FR Polarity	$\overline{COL}$	Column Data	Measured*	Guaranteed
S1 to Sn*	logic 1	logic 1	logic 1	$\lvert V_{LCD} - Sx \rvert$	
S1 to Sn*	logic 0	logic 1	logic 1	$\lvert Sx - V_{SS} \rvert$	$\lvert V_{LCD} - Sx \rvert = \lvert Sx - V_{SS} \rvert \pm 25$ mV
S1 to Sn*	logic 1	logic 1	logic 0	$\lvert Sx - V_{SS} \rvert$	
S1 to Sn*	logic 0	logic	logic 0	$\lvert V_{LCD} - Sx \rvert$	$\lvert V_{LCD} - Sx \rvert = \lvert Sx - V_{SS} \rvert \pm 25$ mV

Table 4b

*n = the V6116 mux programme number (ie. 2, 4 or 8)

Timing Characteristics

V_{DD} = 5V ± 10%, V_{LCD} = 2 to 7V and T_A = -40 to +85°C

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Clock high pulse width	t_{CH}		120			ns
Clock low pulse width	t_{CL}		120			ns
Clock and FR rise time	t_{CR}				200	ns
Clock and FR fall time	t_{CF}				200	ns
Data input setup time	t_{DS}		20 (note 1)			ns
Data input hold time	t_{DH}		30 (note 1)			ns
Data output propagation	t_{PD}	C_{LOAD} = 50pF			100	ns
STR pulse width	t_{STR}		100			ns
CLK falling to STR rising	t_P		10			ns
STR falling to CLK falling	t_D		200			ns
FR frequency (2/4/8)	f_{FR} (note 2)	T_A = 25°C		128/256/512		Hz

Table 5a

Note 1: $t_{DS} + t_{DH}$ minimum must be ≥ 100 ns. If t_{DS} = 20 ns then t_{DH} ≥ 80ns.
Note 2: V6116 n, FR = n times the desired LCD refresh rate where n is the V6116 mux mode number.

V_{DD} = 2 to 6V, V_{LCD} = 2 to 8V and T_A = -40 to +85°C

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Clock high pulse width	t_{CH}		500			ns
Clock low pulse width	t_{CL}		500			ns
Clock and FR rise time	t_{CR}				200	ns
Clock and FR fall time	t_{CF}				200	ns
Data input setup time	t_{DS}		100 (note 1)			ns
Data input hold time	t_{DH}		150 (note 1)			ns
Data output propagation	t_{PD}	C_{LOAD} = 50pF			400	ns
STR pulse width	t_{STR}		500			ns
CLK falling to STR rising	t_P		10			ns
STR falling to CLK falling	t_D		1			µs
FR frequency (2/4/8)	F_{FR} (note 2)			128/256/512		Hz

Table 5b

Note 1: $t_{DS} + t_{DH}$ minimum must be ≥ 500 ns. If t_{DS} = 100 ns then t_{DH} ≥ 400ns.
Note 2: V6116 n, FR = n times the desired LCD refresh rate where n is the V6116 mux mode number.

Timing Waveforms

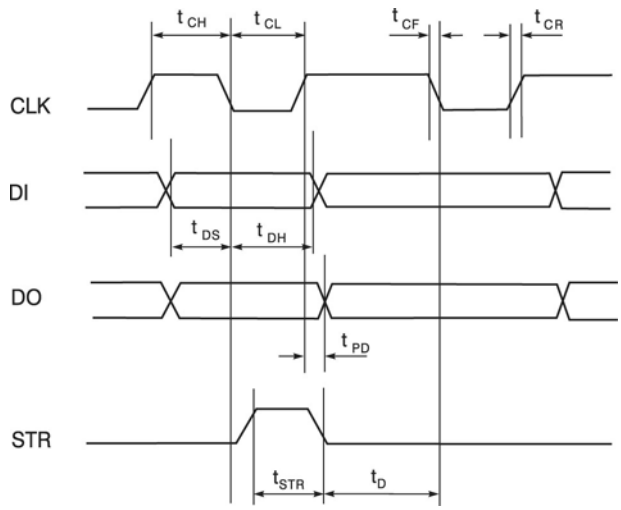


Fig. 3

Programmation Data Bits

Command Bits 0 to 7							
0	1	2	3	4	5	6	7
Multiplex Ratio		W	RAM Address (see Fig. 5)			SET	Blank

Mux Ratio (bit 0, 1)		
0	1	Mux Mode
0	0	2
0	1	4
1	0	-
1	1	8

Bit 6: SET bit forces all column outputs ON
Bit 7: Blank bit forces all column outputs OFF
Bit 2: When "0", write RAM 1 and read RAM 2. When "0" and RAM-Add = 0 and STR, write RAM 1 and read RAM 1. When "1", write RAM 2 and read RAM1. When "1" and RAM-Add = 0 and STR, write RAM 2 and read RAM 2.

Fig. 4

Data Transfer Cycle

V6116 as a row and column driver, 48 bit load cycle, RAM selected address provided by command bits 3 to 5.

Command Bits 3 to 5			Display RAM 1 or 2	
Mux Mode 2	Mux Mode 4	Mux Mode 8	Address	LCD Row
000	000	000	10000000	Row 1
001	001	001	01000000	Row 2
	010	010	00100000	Row 3
	011	011	00010000	Row 4
		100	00001000	Row 5
		101	00000100	Row 6
		110	00000010	Row 7
		111	00000001	Row 8

All mux mode programmations or $\overline{COL}$ states need 48 bit load cycle.

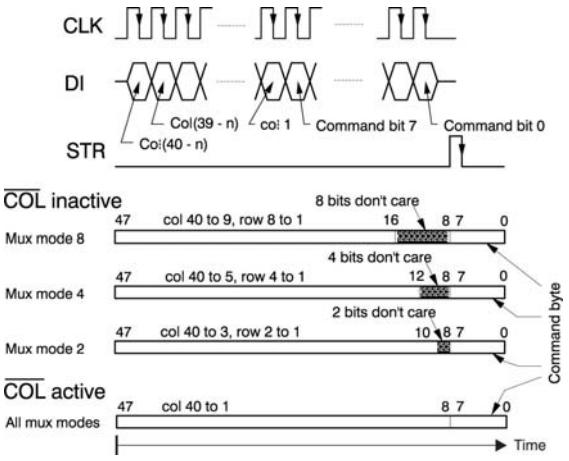
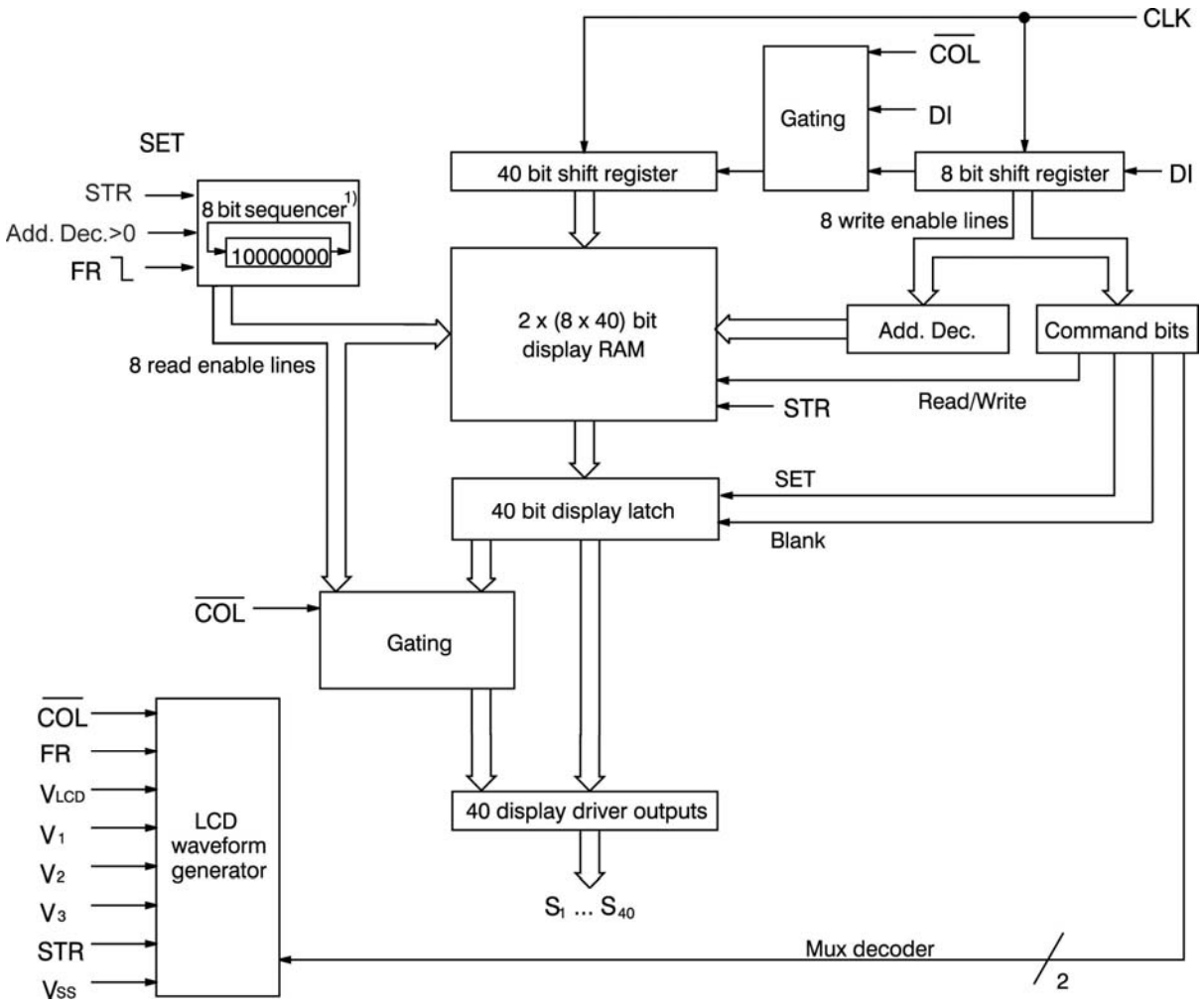


Fig. 5

Block Diagram



Note 1: When falling edge of STR and RAM-Add = 0 and FR arrives, then the display selected RAM address 10000000 (which corresponds to row 1) has to be selected by the 8 bit sequencer. Cascaded V6116s are synchronized in this way. The LCD picture restarts from row 1 each time full RAM data are written.

Fig. 6

Pin Assignment

Name	Function
S1..S40	LCD outputs, see Table 7
V3	LCD voltage bias level 3 (note 1, 2)
V2	LCD voltage bias level 2 (note 1)
V1	LCD voltage bias level 1 (note 1)
V_{LCD}	Power supply for the LCD
FR	AC input signal for LCD driver output
DI	Serial data input
DO	Serial data output
CLN	Data clock input
STR	Data strobe, blank, synchronize input
V_{DD}	Power supply for logic
$\overline{COL}$	Column only driver mode
V_{SS}	Supply GND

Table 9

Name	$\overline{COL}$ inactive			$\overline{COL}$ active
	V6116 (2)	V6116 (4)	V6116 (8)	
S1	Row1	Row1	Row1	Col1
S2	Row2	Row2	Row2	Col2
S3	Col1	Row3	Row3	Col3
S4	Col2	Row4	Row4	Col4
S5	Col3	Col1	Row5	Col5
S6	Col4	Col2	Row6	Col6
S7	Col5	Col3	Row7	Col7
S9-S40	Col7…38	Col5…36	Col1…32	Col9…40

Table 7

Note 1: The V6116 has internal voltage bias level generation. When driving large pixels, an external resistor divider chain can be connected to the voltage bias level inputs to obtain enhanced display contrast (see Fig. 12, 13 and 14). The external resistor divider ratio should be in accordance with the internal resistor ratio (see Table 8).
Note 2: V3 is connected internally to V_{SS} on the V6116 060 mux mode 4.

LCD Voltage Bias Levels

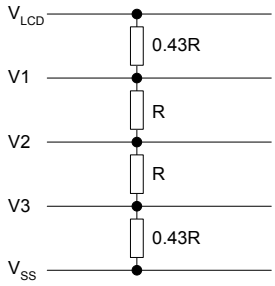
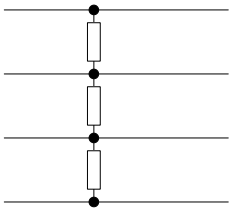
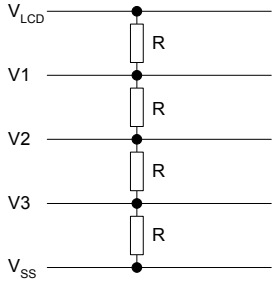
	LCD Drive Type	LCD Bias Configuration	$\frac{V_{OP}}{V_{OFF}(rms)}$ (note 1)	$\frac{V_{ON}(rms)}{V_{OFF}(rms)}$
	V6116 (2) n=2 1:2 MUX	5 Levels	$\sqrt{\frac{2n}{1-\sqrt{\frac{1}{n}}}} = 3.69$	$\sqrt{\frac{\sqrt{n}+1}{\sqrt{n}-1}} = 2.41$
	V6116 (4) n=4 1:4 MUX	1/3 Bias 4 Levels	3	$\sqrt{1+\frac{8}{n}} = 1.73$
	V6116 (8) n=8 1:8 MUX	1/4 Bias 5 Levels	$\frac{4}{\sqrt{1+\frac{3}{n}}} = 3.4$	$\sqrt{\frac{n+15}{n+3}} = 1.446$

Table 8

Note 1: $V_{OP} = V_{LCD} - V_{SS}$

Row and Column Multiplexing Waveform V6116 (2)

$V_{OP} = V_{LCD} - V_{SS}$, $V_{STATE} = V_{COL} - V_{ROW}$

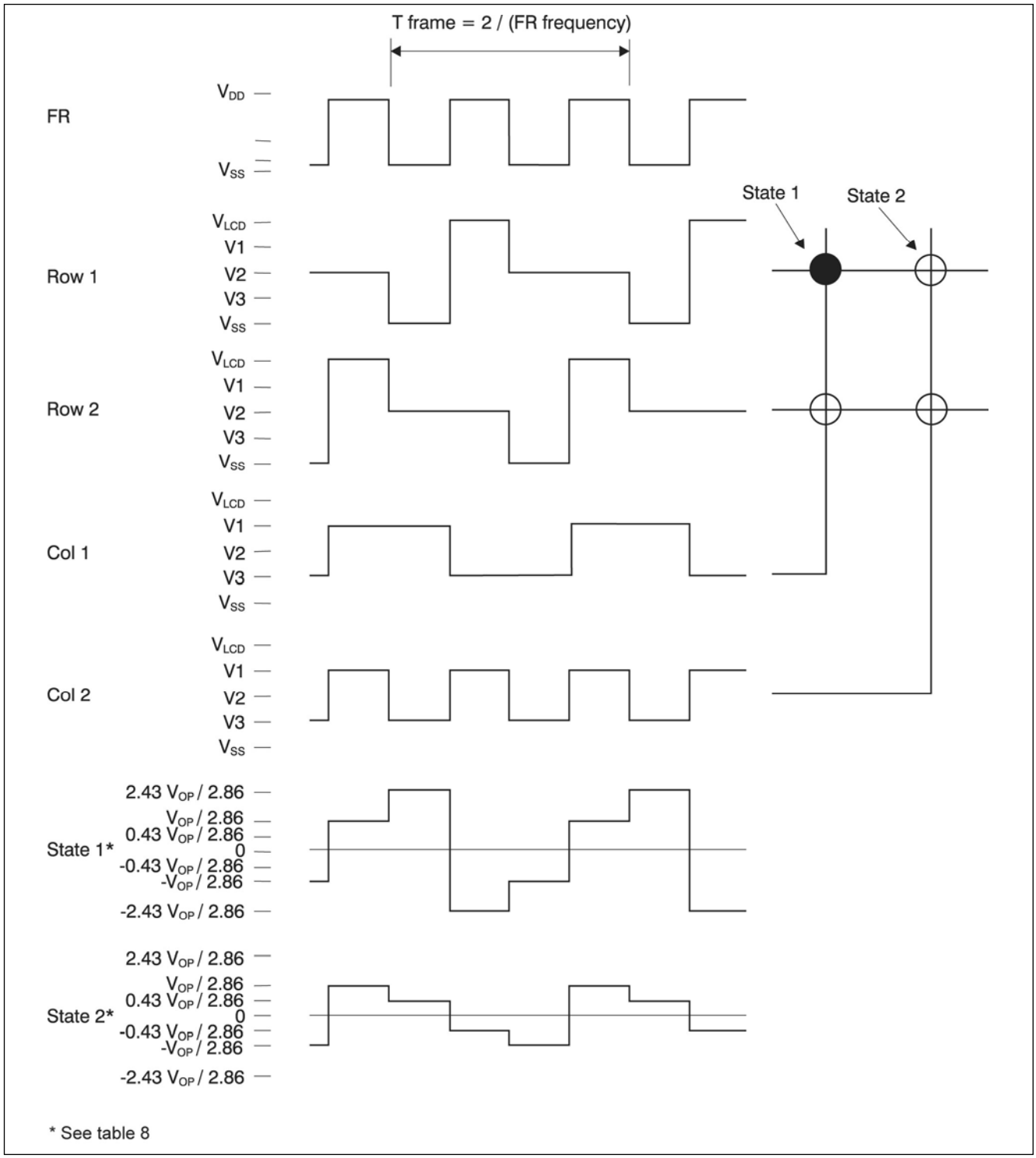


Fig. 7

Row and Column Multiplexing Waveform V6116 (4)

$V_{OP} = V_{LCD} - V_{SS}$, $V_{STATE} = V_{COL} - V_{ROW}$

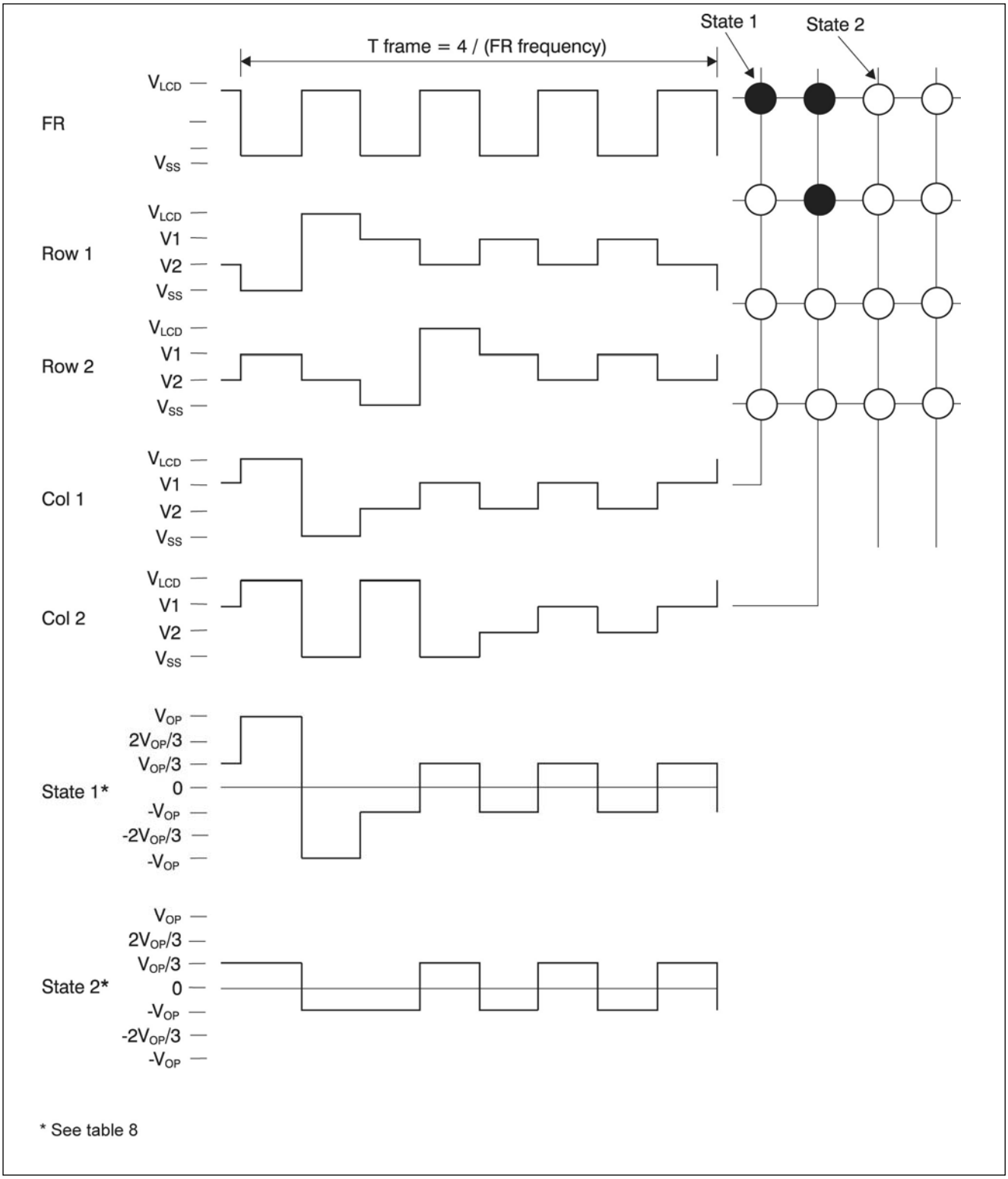


Fig. 8

Row and Column Multiplexing Waveform V6116 (8)

$V_{OP} = V_{LCD} - V_{SS}$, $V_{STATE} = V_{COL} - V_{ROW}$

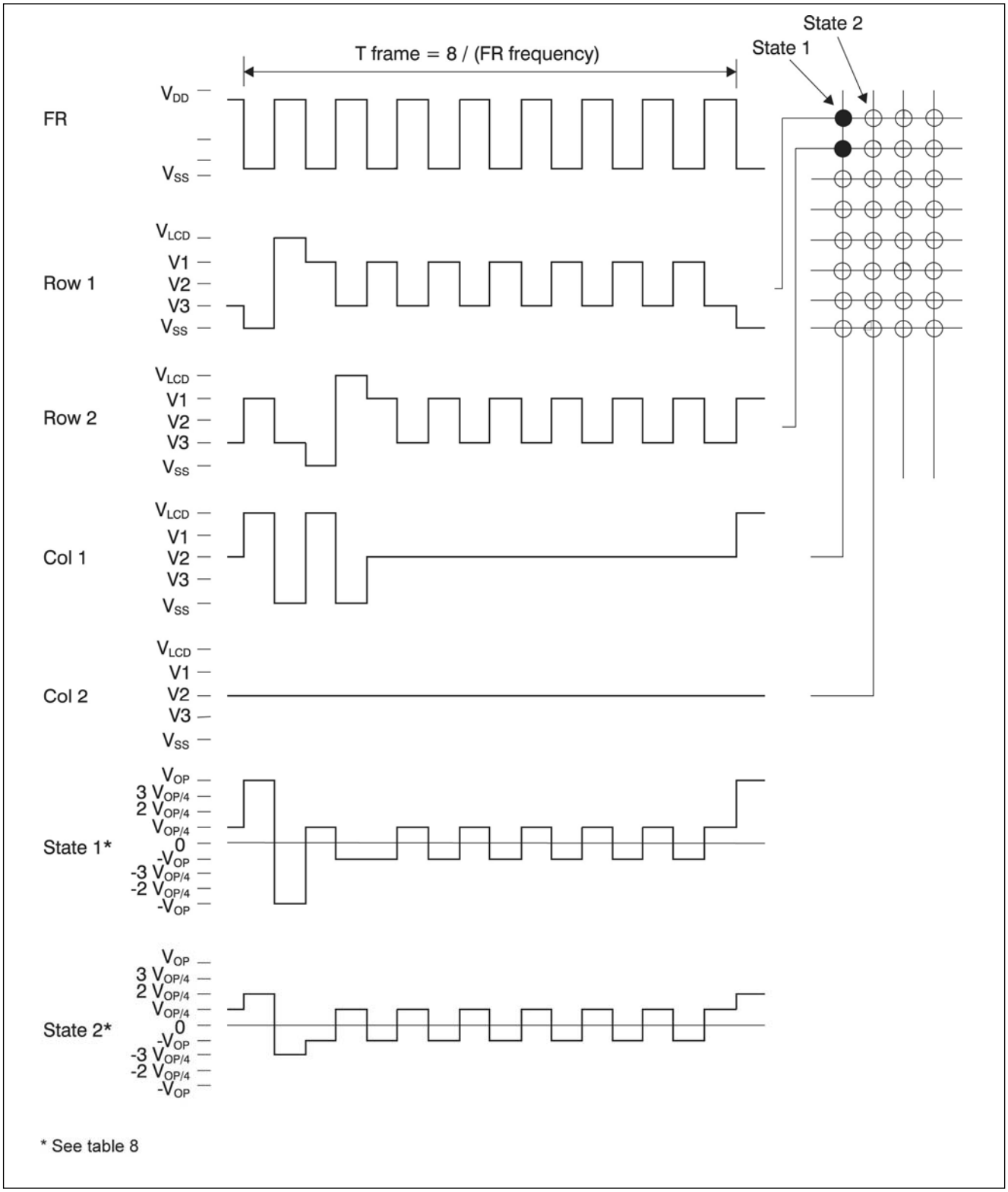


Fig. 9

Functional Description

Supply Voltage V_{LCD}, V_{DD}, V_{SS}

The voltage between V_{DD} and V_{SS} is the supply voltage for the logic and the interface. The voltage between V_{LCD} and V_{SS} is the supply voltage for the LCD and is used for the generation of the internal LCD bias levels. The internal LCD bias levels have a maximum impedance of 25 kΩ for a V_{LCD} voltage from 3 to 8V. Without external connections to the V1, V2, V3 bias level inputs, the V6116 can drive most medium sized LCD (pixel area up to 4'000 mm^2).

For displays with a wide variation in pixel sizes, the configuration shown in Fig. 13 can give enhanced contrast by giving faster pixel switching times. On changing the row polarity (see Fig. 7, 8 and 9) the parallel capacitors lower the impedance of the bias level generation to the peak current, giving faster pixel charge times and thus a higher RMS "on" value. A higher RMS "on" value can give better contrast. IF for a given LCD size and operating voltage, the "off" pixels appear "on", or there is poor contrast, then an external bias level generation circuit can be used with the V6116. An external bias generation circuit can lower the bias level impedance and hence improve the LCD contrast (see Fig. 12). The optimum values of R, Rx and C, vary according to the LCD size used and V_{LCD}. They are best determined through actual experimentation with the LCD.

For LCD with very large average pixel area (eg. up to 10'000 mm^2), the bias level configuration shown in Fig. 14 should be used.

When V6116s are cascaded, connect the V1, V2 and V3 bias inputs as shown in Fig. 10. The pixel load is averaged across all the cascaded drivers. This will give enhanced display contrast as the effective bias level source impedance is the parallel combination of the total number of drivers. For example, if two V6116 are cascaded as shown in Fig. 10, then the maximum bias level impedance becomes 12.5 kΩ for a V_{LCD} voltage from 3 to 8V.

Table 8 shows the relationship between V1, V2 and V3 for the multiplex rates 2, 4 and 8. Note that V_{LCD} > V1 > V2 > V3 for the V6116 2 and V6116 8, and for the V6116 4, V_{LCD} > V1 > V2 and V3 = V_{SS}.

Data Input /Output

The data input pin, DI, is used to load serial data into the V6116. The serial data word length is 48 bits. Data are loaded in inverse numerical order, the data for bit 48 is loaded first and the data for bit 1 last.

The column data bits are loaded first and then the command bits (see Fig. 5).

The data output pin, DO, is used in cascaded applications (see Fig. 10). DO transfers the data to the next cascaded chip. The data at DO is equal to the data at DI delayed by 48 clock periods. In order to cascade V6116s, the DO of one chip must be connected to DI of the following chip (see Fig. 10). In cascaded applications the data for the last V6116 (the one that does not have DO connected) must be loaded first and the data for the first V6116 (its DI is connected to the processor) loaded last (see Fig. 10).

The display selected RAM word length is 40 bits (see Fig. 6). Each LCD row has a corresponding display RAM address which provides the column data (on or off) when the row is selected (on). When downloading data to the V6116, any display selected RAM address can be chosen. Display selected RAM address is given by command bits 3 to 5, the RAM is selected with the command bit 2. If bit 2 = 0, then RAM 1 can be written and RAM 2 is read. When falling edge of STR and RAM-Add = 0, then RAM 1 will be read. If bit 2 = 1, then RAM 2 can be written and RAM 1 is read. When falling edge of STR and RAM-Add = 0, then RAM 2 will be read. This last sequence synchronizes the V6116s when cascaded. Bit 7 forces all column outputs at 0L (display OFF). Bit 6 forces all column outputs at 1L (display ON). When bit 6 (SET) and bit 7 (BLANK) are active, the BLANK function has priority. The command bits, bit 6 and bit 7, are activated when logic 1. The command bits, bit 1 and bit 0, define the mux mode (see Fig. 4).

CLK Input

The CLK input is used to clock the DI serial data into the shift register and to clock the DO serial data out. Loading and shifting of the data occurs at the falling edge of this clock, outputting of the data at the rising edge (see Fig. 3). When cascading devices, all CLK lines should be tied together (see Fig. 10).

STR Input

The STR input is used to write to the display RAM, to blank the LCD (V6116 060), and to synchronize cascaded V6116s. The STR input writes the data loaded into the shift register, on the DI input, to the display selected RAM on the falling edge of the STR signal.

The STR input when high blanks the LCD by disconnecting the internal voltage bias generation from the V_{SS} potential (V6116 060). Segment outputs S1 to S40 (rows and columns) are pulled up to V_{LCD}. The delay to driving the LCD with V_{LCD} on S1 to S40, is dependent on the capacitive load of the LCD and is typically 1 µs. An LCD pixel responds to RMS voltage and takes approximately 100 ms to turn on or off. The delay from putting STR high to the LCD being blank is dependent on the LCD off time and is typically 100 ms. In applications which have a long STR pulse width (10 µs) the LCD is driven by V_{LCD} on both the rows and columns during this time. As the time is short (1 µs), it will have zero measurable effect on the RMS "on" value (over 100 ms) of an LCD pixel and also zero measurable effect on the pixel DC component. Such STR pulses will not be visible to the human eye on an LCD.

Note: if an external voltage bias generation circuit is used as shown in Fig. 12 to 14, the LCD blank function (STR high) will not blank the LCD. Fig. 15 (only available for the V6116 060, with internal resistor) shows how to do a BLANK with the external resistor divider bias by STR signal. When STR is high, the LCD will be driven by the parallel combination of the external voltage bias generation circuit and part of the internal voltage bias generation circuit.

The STR input is used also to synchronize the V6116's circuit when cascaded. The synchronization occurs on the falling edge of the STR signal, provided bit 6 and 7 preset to 11. The synchronization will set effective on the next falling edge of the FR signal. A time frame begins with row 1 and so the LCD picture is rebuilt from row 1 each time cascaded V6116s are synchronized. When cascading devices, all STR lines must be tied together (see Fig. 10).

FR Input

The FR signal controls the segment output frequency generation (see Fig. 7, 8 and 9). To avoid having DC on the display, the FR signal must have a 50% duty cycle. The frequency of the FR signal must be n times the desired display refresh rate, where n is the V6116 mux mode no. (2, 4 or 8). For example, if the desired refresh rate is 40 Hz, the FR signal frequency must be 320 Hz for

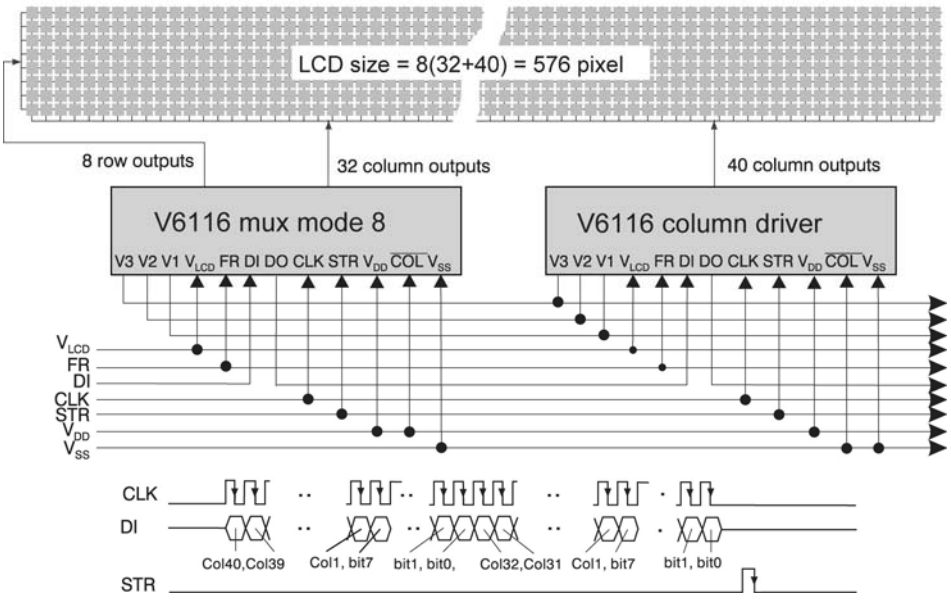
the V6116 8. A selected row (on) is in phase with the FR signal (see Fig. 7, 8 and 9).
It is recommended that data transfer to the V6116 should be synchronized to the FR signal to avoid a falling or rising edge on the FR signal while writing data to the V6116. The LCD pixels change polarity with the FR signal. On the edges of the FR signal current spikes will appear on the V_{SS} and V_{LCD} supply lines. If the supply lines have high impedance then voltage spikes will appear. These voltage spikes could interfere with data loading on the DI and CLK pins. The V6116 has filters in order to reduce perturbation on the input signals.
It is also recommended that data transfer to the V6116 should be synchronized to the FR signal to avoid DC component which may especially appear during Blink function.

Driver Outputs S1 to S40
There are 40 LCD driver outputs on the V6116. When $\overline{COL}$ is inactive, the outputs S1 to Sn function as row drivers and the outputs S(n+1) to S40 function as column drivers, where n is the V6116 mux mode no. (2, 4 or 8). When $\overline{COL}$ is active, all 40 outputs function as column drivers (see Table 6). There is a one to one relationship between the display selected RAM and the LCD driver outputs. Each pixel (segment) driven by the V6116 on the LCD has a display RAM bit which corresponds to it. Setting the bit turns the segment "on" and clearing it turns it "off".

$\overline{COL}$ Input
The V6116 functions as a row and column driver while the $\overline{COL}$ input is inactive. When active, the $\overline{COL}$ input configures the V6116 to function as a column driver only. The former row outputs function as column outputs. In cascaded applications, one V6116 should be used in the row and column configuration ($\overline{COL}$ inactive) and the rest as pure column drivers ($\overline{COL}$ active) (see Fig. 10).
Note: when cascading V6116s never cascade one mux mode no. with another. If a V6116 mux mode 8 is used to drive the rows, then only V6116s mux mode 8 can be cascaded with it (see Fig. 10).

Power Up
On power up the data in the shift registers, the two display RAMs and the 40 bit display latches are undefined. The STR input and the command bit 7 should be taken high on power up to blank the display, then the display data written to the display selected RAM (see Fig. 11). When finished the initial write to the display selected RAM, take the STR input low to display the display selected RAM contents (see also section "STR Input").

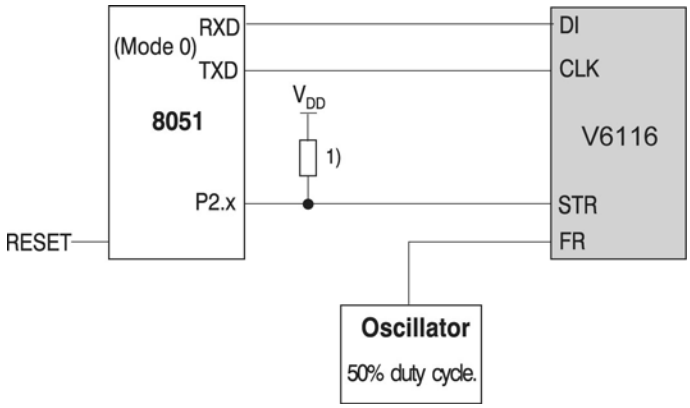
Applications
Two V6116 Mux Mode 8 Cascaded



By connecting the V1, V2 and V3 bias outputs as shown, the pixel load is averaged across all the drivers. The effective bias level source impedance is the parallel combination of the total number of drivers. For example, if two V6116 are cascaded as above, then the maximum bias level impedance becomes 12.5 kΩ.

Fig. 10

Microprocessor Interface and LCD Blanking



1) When the microprocessor is reset, the port pin will be configured as an input and so the STR line would float. The pull-up resistor will ensure that the LCD is blank while the system reset line is active and after until the port pin is set up by software.

Writing Data to the Display RAM while keeping the LCD Blank

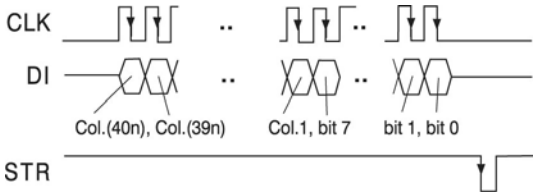
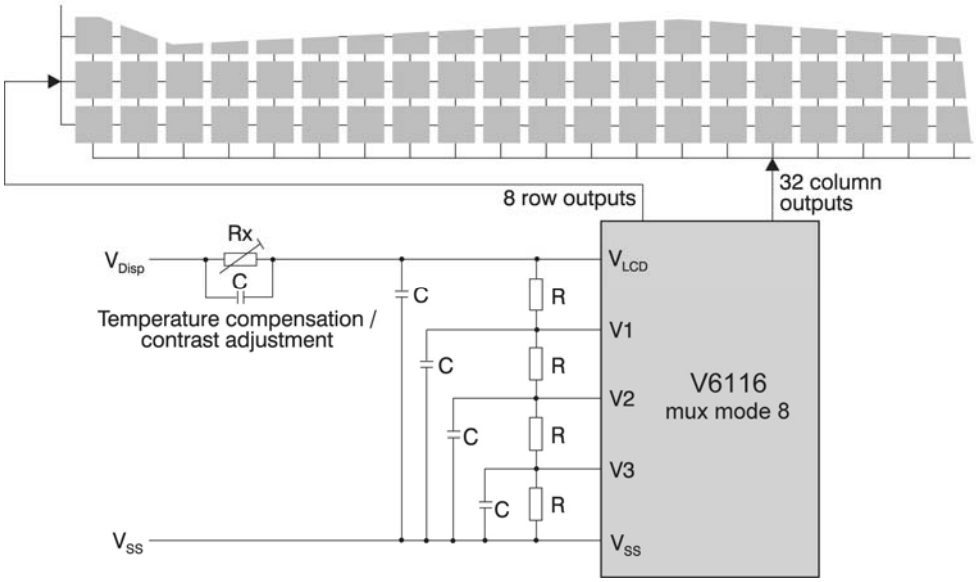


Fig. 11

V6116 with External Resistor Divider Bias Generation

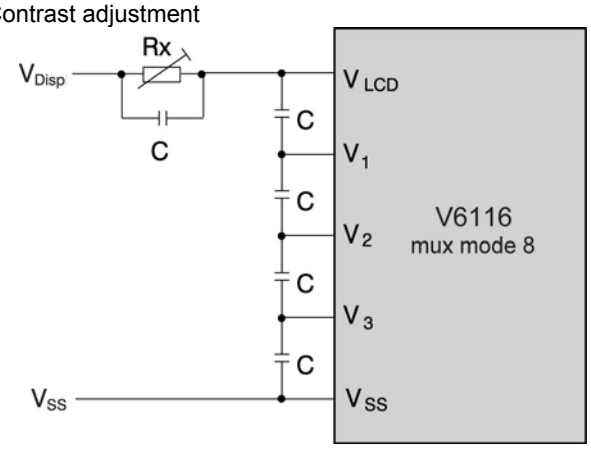


Example set values:
R = 3.3 – 10 kΩ
C = 2.2 – 47 nF
Rx is given by the formula:
Rx = 4R ((V_{DISP}/V_{LCD})-1) = 10 – 30 kΩ

Fig. 12

Enhancing Switching from the V6116

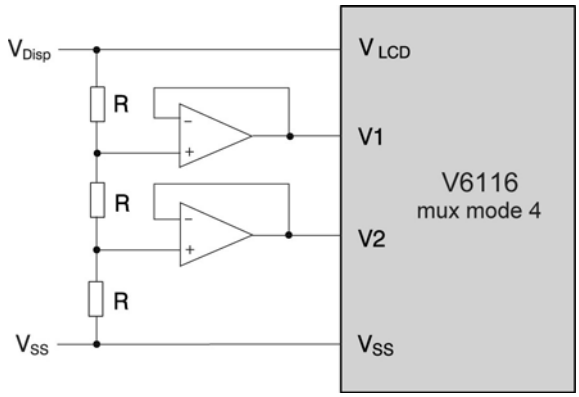
Temperature compensation/
Contrast adjustment



C = 1µF
Rx is given by the formula
Rx = 4(24 kΩ) ((V_{DISP}/V_{LCD})-1)

Fig. 13

Bias Configuration for Large LCD



Large LCD example:
V_{OP} = 5V, average pixel active area = up to 10'000 mm^2, display refresh rate = 64 Hz

For a single V6116 mux mode 4 driving of such an LCD, the voltage follower buffer (opamp) requirement is:
peak current 1.8 mA
steady state current typically 150 µA

Fig. 14

LCD Blank with External Resistor Divider Bias Generation (only available for the V6116 060)

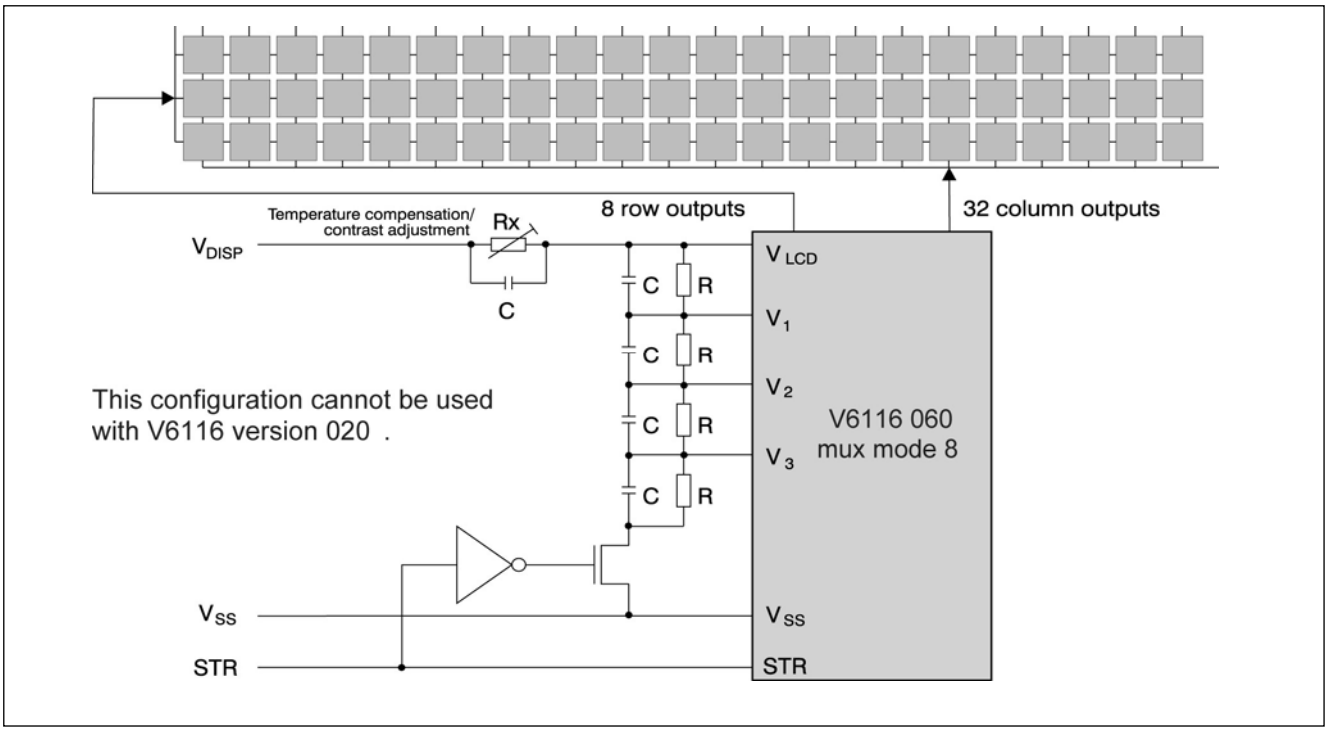
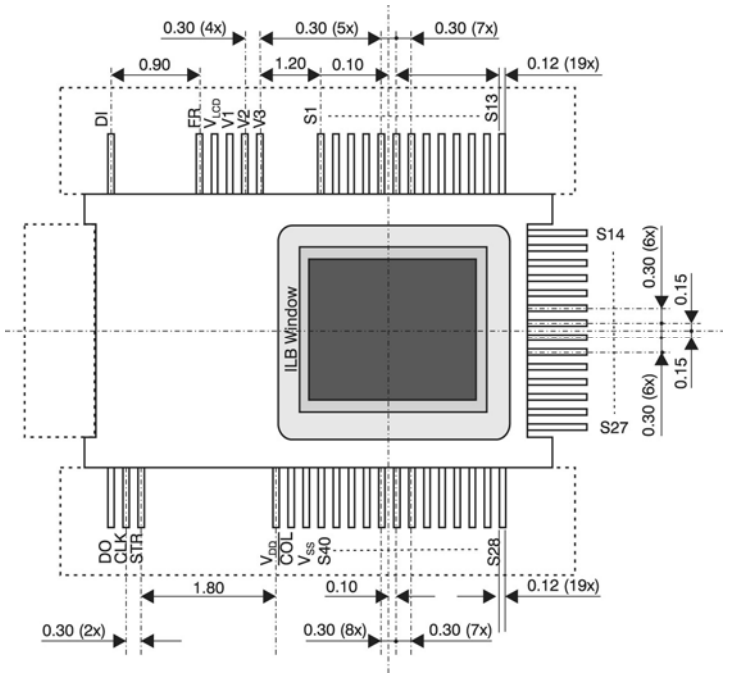


Fig. 15

Package and Ordering Information

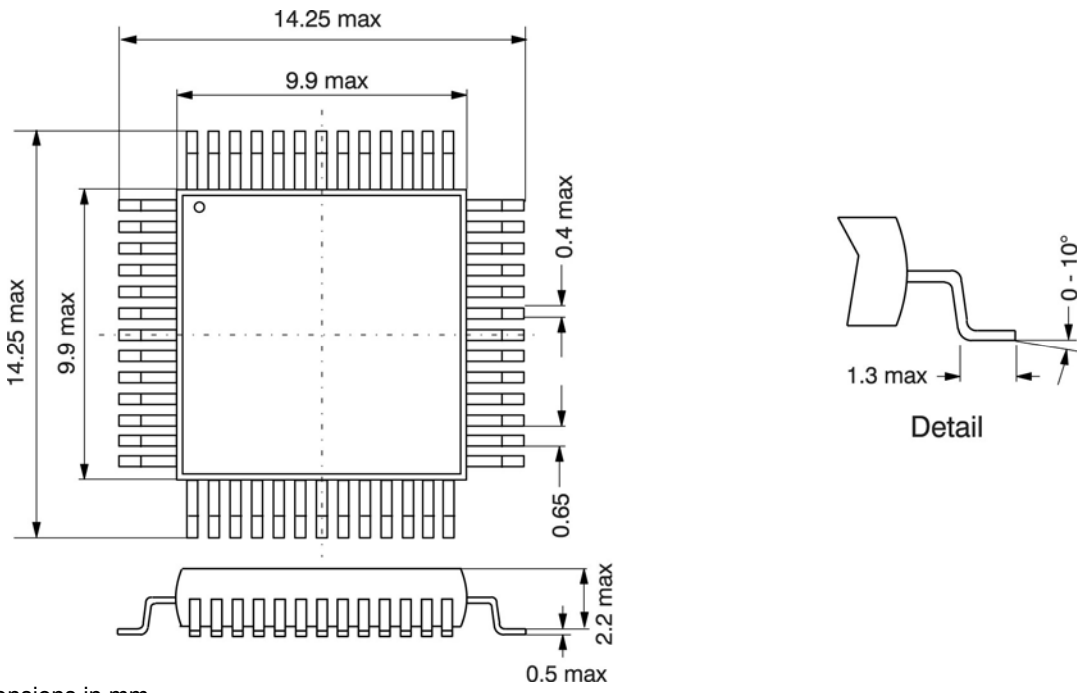
Dimensions of TAB Package



All dimensions in mm

Fig. 16

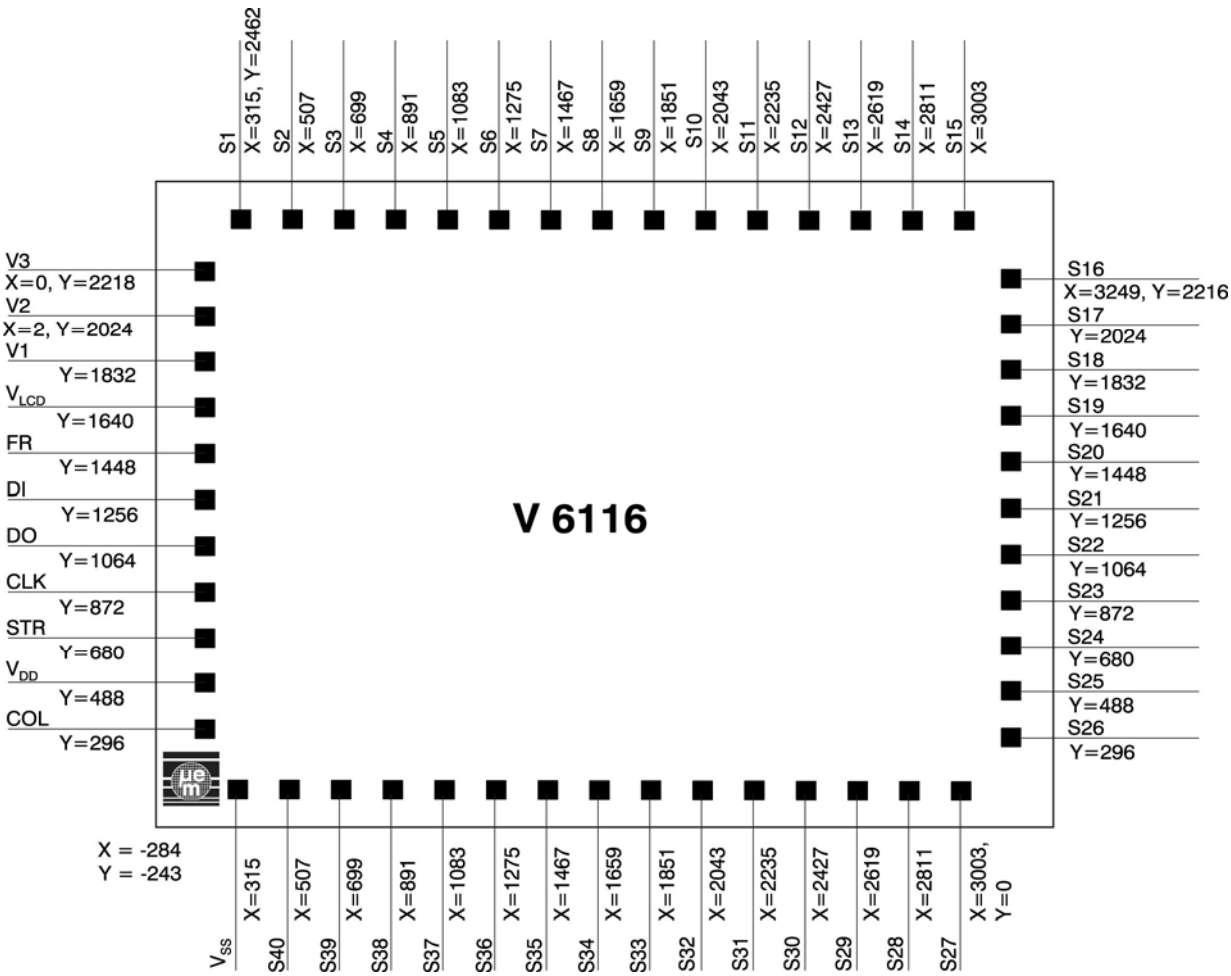
Dimensions of QPF Package



All dimensions in mm

Fig. 17

Dimensions of the Chip



All dimensions in micron

Bump height : 25 microns
Chip size is X = 3784 by Y = 2946 microns or X = 149 by Y = 116 mils
Note: The origin (0,0) is the lower left coordinate of center pads
The lower left corner of the chip shows the distances to the origin

Fig. 18

Ordering Information
When ordering, please specify the complete Part Number

Part Number	Package / Die Form	Delivery Form / Bumping
V6116V6WP11E	Die in waffle pack, 11 mils thickness	With gold bumps
V6116V6WP27E	Die in waffle pack, 27 mils thickness	With gold bumps
V6116V60TBA-3041	TAB (Tape Automated Bonding), film A	-

For other delivery form (QFP52 package or version 20), please contact EM Microelectronic-Marin S.A.
Minimum order quantity might apply.