

1GB - 128Mx72 SDRAM REGISTERED and SPD, w/PLL

FEATURES

- Clock speeds of 100MHz and 133MHz
- Burst Mode Operation
- Auto and Self Refresh capability
- LVTTTL compatible inputs and outputs
- Serial Presence Detect with EEPROM
- Fully synchronous: All signals are registered on the positive edge of the system clock
- Programmable Burst Lengths: 1, 2, 4, 8 or Full Page
- 3.3V ± 0.3V Power Supply
- 168 Pin DIMM JEDEC

DESCRIPTION

The W3DG72127V is a 128Mx72 synchronous DRAM module which consists of eighteen 128Mx4 SDRAM components in TSOP II package, two 18 bit drive ICs for input control signal and one 2K EEPROM in an 8 pin TSSOP package for Serial Presence Detect which are mounted on a 168 Pin DIMM multilayer FR4 Substrate.

* This product is subject to change without notice.

Pin Configurations (FRONT SIDE/BACK SIDE)

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	V _{SS}	29	DQM1	57	DQ18	85	V _{SS}	113	DQM5	141	DQ50
2	DQ0	30	CS0#	58	DQ19	86	DQ32	114	*CS1#	142	DQ51
3	DQ1	31	DNU	59	V _{CC}	87	DQ33	115	RAS#	143	V _{CC}
4	DQ2	32	V _{SS}	60	DQ20	88	DQ34	116	V _{SS}	144	DQ52
5	DQ3	33	A0	61	NC	89	DQ35	117	A1	145	NC
6	V _{CC}	34	A2	62	*VREF	90	V _{CC}	118	A3	146	*VREF
7	DQ4	35	A4	63	*CKE1	91	DQ36	119	A5	147	REGE
8	DQ5	36	A6	64	V _{SS}	92	DQ37	120	A7	148	V _{SS}
9	DQ6	37	A8	65	DQ21	93	DQ38	121	A9	149	DQ53
10	DQ7	38	A10/AP	66	DQ22	94	DQ39	122	BA0	150	DQ54
11	DQ8	39	BA1	67	DQ23	95	DQ40	123	A11	151	DQ55
12	V _{SS}	40	V _{CC}	68	V _{SS}	96	V _{SS}	124	V _{CC}	152	V _{SS}
13	DQ9	41	V _{CC}	69	DQ24	97	DQ41	125	*CLK1	153	DQ56
14	DQ10	42	CLK0	70	DQ25	98	DQ42	126	*A12	154	DQ57
15	DQ11	43	V _{SS}	71	DQ26	99	DQ43	127	V _{SS}	155	DQ58
16	DQ12	44	DNU	72	DQ27	100	DQ44	128	CKE0	156	DQ59
17	DQ13	45	CS2#	73	V _{CC}	101	DQ45	129	*CS3#	157	V _{CC}
18	V _{CC}	46	DQM2	74	DQ28	102	V _{CC}	130	DQM6	158	DQ60
19	DQ14	47	DQM3	75	DQ29	103	DQ46	131	DQM7	159	DQ61
20	DQ15	48	DNU	76	DQ30	104	DQ47	132	*A13	160	DQ62
21	CB0	49	V _{CC}	77	DQ31	105	CB4	133	V _{CC}	161	DQ63
22	CB1	50	NC	78	V _{SS}	106	CB5	134	NC	162	V _{SS}
23	V _{SS}	51	NC	79	CLK2	107	V _{SS}	135	NC	163	*CLK3
24	NC	52	CB2	80	NC	108	NC	136	CB6	164	NC
25	NC	53	CB3	81	NC	109	NC	137	CB7	165	**SA0
26	V _{CC}	54	V _{SS}	82	**SDA	110	V _{CC}	138	V _{SS}	166	**SA1
27	WE#	55	DQ16	83	**SCL	111	CAS#	139	DQ48	167	**SA2
28	DQM0	56	DQ17	84	V _{CC}	112	DQM4	140	DQ49	168	V _{CC}

PIN NAMES

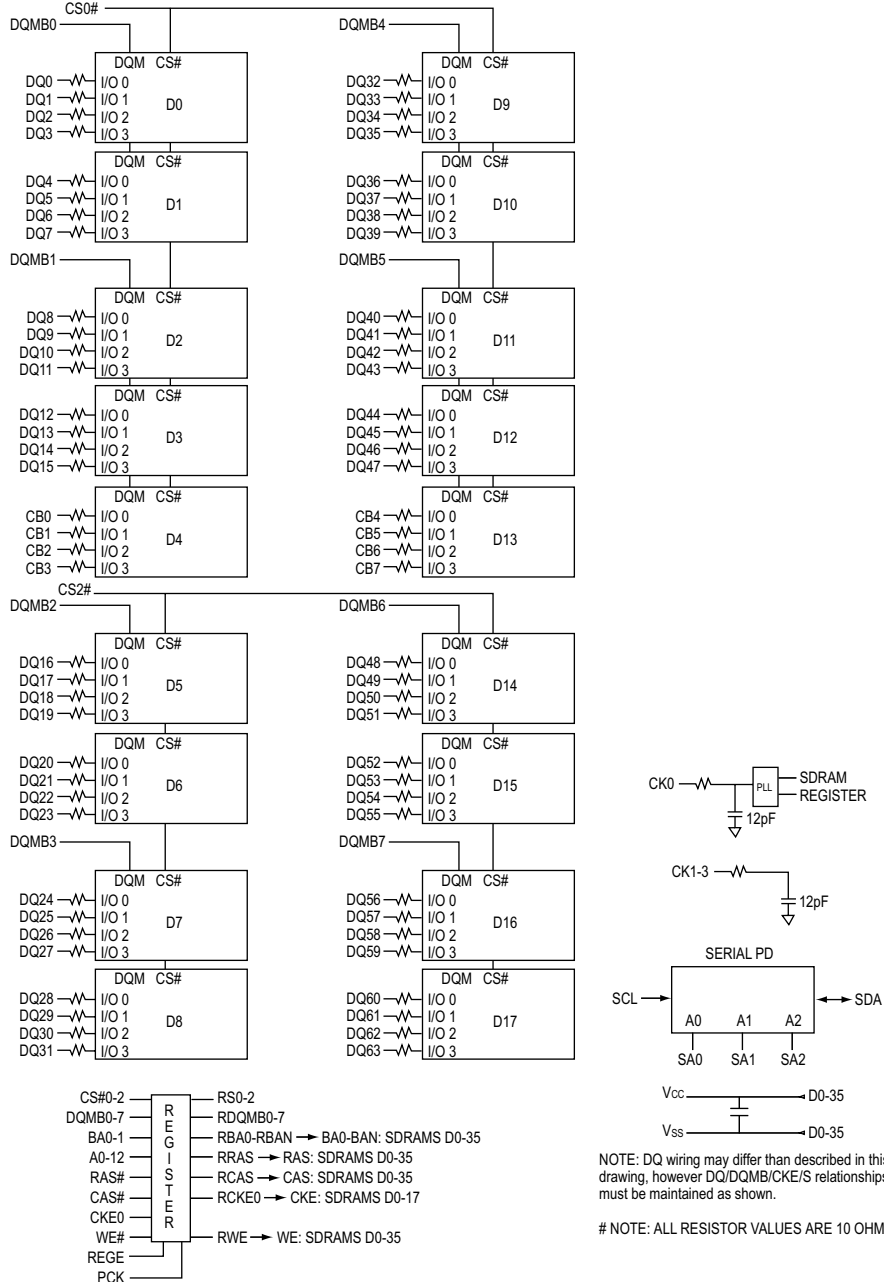
A0 – A12	Address input (Multiplexed)
BA0-1	Select Bank
DQ0-63	Data Input/Output
CB0-7	Check bit (Data-in/data-out)
CLK0	Clock input
CKE0	Clock Enable input
CS0#,CS2#	Chip select Input
RAS#	Row Address Strobe
CAS#	Column Address Strobe
WE#	Write Enable
DQM0-7	DQM
V _{CC}	Power Supply (3.3V)
V _{SS}	Ground
*VREF	Power supply for reference
REGE	Register Enable
SDA	Serial data I/O
SCL	Serial clock
SA0-2	Address in EEPROM
DNU	Do not use
NC	No Connect

* These pins are not used in this module.

** These pins should be NC in the system which does not support SPD.



FUNCTIONAL BLOCK DIAGRAM





ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Units
Voltage on any pin relative to Vss	V _{IN} , V _{OUT}	-1.0 ~ 4.6	V
Voltage on Vcc supply relative to Vss	V _{CC} , V _{CCQ}	-1.0 ~ 4.6	V
Storage Temperature	T _{STG}	-55 ~ +150	°C
Power Dissipation	P _D	36	W
Short Circuit Current	I _{OS}	50	mA

Note: Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded.
 Functional operation should be restricted to recommended operating condition.
 Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS

Voltage Referenced to: V_{SS} = 0V, 0°C ≤ T_A ≤ 70°

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply Voltage	V _{CC}	3.0	3.3	3.6	V	
Input High Voltage	V _{IH}	2.0	3.0	V _{CCQ} +0.3	V	1
Input Low Voltage	V _{IL}	-0.3	—	0.8	V	2
Output High Voltage	V _{OH}	2.4	—	—	V	I _{OH} = -2mA
Output Low Voltage	V _{OL}	—	—	0.4	V	I _{OL} = -2mA
Input Leakage Current	I _{LI}	-10	—	10	µA	3

Note: 1. V_{IH} (max)= 5.6V AC. The overshoot voltage duration is ≤ 3ns.
 2. V_{IL} (min)= -2.0V AC. The undershoot voltage duration is ≤ 3ns.
 3. Any input 0V ≤ V_{IN} ≤ V_{CCQ}
 Input leakage currents include Hi-Z output leakage for all bi-directional buffers with Tri-State outputs.

CAPACITANCE

T_A = 25 °C, f = 1MHz, V_{CC} = 3.3V, V_{REF} = 1.4V ± 200mV

Parameter	Symbol	Max	Unit
Input Capacitance (A0-A12)	C _{IN1}	9	pF
Input Capacitance (RAS#,CAS#,WE#)	C _{IN2}	9	pF
Input Capacitance (CKE0)	C _{IN3}	9	pF
Input Capacitance (CLK0)	C _{IN4}	17	pF
Input Capacitance (CS0#,CS2#)	C _{IN5}	9	pF
Input Capacitance (DQM0-DQM7)	C _{IN6}	7	pF
Input Capacitance (BA0-BA1)	C _{IN7}	9	pF
Data input/output capacitance (DQ0-DQ63)	C _{OUT}	10	pF
Data input/output capacitance (CB0-CB7)	C _{OUT1}	10	pF



OPERATING CURRENT CHARACTERISTICS

$V_{CC} = 3.3V, 0^{\circ}C \leq T_A \leq 70^{\circ}C$

Parameters	Symbol	Conditions	Versions	Units	Note
			133/100		
Operating Current (One bank active)	I _{CC1}	Burst Length = 1 t _{RC} ≥ t _{RC(min)} I _{OL} = 0mA	3885	mA	1
Precharge Standby Current in Power Down Mode	I _{CC2P}	C _{KE} ≤ V _{IL(max)} , t _{CC} = 10ns	395	mA	
	I _{CC2PS}	C _{KE} & CLK ≤ V _{IL(max)} , t _{CC} = ∞	330	mA	
Precharge Standby Current in Non-Power Down Mode	I _{CC2N}	C _{KE} ≥ V _{IH(min)} , CS ≥ V _{IH(min)} , t _{CC} = 10ns Input signals are charged one time during 20	825	mA	
	I _{CC2NS}	C _{KE} ≥ V _{IH(min)} , CLK ≤ V _{IL(max)} , t _{CC} = ∞ Input signals are stable	275	mA	
Active standby current in power-down mode	I _{CC3P}	C _{KE} ≥ V _{IL(max)} , t _{CC} = 10ns	465	mA	
	I _{CC3PS}	C _{KE} & CLK ≤ V _{IL(max)} , t _{CC} = ∞	372	mA	
Active standby in current non power- down mode	I _{CC3N}	C _{KE} ≥ V _{IH(min)} , CS ≥ V _{IH(min)} , t _{CC} = 10ns Input signals are charged one time during 20ns	1185	mA	
	I _{CC3NS}	C _{KE} ≥ V _{IH(min)} , CLK ≤ V _{IL(max)} , t _{CC} = ∞ input signals are stable	830	mA	
Operating current (Burst mode)	I _{CC4}	I _O = mA Page burst 4 Banks activated t _{CCD} = 2CLK	3885	mA	1
Refresh current	I _{CC5}	t _{RC} ≥ t _{RC(min)}	6225	mA	2
Self refresh current	I _{CC6}	C _{KE} ≤ 0.2V	411	mA	

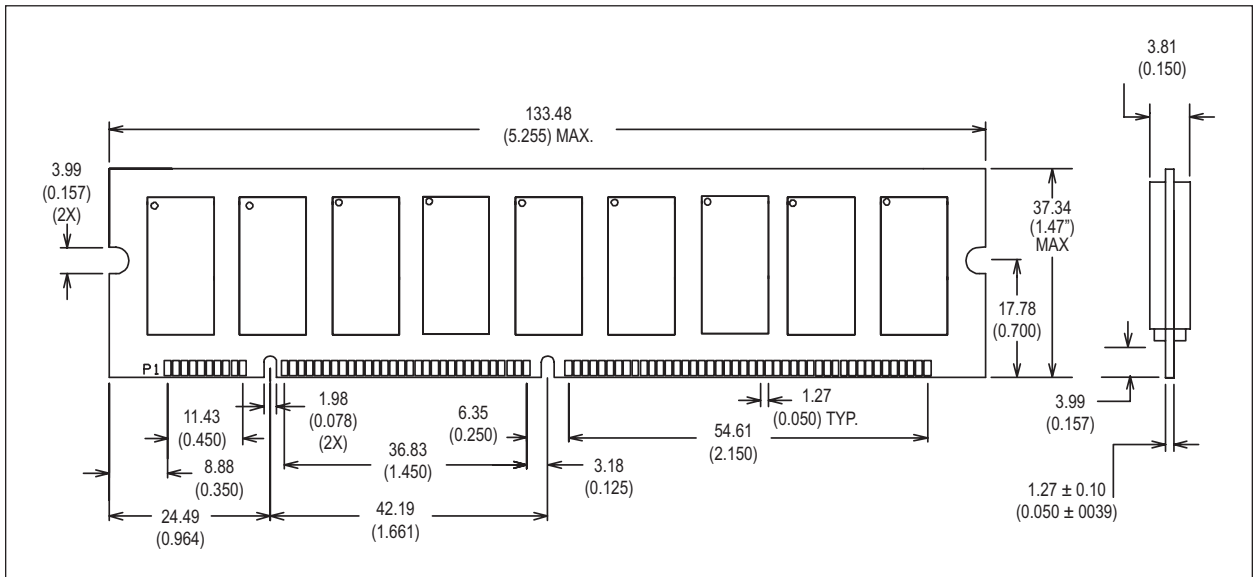
- Notes: 1. Measured with outputs open.
 2. Refresh period is 64ms.
 3. Unless otherwise noticed, input swing level is CMOS (V_{IH}/V_{IL} = V_{CC}/V_{SS0})



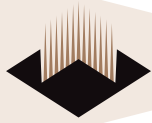
ORDERING INFORMATION

Part Number	Speed	CAS Latency	Height*
W3DG72127V10D2	100MHz	CL=2	37.34 (1.47")
W3DG72127V7D2	133MHz	CL=2	37.34 (1.47")
W3DG72127V75D2	133MHz	CL=3	37.34 (1.47")

PACKAGE DIMENSIONS



* ALL DIMENSIONS ARE IN MILLIMETERS AND (INCHES)



Document Title

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Revision History

Rev #	History	Release Date	Status
Rev A	Created Datasheet	3-26-02	Advanced
Rev 0	Changed Advanced to Final	9-19-02	Final
Rev 1	Changed mechanical package dimensions	1-22-04	Final
Rev 2	2.1 Updated Cap & IDD specs	6-10-04	Final
	2.2 Added Package Dimensions in millimeters		
	2.3 Removed "ED" from part number		