256MB – 2x16Mx64 DDR SDRAM UNBUFFERED

FEATURES

- DDR266 and DDR333
- Double-data-rate architecture
- Bi-directional data strobes (DQS)
- Differential clock inputs (CK & CK#)
- Programmable Read Latency 2,2.5 (clock)
- Programmable Burst Length (2,4,8)
- Programmable Burst type (sequential & interleave)
- Edge aligned data output, center aligned data input.
- Auto and self refresh
- Serial presence detect
- Dual Rank
- Power supply: 2.5V ± 0.2V
- JEDEC 184 pin DIMM package
  - JD3 PCB height: 30.48 (1.20")

NOTE: Consult factory for availability of:
- RoHS compliant products
- Vendor source control options
- Industrial temperature option

DESCRIPTION

The W3EG6433S is a 2x16Mx64 Double Data Rate SDRAM memory module based on 256Mb DDR SDRAM component. The module consists of sixteen 16Mx8 DDR SDRAMs in 66 pin TSOP packages mounted on a 184 pin FR4 substrate.

Synchronous design allows precise cycle control with the use of system clock. Data I/O transactions are possible on both edges and Burst Lengths allow the same device to be useful for a variety of high bandwidth, high performance memory system applications.

* This product is under development, is not qualified or characterized and is subject to change without notice.

OPERATING FREQUENCIES

	DDR333@CL=2.5	DDR266 @CL=2	DDR266 @CL=2	DDR266 @CL=2.5
Clock Speed	166MHz	133MHz	133MHz	133MHz
CL-t_{RCD}-t_{RP}	2.5-3-3	2-2-2	2-3-3	2.5-3-3

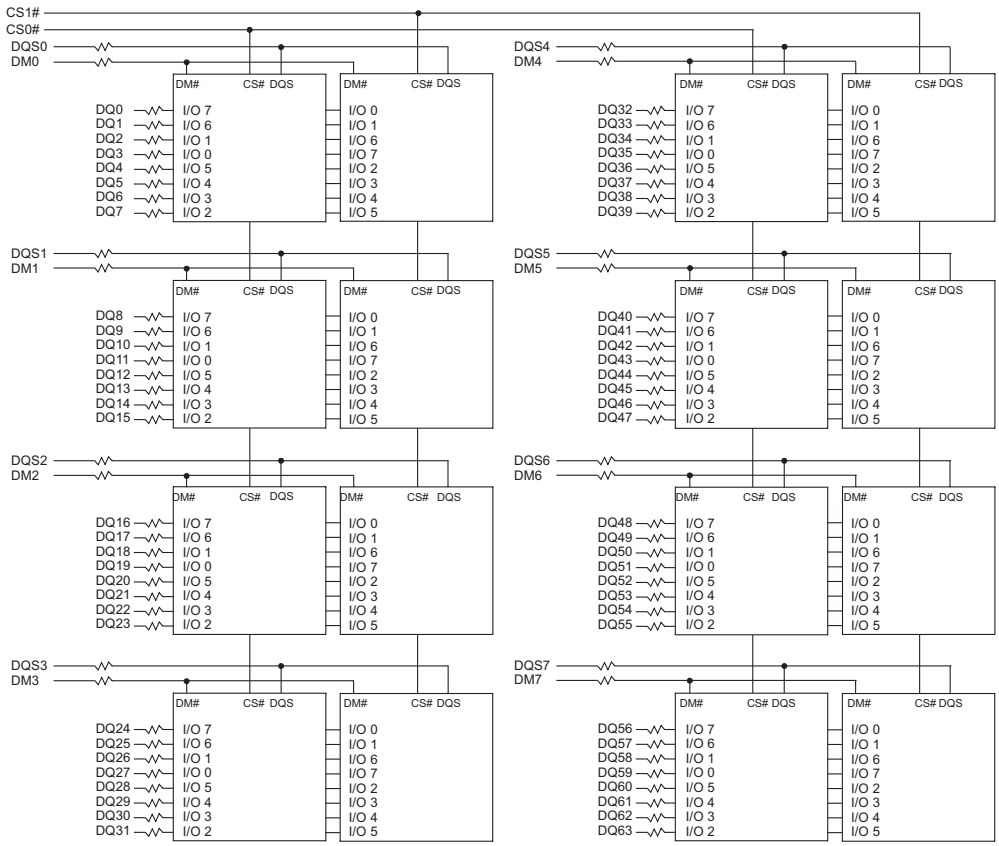
PIN CONFIGURATION

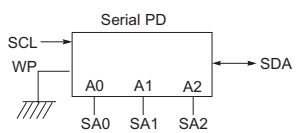
PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL
1	V_{REF}	47	NC	93	V_{SS}	139	V_{SS}
2	DQ0	48	A0	94	DQ4	140	NC
3	V_{SS}	49	NC	95	DQ5	141	A10
4	DQ1	50	V_{SS}	96	V_{CCQ}	142	NC
5	DQS0	51	NC	97	DQM0	143	V_{CCQ}
6	DQ2	52	BA1	98	DQ6	144	NC
7	V_{CC}	53	DQ32	99	DQ7	145	V_{SS}
8	DQ3	54	V_{CCQ}	100	V_{SS}	146	DQ36
9	NC	55	DQ33	101	NC	147	DQ37
10	NC	56	DQS4	102	NC	148	V_{CC}
11	V_{SS}	57	DQ34	103	NC	149	DM4
12	DQ8	58	V_{SS}	104	V_{CCQ}	150	DQ38
13	DQ9	59	BA0	105	DQ12	151	DQ39
14	DQS1	60	DQ35	106	DQ13	152	V_{SS}
15	V_{CCQ}	61	DQ40	107	DQM1	153	DQ44
16	CK1	62	V_{CCQ}	108	V_{CC}	154	RAS#
17	CK1#	63	WE#	109	DQ14	155	DQ45
18	V_{SS}	64	DQ41	110	DQ15	156	V_{CCQ}
19	DQ10	65	CAS#	111	CKE1	157	CS0#
20	DQ11	66	V_{SS}	112	V_{CCQ}	158	CS1#
21	CKE0	67	DQS5	113	NC	159	DM5
22	V_{CCQ}	68	DQ42	114	DQ20	160	V_{SS}
23	DQ16	69	DQ43	115	NC	161	DQ46
24	DQ17	70	V_{CC}	116	V_{SS}	162	DQ47
25	DQS2	71	NC	117	DQ21	163	NC
26	V_{SS}	72	DQ48	118	A11	164	V_{CCQ}
27	A9	73	DQ49	119	DM2	165	DQ52
28	DQ18	74	V_{SS}	120	V_{CC}	166	DQ53
29	A7	75	CK2#	121	DQ22	167	NC
30	V_{CCQ}	76	CK2	122	A8	168	V_{CC}
31	DQ19	77	V_{CCQ}	123	DQ23	169	DQM6
32	A5	78	DQS6	124	V_{SS}	170	DQ54
33	DQ24	79	DQ50	125	A6	171	DQ55
34	V_{SS}	80	DQ51	126	DQ28	172	V_{CCQ}
35	DQ25	81	V_{SS}	127	DQ29	173	NC
36	DQS3	82	V_{CCID}	128	V_{CCQ}	174	DQ60
37	A4	83	DQ56	129	DM3	175	DQ61
38	V_{CC}	84	DQ57	130	A3	176	V_{SS}
39	DQ26	85	V_{CC}	131	D30	177	DM7
40	DQ27	86	DQS7	132	V_{SS}	178	DQ62
41	A2	87	DQ58	133	DQ31	179	DQ63
42	V_{SS}	88	DQ59	134	NC	180	V_{CCQ}
43	A1	89	V_{SS}	135	NC	181	SA0
44	NC	90	NC	136	V_{CCQ}	182	SA1
45	NC	91	SDA	137	CK0	183	SA2
46	V_{CC}	92	SCL	138	CK0#	184	V_{CCSPD}

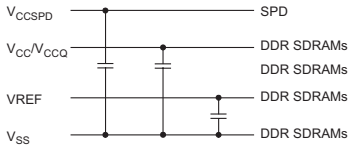
PIN NAMES

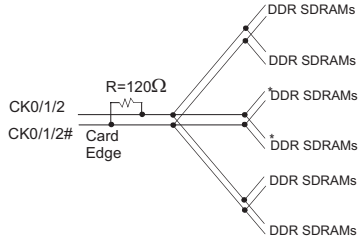
A0-A11	Address input (Multiplexed)
BA0-BA1	Bank Select Address
DQ0-DQ63	Data Input/Output
DQS0-DQS8	Data Strobe Input/Output
CK0, CK1, CK2	Clock Input
CK0#CK1#, CK2#	Clock Input
CKE0, CKE1	Clock Enable input
CS0#, CS1#	Chip Select Input
RAS#	Row Address Strobe
CAS#	Column Address Strobe
WE#	Write Enable
DM0-DM7	Data-in-mask
V_{CC}	Power Supply
V_{CCQ}	Power Supply for DQS
V_{SS}	Ground
V_{REF}	Power Supply for Reference
V_{CCSPD}	Serial EEPROM Power Supply
SDA	Serial data I/O
SCL	Serial clock
SA0-SA2	Address in EEPROM
NC	No Connect

FUNCTIONAL BLOCK DIAGRAM









BA0 - BA1 → BA0-BA1 : DDR SDRAMs
A0 - A11 → A0-A11 : DDR SDRAMs
RAS# → RAS# DDR SDRAMs
CAS# → CAS# : DDR SDRAMs
CKE0/1 → CKE : DDR SDRAMs
WE# → WE# DDR SDRAMs

* Clock Wiring	
Clock Input	DDR SDRAMs
*CK0/CK0#	4 DDR SDRAMs
*CK1/CK1#	6 DDR SDRAMs
*CK2/CK2#	6 DDR SDRAMs

*Clock Net Wiring

Notes :
1. DQ-to-I/O wiring is shown as recommended but may be changed.
2. DQ/DQS/DM/CKE/CS# relationships must be maintained as shown.
3. DQ, DQS, DM#/DQS# resistors: 22 Ohms + 5%.
4. BAx, Ax, RAS#, CAS#, WE# resistors: 3 Ohms + 5%.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Units
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	-0.5 to 3.6	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}, V_{CCQ}	-1.0 to 3.6	V
Storage Temperature	T_{STG}	-55 to +150	°C
Power Dissipation	P_D	24	W
Short Circuit Current	I_{OS}	50	mA

Note: Permanent device damage may occur if 'ABSOLUTE MAXIMUM RATINGS' are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability

DC OPERATING CONDITIONS

Recommended perating conditions (Voltage referenced to V_{SS}=0V, TA=0 to 70°C)

Parameter	Symbol	Min	Max	Unit	Note
Supply Voltage (for device with a nominal V_{CC} of 2.5V)	V_{CC}	2.3	2.7	V	
I/O Supply Voltage	V_{CCQ}	2.3	2.7	V	
I/O Reference Voltage	V_{REF}	0.49*V_{CCQ}	0.51*V_{CCQ}	V	1
I/OTermination Voltage	V_{TT}	V_{REF}-0.04	V_{REF}+0.04	V	2
Input Logic High Voltage	V_{IH}	V_{REF} + 0.15	V_{CCQ} + 0.3	V	
Input Logic Low Voltage	V_{IL}	-0.3	V_{REF} -0.15	V	
Input Voltage Level, CK and CK# Inputs	$V_{IN(DC)}$	-0.3	V_{CCQ} + 0.3	V	
Input Differential Voltage, CK and CK# Inputs	$V_{ID(DC)}$	0.36	V_{CCQ} + 0.6	V	3
V-I Matching: Pullup to Pulldown Current Ratio	VI(Ratio)	0.71	1.4	-	4
Input leakage current	I_I	-2	2	uA	
Output leakage current	I_{OZ}	-5	5	uA	
Output High Current(Normal strengh driver); V_{OUT} = V_{TT} = 0.84V	I_{OH}	-16.8		uA	
Output High Current(Normal strengh driver); V_{OUT} = V_{TT} = 0.84V	I_{OL}	16.8		uA	
Output High Current(Half strengh driver); V_{OUT} = V_{TT} = 0.45V	V_{OH}	-9		uA	
Output High Current(Half strengh driver); V_{OUT} = V_{TT} = 0.45V	V_{OL}	9		uA	

NOTES:
1. V_{REF} is expected to be equal to 0.5*V_{CCQ} of the transmitting device, and to track variations in the dc level of same. Peak-to peak noise on V_{REF} may not exceed +/-2% of the dc value.
2. V_{TT} is not applied directly to the device. V_{TT} is a system supply for signal termination resistors, is expected to be set equal to V_{REF}, and must track variations in the DC level of V_{REF}.
3. V_{ID} is the magnitude of the difference between the input level on CK and the input level on CK#.
4. The ratio of the pullup current to the pulldown current is specified for the same temperature and voltage, over the entire temperature and voltage range, for device drain to source voltages from 0.25V to 1.0V. For a given output, it represents the maximum difference between pullup and pulldown drivers due to process variation. The full variation in the ratio of the maximum to minimum pullup and pulldown current will not exceed 1/7 for device drain to source voltages from 0.1 to 1.0.

CAPACITANCE

T_A = 25°C. f = 1MHz, V_{CC} = 2.5V

Parameter	Symbol	Max	Unit
Input Capacitance (A0-A11)	C_{IN1}	81	pF
Input Capacitance (RAS#,CAS#,WE#)	C_{IN2}	81	pF
Input Capacitance (CKE0, CKE1, CKE2)	C_{IN3}	50	pF
Input Capacitance (CLK0, CLK1, CLK2)	C_{IN4}	34	pF
Input Capacitance (CS0#, CS1#)	C_{IN5}	50	pF
Input Capacitance (DMO ~ DM7)	C_{IN6}	12	pF
Input Capacitance (BA0-BA1)	C_{IN7}	81	pF
Data input/output capacitance (DQ0-DQ63)(DQS)	C_{OUT}	12	pF
Data input/output capacitance (CB0-CB7)	C_{OUT}	-	pF

I_{DD} SPECIFICATIONS AND TEST CONDITIONS

$0°C \leq T_A \leq 70°C$, V_{CCQ} = 2.5V ± 0.2V, V_{CC} = 2.5V ± 0.2V

Includes DDR SDRAM component only

Parameter	Symbol	Conditions	DDR333@CL=2.5 Max	DDR266@CL=2 Max	DDR266@CL=2/2.5 Max	Units
Operating Current	I_{DD0}	One device bank; Active - Precharge; t_{RC}=t_{RC} (MIN); t_{CK}=t_{CK} (MIN); DQ,DM and DQS inputs changing once per clock cycle; Address and control inputs changing once every two cycles.	680	640	640	mA
Operating Current	I_{DD1}	One device bank; Active-Read-Precharge Burst = 2; t_{RC}=t_{RC} (MIN); t_{CK}=t_{CK} (MIN); I_{OUT} = 0mA; Address and control inputs changing once per clock cycle.	880	800	800	mA
Precharge Power-Down Standby Current	I_{DD2P}	All device banks idle; Power-down mode; t_{CK}=t_{CK} (MIN); CKE=(low)	24	24	24	rnA
Idle Standby Current	I_{DD2F}	CS# = High; All device banks idle; t_{CK}=t_{CK} (MIN); CKE = high; Address and other control inputs changing once per clock cycle. V_{IN} = V_{REF} for DQ, DQS and DM.	200	180	180	mA
Active Power-Down Standby Current	I_{DD3P}	One device bank active; Power-Down mode; t_{CK} (MIN); CKE=(low)	240	200	200	mA
Active Standby Current	I_{DD3N}	CS# = High; CKE = High; One device bank; Active-Precharge; t_{RC}=t_{RAS} (MAX); t_{CK}=t_{CK} (MIN); DQ, DM and DQS inputs changing twice per clock cycle; Address and other control inputs changing once per clock cycle.	360	320	320	mA
Operating Current	I_{DD4R}	Burst = 2; Reads; Continuous burst; One device bank active; Address and control inputs changing once per clock cycle; T_{CK}= T_{CK} (MIN); I_{OUT} = 0mA.	1,120	960	960	mA
Operating Current	I_{DD4W}	Burst = 2; Writes; Continuous burst; One device bank active; Address and control inputs changing once per clock cycle; t_{CK}=t_{CK} (MIN); DQ,DM and DQS inputs changing once per clock cycle.	1,160	1,000	1,000	rnA
Auto Refresh Current	I_{DD5}	t_{RC} = t_{RC} (MIN)	1,320	1,240	1,240	mA
Self Refresh Current	I_{DD6}	CKE ≤ 0.2V	16	16	16	mA
Operating Current	I_{DD7A}	Four bank interleaving Reads (BL=4) with auto precharge with t_{RC}=t_{RC} (MIN); t_{CK}=t_{CK} (MIN); Address and control inputs change only during Active Read or Write commands.	2,400	2,000	2,000	mA

NOTES:

- Module I_{DD} was calculated on the basis of component I_{DD} and can be different measured according to dq hearing cap.
- I_{DD} specification is based on **SAMSUNG** components. Other DRAM manufactures specification may be different.

DDR SDRAM COMPONENT ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

AC Characteristics			335 (DDR333@CL=2.5)		262 (DDR266@CL=2.0)		263 (DDR266@CL=2.0)		265 (DDR266@CL=2.5)			
Parameter		**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Units**	**Notes**
Row cycle time		t_{RC}	60		60		65		65		ns	
Refresh row cycle time		t_{RFC}	72		75		75		75		ns	
Row active time		t_{RAS}	42	70K	45	120K	45	120K	45	120K	ns	
RAS to CAS delay		t_{RCD}	18		15		20		20		ns	
Row precharge time		t_{RP}	18		15		20		20		ns	
Row active to Row active delay		t_{RRD}	12		15		15		15		ns	
Write recovery time		t_{WR}	15		15		15		15		ns	
Last data in to Read command		t_{WTD}	1		1		1		1		t_{CK}	
Col. address to Col. address delay		t_{CCD}	1		1		1		1		t_{CK}	
Clock cycle time	CL=2.0	t_{CK}	7.5	12	7.5	12	7.5	12	10	12	ns	
	CL=2.5		6	12	7.5	12	7.5	12	7.5	12	ns	
Clock high level width		t_{CH}	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	t_{CK}	
Clock low level width		t_{CL}	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	t_{CK}	
DQS-out access time from CK/CK		t_{DQSCK}	-0.6	+0.6	-0.75	+0.75	-0.75	+0.75	-0.75	+0.75	ns	
Output data access time from CK/CK		t_{AC}	-0.7	+0.7	-0.75	+0.75	-0.75	+0.75	-0.75	+0.75	ns	
Data strobe edge to output data edge		t_{DQSQ}	-	0.45	-	0.5	-	0.5	-	0.5	ns	12
Read Preamble		t_{RPRE}	0.9	1.1	0.9	1.1	0.9	1.1	0.9	1.1	t_{CK}	
Read Postamble		t_{RPST}	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	t_{CK}	
CK to valid DQS-in		t_{DQSS}	0.75	1.25	0.75	1.25	0.75	1.25	0.75	1.25	t_{CK}	
DQS-in setup time		t_{WPRES}	0		0		0		0		ns	3
DQS-in hold time		t_{WPRE}	0.25		0.25		0.25		0.25		t_{CK}	
DQS falling edge to CK rising-setup time		t_{DSS}	0.2		0.2		0.2		0.2		t_{CK}	
DQS falling edge from Ck rising-hold time		t_{DSH}	0.2		0.2		0.2		0.2		t_{CK}	
DQS-in high level width		t_{DQSH}	0.35		0.35		0.35		0.35		t_{CK}	
DQS-in low level width		t_{DQSL}	0.35		0.35		0.35		0.35		t_{CK}	
DQS-in cycle time		t_{DSC}	0.9	1.1	0.9	1.1	0.9	1.1	0.9	1.1	t_{CK}	
Address and Control Input setup time (fast)		t_{IS}	0.75		0.9		0.9		0.9		ns	i,5.7~9
Address and Control Input hold time (fast)		t_{IH}	0.75		0.9		0.9		0.9		ns	i,5.7~9
Address and Control Input setup time (slow)		t_{IS}	0.8		1.0		1.0		1.0		ns	i,6~9
Address and Control Input setup time (slow)		t_{IH}	0.8		1.0		1.0		1.0		ns	i,6~9
Data-out high impedence time from CK/CK		t_{HZ}		+0.7		+0.75		+0.75		+0.75	ns	1
Data-out high impedence time from CK/CK		t_{LZ}	-0.7	+0.7	-0.75	+0.75	-0.75	+0.75	-0.75	+0.75	ns	1
Input Slew Rate (for input only pins)		$t_{SL(I)}$	0.5		0.5		0.5		0.5		V/ns	
Input Slew Rate (for I/O pins)		$t_{SL(IO)}$	0.5		0.5		0.5		0.5		V/ns	

DDR SDRAM COMPONENT ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (continued)

AC Characteristics		335 (DDR333@CL=2.5)		262 (DDR266@CL=2.0)		263 (DDR266@CL=2.0)		265 (DDR266@CL=2.5)			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Units**	**Notes**
Output Slew Rate (x4,x8)	$t_{SL(O)}$	1.0	4.5	1.0	4.5	1.0	4.5	1.0	4.5	V/ns	
Output Slew Rate Matching Ratio (rise to fall)	t_{SLMR}	0.67	1.5	0.67	1.5	0.67	1.5	0.67	1.5	ns	
Mode register set cycle time	t_{MRD}	12		15		15		15		ns	j, k
DQ & DM setup time to DQS	t_{DS}	0.5		0.5		0.5		0.5		ns	j, k
DQ & DM hold time to DQS	t_{DH}	0.45		0.5		0.5		0.5		ns	8
Control & Address input pulse width	t_{IPW}	2.2		2.2		2.2		2.2		ns	8
DQ & DM input pulse width	t_{DIPW}	1.75		1.75		1.75		1.75		ns	
Power down exit time	t_{RDEX}	6		7.5		7.5		7.5		ns	
Exit self refresh to non-Read command	t_{XSRD}	75		75		75		75		ns	
Exit self refresh to read command	t_{XSRD}	200		200		200		200		t_{CK}	
Refreash interval time	t_{REFI}		15.6		15.6		15.6		15.6	us	4
Output DQS valid window	t_{QH}	t_{HP}-t_{QHS}	-	t_{HP}-t_{QHS}	-	t_{HP}-t_{QHS}	-	t_{HP}-t_{QHS}		ns	11
Clock half period	t_{QH}	t_{CLmin} or t_{chmin}	-	t_{CLmin} or t_{chmin}	-	t_{CLmin} or t_{chmin}	-	t_{CLmin} or t_{chmin}		ns	10, 11
Data hold skew factor	t_{QHS}		0.55		0.75		0.75		0.75	ns	11
DQS write postamble time	t_{WPST}	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	t_{CK}	2
Active to Read with Auto precharge command	t_{RAP}	18		20		20		20			
Autoprecharge write recovery & Precharge time	t_{XSNR}	t_{WR}/t_{CK} + t_{RP}/t_{CK})		t_{WR}/t_{CK} + t_{RP}/t_{CK})		t_{WR}/t_{CK} + t_{RP}/t_{CK})		t_{WR}/t_{CK} + t_{RP}/t_{CK})		t_{CK}	13

Notes

1. t_{HZ} and t_{LZ} transitions occur in the same access time windows as valid data transitions. These parameters are not referenced to a specific voltage level but specify when the device output in no longer driving (HZ), or begins driving (LZ).
2. The maximum limit for this parameter is not a device limit. The device will operate with a greater value for this parameter, but system performance (bus turnaround) will degrade accordingly.
3. The specific requirement is that DQS be valid (HIGH, LOW, or at some point on a valid transition) on or before this CK edge. A valid transition is defined as monotonic and meeting the input slew rate specifications of the device. When no writes were previously in progress on the bus, DQS will be transitioning from High- Z to logic LOW. If a previous write was in progress, DQS could be HIGH, LOW, or transitioning from HIGH to LOW at this time, depending on t_{DQSS}.
4. A maximum of eight AUTO REFRESH commands can be posted to any given DDR SDRAM device.
5. For command/address input slew rate ≥ 1.0 V/ns.
6. For command/address input slew rate ≥ 0.5 V/ns and > 1.0 V/ns
7. For CK & CK# slew rate ≥ 1.0 V/ns.
8. These parameters guarantee device timing, but they are not necessarily tested on each device. They may be guaranteed by device design or tester correlation.
9. Slew Rate is measured between V_{OH}(ac) and V_{OL}(ac).
10. Min (t_{CL}, t_{CH}) refers to the smaller of the actual clock low time and the actual clock high time as provided to the device (i.e. this value can be greater than the minimum specification limits for t_{CL} and t_{CH}. For example, t_{CL} and t_{CH} are = 50% of the period, less the half period jitter (t_{JIT}(HP)) of the clock source, and less the half period jitter due to crosstalk (t_{JIT}(crosstalk)) into the clock traces.
11. $t_{QH} = t_{HP} - t_{QHS}$, where:
t_{HP} = minimum half clock period for any given cycle and is defined by clock high or clock low (t_{CH}, t_{CL}). t_{QHS} accounts for 1) The pulse duration distortion of on-chip clock circuits; and 2) The worst case push-out of DQS on one transition followed by the worst case pull-in of DQ on the next transition, both of which are, separately, due to data pin skew and output pattern effects, and p-channel to n-channel variation of the output drivers.
12. t_{DQSQ}
Consists of data pin skew and output pattern effects and p-channel to n-channel variation of the output drivers for any given cycle.
13. $t_{DAL} = (t_{WR}/t_{CK}) + (t_{RP}/t_{CK})$
For each of the terms above, if not already an integer, round to the next highest integer. Example: For DDR266 at CL=2.5 and t_{CK}=7.5ns t_{DAL} = (15 ns / 7.5 ns) + (20 ns/ 7.5ns) = (2) + (3) t_{DAL} = 5 clocks

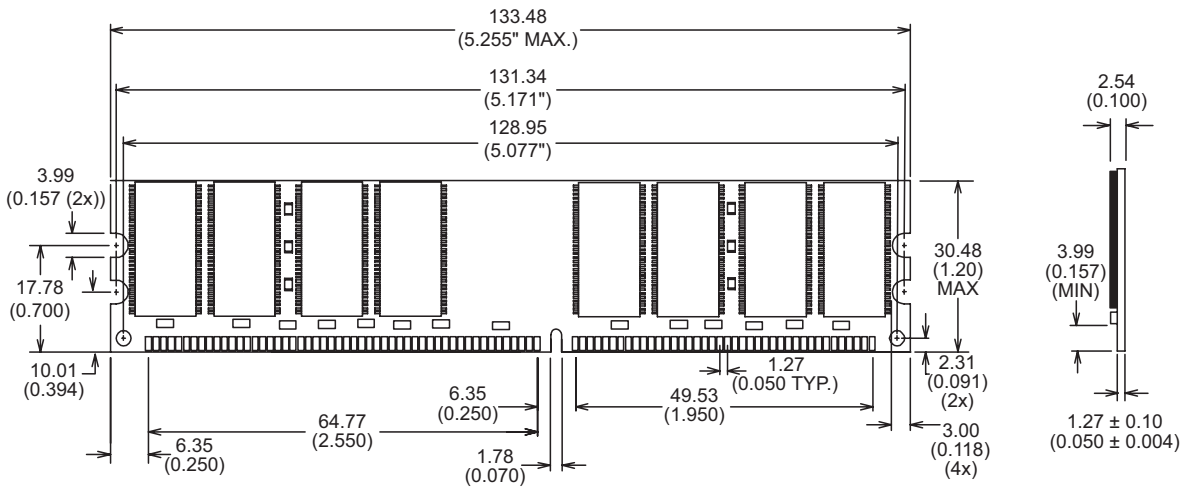
ORDERING INFORMATION FOR JD3

Part Number	Speed	CAS Latency	t_{RCD}	t_{RP}	Height*
W3EG6433S335JD3	166MHz/333Mb/s	2.5	3	3	30.48 (1.20")
W3EG6433S263JD3	133MHz/266Mb/s	2	2	2	30.48 (1.20")
W3EG6433S263JD3	133MHz/266Mb/s	2	3	3	30.48 (1.20")
W3EG6433S265JD3	133MHz/266Mb/s	2.5	3	3	30.48 (1.20")

NOTES:

- Consult Factory for availability of RoHS compliant products. (G = RoHS Compliant)
- Vendor specific part numbers are used to provide memory components source control. The place holder for this is shown as lower case "x" in the part numbers above and is to be replaced with the respective vendors code. Consult factory for qualified sourcing options. (M = Micron, S = Samsung & consult factory for others)
- Consult factory for availability of industrial temperature (-40°C to 85°C) option

PACKAGE DIMENSIONS FOR JD3



* ALL DIMENSIONS ARE IN MILLIMETERS AND (INCHES)

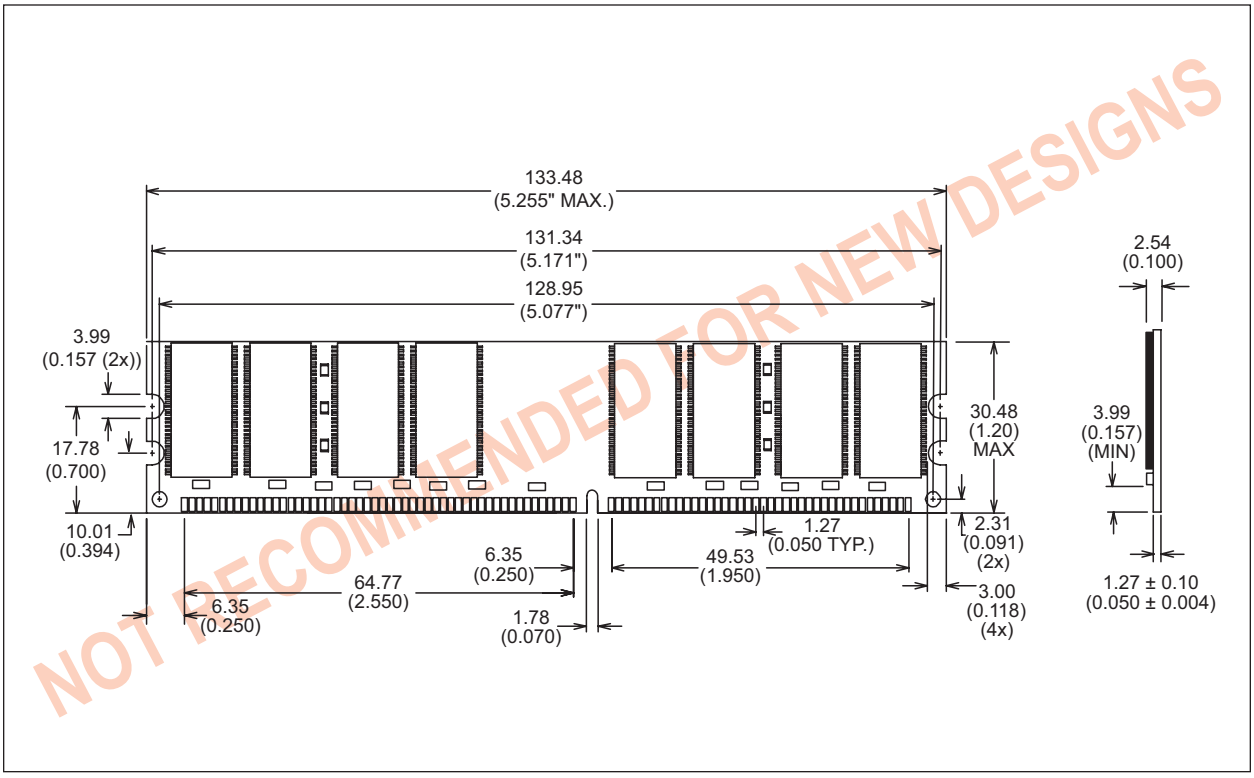
ORDERING INFORMATION FOR D3

Part Number	Speed	CAS Latency	t_{RCD}	t_{RP}	Height*
W3EG6433S335D3	166MHz/333Mb/s	2.5	3	3	30.48 (1.20")
W3EG6433S262D3	133MHz/266Mb/s	2	2	2	30.48 (1.20")
W3EG6433S263D3	133MHz/266Mb/s	2	3	3	30.48 (1.20")
W3EG6433S265D3	133MHz/266Mb/s	2.5	3	3	30.48 (1.20")

NOTES:

- Consult Factory for availability of RoHS compliant products. (G = RoHS Compliant)
- Vendor specific part numbers are used to provide memory components source control. The place holder for this is shown as lower case "x" in the part numbers above and is to be replaced with the respective vendors code. Consult factory for qualified sourcing options. (M = Micron, S = Samsung & consult factory for others)
- Consult factory for availability of industrial temperature (-40°C to 85°C) option

PACKAGE DIMENSIONS FOR D3



* ALL DIMENSIONS ARE IN MILLIMETERS AND (INCHES)

Document Title

256MB – 2x16Mx64 DDR SDRAM UNBUFFERED

Revision History

Rev #	History	Release Date	Status
Rev 1	1.1 Created Datasheet 1.2 Added lead-free and RoHS notes 1.3 Added AC specs 1.4 Moved from Advanced to Preliminary	12-04	Preliminary
Rev 2	2.1 Added JEDEC standard PCB 2.2 D3 option is "NOT RECOMMENDED FOR NEW DESIGNS" 2.3 Added lead-free and RoHS notes 2.4 Added source control notes 2.5 Added industrial temperature options	5-05	Preliminary
Rev 3	3.1 Update AC, I_{DD} and cap specs 3.2 Add 333MH speed	11-05	Preliminary