

# 512K x 32/256K x 32 Dual Array Synchronous Pipeline Burst NBL SRAM

## FEATURES

- Fast clock speed: 166, 150, 133, and 100MHz
- Fast access times: 3.5ns, 3.8ns, 4.2ns, and 5.0ns
- Fast OE# access times: 3.5ns, 3.8ns, 4.2ns, and 5.0ns
- Single +2.5V ± 5% power supply (V<sub>CC</sub>)
- Snooze Mode for reduced-standby power
- Individual Byte Write control
- Clock-controlled and registered addresses, data I/Os and control signals
- Burst control (interleaved or linear burst)
- Packaging:
  - 209-bump BGA package
- Low capacitive bus loading

## DESCRIPTION

The WED2ZLRSP01S, Dual Independent Array, NBL-SSRAM device employs high-speed, Low-Power CMOS silicon and is fabricated using an advanced CMOS process. WEDC's 24Mb, Sync Burst SRAM MCP integrates two totally independent arrays, the first organized as a 512K x 32, and the second a 256K x 32.

All Synchronous inputs pass through registers controlled by a positive edge triggered, single clock input per array. The NBL or No Bus Latency Memory provides 100% bus utilization, with no loss of cycles caused by change in modal operation (Write to Read/Read to Write). All inputs except for Asynchronous Output Enable and Burst Mode control are synchronized on the positive or rising edge of Clock. Burst order control must be tied either HIGH or LOW, Write cycles are internally self-timed, and writes are initiated on the rising edge of clock. This feature eliminates the need for complex off-chip write pulse generation and proved increased timing flexibility for incoming signals.

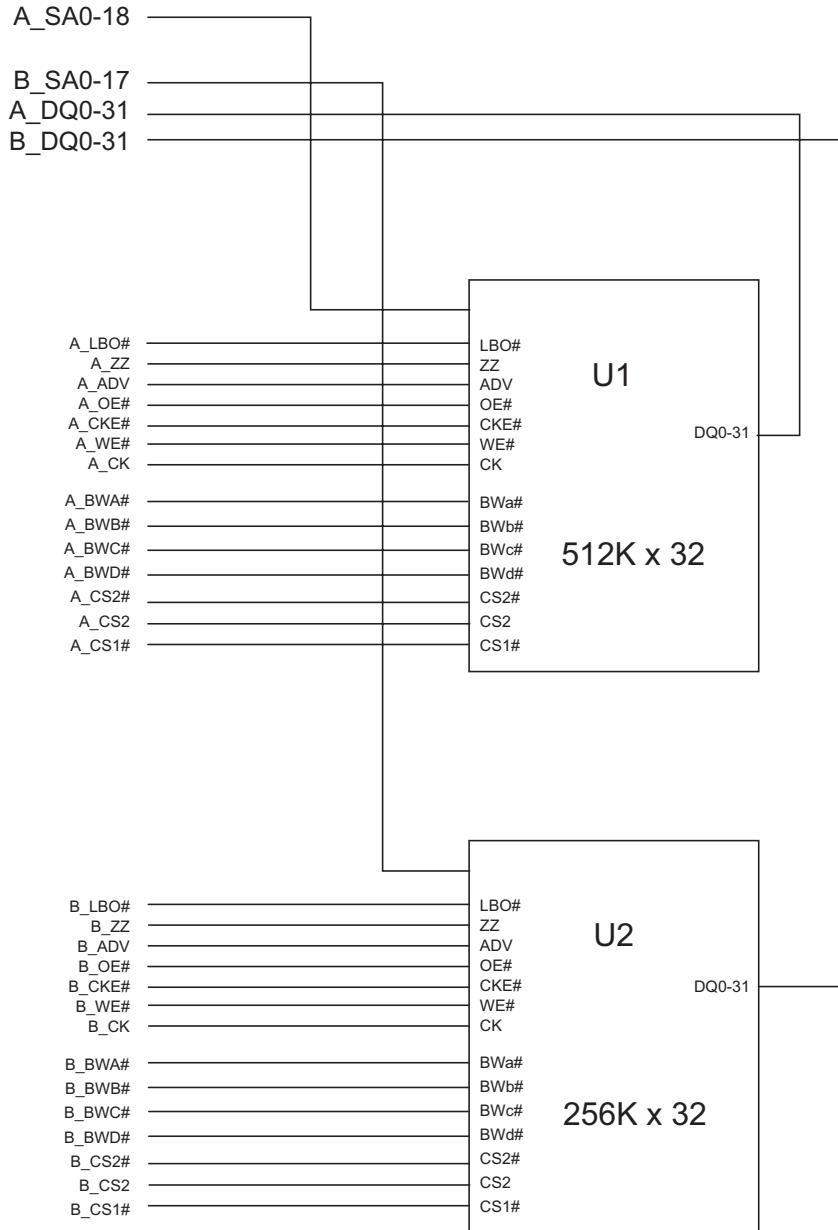
## PIN CONFIGURATION

(TOP VIEW)

	1	2	3	4	5	6	7	8	9	10	11
<b>A</b>	V <sub>SS</sub>	A_DATb0	A_DATb1	A_DATb2	A_DATb3	V <sub>SS</sub>	A_DATa0	A_DATa1	A_DATa2	A_DATa3	V <sub>SS</sub>
<b>B</b>	NC	A_DATb4	A_DATb5	A_DATb6	A_DATb7	V <sub>SS</sub>	A_DATa4	A_DATa5	A_DATa6	A_DATa7	NC
<b>C</b>	A_ADR	A_ADR	A_OE#	A_ADV	A_BWEb	V <sub>SS</sub>	A_BWEa	A_ZZ	A_ADR	A_ADR	A_ADR
<b>D</b>	A_ADR	V <sub>SS</sub>	A_CKE#	V <sub>CC</sub>	V <sub>CC</sub>	V <sub>CC</sub>	V <sub>CC</sub>	V <sub>CC</sub>	V <sub>CC</sub>	A_ADR	A_ADR
<b>E</b>	A_ADR	A_CK	A_GWE#	V <sub>CC</sub>	V <sub>CC</sub>	V <sub>CC</sub>	V <sub>CC</sub>	V <sub>CC</sub>	V <sub>CC</sub>	A_ADR <sub>1</sub>	A_ADR <sub>0</sub>
<b>F</b>	A_ADR	V <sub>SS</sub>	A_CS2#	V <sub>CC</sub>	V <sub>CC</sub>	V <sub>CC</sub>	V <sub>CC</sub>	V <sub>CC</sub>	V <sub>CC</sub>	A_ADR	A_ADR
<b>G</b>	A_ADR	A_ADR	A_CS1#	A_CS2	A_BWEc	V <sub>SS</sub>	A_BWEd	A_LBO#	A_ADR	A_ADR	A_ADR
<b>H</b>	NC	A_DATc0	A_DATc1	A_DATc2	A_DATc3	V <sub>SS</sub>	A_DATd0	A_DATd1	A_DATd2	A_DATd3	NC
<b>J</b>	V <sub>SS</sub>	A_DATc4	A_DATc5	A_DATc6	A_DATc7	V <sub>SS</sub>	A_DATd4	A_DATd5	A_DATd6	A_DATd7	V <sub>SS</sub>
<b>K</b>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>
<b>L</b>	V <sub>SS</sub>	B_DATb0	B_DATb1	B_DATb2	B_DATb3	V <sub>SS</sub>	B_DATa0	B_DATa1	B_DATa2	B_DATa3	V <sub>SS</sub>
<b>M</b>	NC	B_DATb4	B_DATb5	B_DATb6	B_DATb7	V <sub>SS</sub>	B_DATa4	B_DATa5	B_DATa6	B_DATa7	NC
<b>N</b>	B_ADR	B_ADR	B_OE#	B_ADV	B_BWEb	V <sub>SS</sub>	B_BWEa	B_ZZ	B_ADR	B_ADR	B_ADR
<b>P</b>	B_ADR	V <sub>SS</sub>	B_CKE#	V <sub>CC</sub>	V <sub>CC</sub>	V <sub>CC</sub>	V <sub>CC</sub>	V <sub>CC</sub>	V <sub>CC</sub>	B_ADR	B_ADR
<b>R</b>	B_ADR	B_CK	B_GWE#	V <sub>CC</sub>	V <sub>CC</sub>	V <sub>CC</sub>	V <sub>CC</sub>	V <sub>CC</sub>	V <sub>CC</sub>	B_ADR <sub>1</sub>	B_ADR <sub>0</sub>
<b>T</b>	B_ADR	V <sub>SS</sub>	B_CS2#	V <sub>CC</sub>	V <sub>CC</sub>	V <sub>CC</sub>	V <sub>CC</sub>	V <sub>CC</sub>	V <sub>CC</sub>	B_ADR	B_ADR
<b>U</b>	B_ADR	NC	B_CS1#	B_CS2	B_BWEc	V <sub>SS</sub>	B_BWEd	B_LBO#	B_ADR	B_ADR	B_ADR
<b>V</b>	NC	B_DATc4	B_DATc5	B_DATc6	B_DATc7	V <sub>SS</sub>	B_DATd4	B_DATd5	B_DATd6	B_DATd7	NC
<b>W</b>	V <sub>SS</sub>	B_DATc0	B_DATc1	B_DATc2	B_DATc3	V <sub>SS</sub>	B_DATd0	B_DATd1	B_DATd2	B_DATd3	V <sub>SS</sub>



FIG. 1 BLOCK DIAGRAM





FUNCTION DESCRIPTION

The WED2ZLRSP01S is an NBL Dual Array SSRAM designed to sustain 100% bus bandwidth by eliminating turnaround cycle when there is transition from Read to Write, or vice versa. All inputs (with the exception of OE#, LBO# and ZZ) are synchronized to rising clock edges, and all features are available on each of the independent arrays.

All read, write and deselect cycles are initiated by the ADV input. Subsequent burst addresses can be internally generated by the burst advance pin (ADV). ADV should be driven to Low once the device has been deselected in order to load a new address for next operation.

Clock Enable (CKE#) pin allows the operation of the chip to be suspended as long as necessary. When CKE# is high, all synchronous inputs are ignored and the internal device registers will hold their previous values. NBL SSRAM latches external address and initiates a cycle when CKE# and ADV are driven low at the rising edge of the clock.

Output Enable (OE#) can be used to disable the output at any given time. Read operation is initiated when at the rising edge of the clock, the address presented to the address inputs are latched in the address register, CKE# is driven low, the write enable input signals WE# are driven high, and ADV driven low. The internal array is read between the first rising edge and the second rising edge of the clock and the data is latched in the output register. At the second clock edge the data is driven out of the SRAM. During read operation OE# must be driven low for the device to drive out the requested data.

Write operation occurs when WE# is driven low at the rising edge of the clock. BW#[d:a] can be used for byte write operation. The pipe-lined NBL SSRAM uses a late-late write cycle to utilize 100% of the bandwidth. At the first rising edge of the clock, WE and address are registered, and the data associated with that address is required two cycle later.

Subsequent addresses are generated by ADV High for the burst access as shown below. The starting point of the burst sequence is provided by the external address. The burst address counter wraps around to its initial state upon completion. The burst sequence is determined by the state of the LBO# pin. When this pin is low, linear burst sequence is selected. And when this pin is high, Interleaved burst sequence is selected.

During normal operation, ZZ must be driven low. When ZZ is driven high, the SRAM will enter a Power Sleep Mode after 2 cycles. At this time, internal state of the SRAM is preserved. When ZZ returns to low, the SRAM operates after 2 cycles of wake up time.

BURST SEQUENCE TABLE

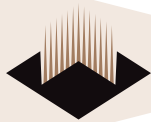
(Interleaved Burst, LBO# = High)

Table with 4 cases (Case 1-4) showing address sequences for LBO# Pin High. Columns include LBO# Pin, High, and address bits A1, A0 for each case. A downward arrow indicates the sequence from First Address to Fourth Address.

(Interleaved Burst, LBO = High)

Table with 4 cases (Case 1-4) showing address sequences for LBO# Pin High. Columns include LBO# Pin, High, and address bits A1, A0 for each case. A downward arrow indicates the sequence from First Address to Fourth Address.

NOTE 1: LBO# pin must be tied to High or Low, and Floating State must not be allowed.



TRUTH TABLES

SYNCHRONOUS TRUTH TABLE

CEx#	ADV	WE#	BWx#	OE#	CKE#	CK	Address Accessed	Operation
H	L	X	X	X	L	↑	N/A	Deselect
X	H	X	X	X	L	↑	N/A	Continue Deselect
L	L	H	X	L	L	↑	External Address	Begin Burst Read Cycle
X	H	X	X	L	L	↑	Next Address	Continue Burst Read Cycle
L	L	H	X	H	L	↑	External Address	NOP/Dummy Read
X	H	X	X	H	L	↑	Next Address	Dummy Read
L	L	L	L	X	L	↑	External Address	Begin Burst Write Cycle
X	H	X	L	X	L	↑	Next Address	Continue Burst Write Cycle
L	L	L	H	X	L	↑	N/A	NOP/Write Abort
X	H	X	H	X	L	↑	Next Address	Write Abort
X	X	X	X	X	H	↑	Current Address	Ignore Clock

NOTES:

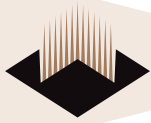
1. X means "Don't Care."
2. The rising edge of clock is symbolized by ( ↑ )
3. A continue deselect cycle can only be entered if a deselect cycle is executed first.
4. WRITE# = L means Write operation in WRITE TRUTH TABLE.  
WRITE# = H means Read operation in WRITE TRUTH TABLE.
5. Operation finally depends on status of asynchronous input pins (ZZ and OE#).
6. CEx# refers to the combination of CE<sub>1</sub>#, CE<sub>2</sub> and CE<sub>2</sub>#.
7. Applies to each of the independent arrays.

WRITE TRUTH TABLE

WE#	BWa#	BWb#	BWc#	BWd#	Operation
H	X	X	X	X	Read
L	L	H	H	H	Write Byte a
L	H	L	H	H	Write Byte b
L	H	H	L	H	Write Byte c
L	H	H	H	L	Write Byte d
L	L	L	L	L	Write All Bytes
L	H	H	H	H	Write Abort/NOP

NOTES:

1. X means "Don't Care."
2. All inputs in this table must meet setup and hold time around the rising edge of CK ( ↑ ).
3. Applies to each of the independent arrays.



## ABSOLUTE MAXIMUM RATINGS\*

Voltage on Vdd Supply Relative to Vss	-0.3V to +3.6V
V <sub>IN</sub> (DQx)	-0.3V to +3.6V
V <sub>IN</sub> (Inputs)	-0.3V to +3.6V
Storage Temperature (BGA)	-55°C to +125°C
Short Circuit Output Current	100mA

\*Stress greater than those listed under "Absolute Maximum Ratings": may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## ELECTRICAL CHARACTERISTICS (0°C ≤ T<sub>A</sub> ≤ 70°C)

Description	Symbol	Conditions	Min	Max	Units	Notes
Input High (Logic 1) Voltage	V <sub>IH</sub>		1.7	V <sub>CC</sub> + 0.3	V	1
Input Low (Logic 0) Voltage	V <sub>IL</sub>		-0.3	0.7	V	1
Input Leakage Current	I <sub>LI</sub>	0V ≤ V <sub>IN</sub> ≤ V <sub>CC</sub>	-5	5	μA	2
Output Leakage Current	I <sub>LO</sub>	Output(s) Disabled, 0V ≤ V <sub>IN</sub> ≤ V <sub>CC</sub>	-5	5	μA	
Output High Voltage	V <sub>OH</sub>	I <sub>OH</sub> = -1.0mA	2.0	---	V	1
Output Low Voltage	V <sub>OL</sub>	I <sub>OL</sub> = 1.0mA	---	0.4	V	1
Supply Voltage	V <sub>CC</sub>		2.375	2.625	V	1

### NOTES:

- All voltages referenced to V<sub>SS</sub> (GND)
- ZZ pin has an internal pull-up, and input leakage is higher.

## DC CHARACTERISTICS

Description	Symbol	Conditions	Typ	166 MHz	150 MHz	133 MHz	100 MHz	Units	Notes
Power Supply Current: Operating	I <sub>DD</sub>	Device Selected; All Inputs ≤ V <sub>IL</sub> or ≥ V <sub>IH</sub> ; Cycle Time = t <sub>CYC</sub> MIN; V <sub>CC</sub> = MAX; Output Open		650	600	560	500	mA	1, 2
Power Supply Current: Standby	I <sub>SB2</sub>	Device Deselected; V <sub>CC</sub> = MAX; All Inputs ≤ V <sub>SS</sub> + 0.2 or V <sub>CC</sub> - 0.2; All Inputs Static; CK Frequency = 0; ZZ ≤ V <sub>IL</sub>	30	60	60	60	60	mA	2
Power Supply Current: Current	I <sub>SB3</sub>	Device Selected; All Inputs ≤ V <sub>IL</sub> or ≥ V <sub>IH</sub> ; Cycle Time = t <sub>CYC</sub> MIN; V <sub>CC</sub> = MAX; Output Open; ZZ ≥ V <sub>CC</sub> - 0.2V	20	40	40	40	40	mA	2
Clock Running Standby Current	I <sub>SB4</sub>	Device Deselected; V <sub>CC</sub> = MAX; All Inputs ≤ V <sub>SS</sub> + 0.2 or V <sub>CC</sub> - 0.2; Cycle Time = t <sub>CYC</sub> MIN; ZZ ≤ V <sub>IL</sub>		140	120	100	80	mA	2

### NOTES:

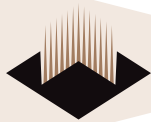
- I<sub>DD</sub> is specified with no output current and increases with faster cycle times. I<sub>DD</sub> increases with faster cycle times and greater output loading.
- Typical values are measured at 2.5V, 25°C, and 10ns cycle time.

## BGA CAPACITANCE

Description	Symbol	Conditions	Typ	Max	Units	Notes
Control Input Capacitance	C <sub>I</sub>	T <sub>A</sub> = 25°C; f = 1MHz	5	7	pF	1
Input/Output Capacitance (DQ)	C <sub>O</sub>	T <sub>A</sub> = 25°C; f = 1MHz	6	8	pF	1
Address Capacitance	C <sub>A</sub>	T <sub>A</sub> = 25°C; f = 1MHz	5	7	pF	1
Clock Capacitance	C <sub>CK</sub>	T <sub>A</sub> = 25°C; f = 1MHz	3	5	pF	1

### NOTES:

- This parameter is sampled.



AC CHARACTERISTICS

Parameter	Symbol	166MHz		150MHz		133MHz		100MHz		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
Clock Time	t <sub>cyc</sub>	6.0		6.7		7.5		10.0		ns
Clock Access Time	t <sub>cd</sub>	—	3.5	—	3.8	—	4.2	—	5.0	ns
Output enable to Data Valid	t <sub>oE</sub>	—	3.5	—	3.8	—	4.2	—	5.0	ns
Clock High to Output Low-Z	t <sub>lZC</sub>	1.5	—	1.5	—	1.5	—	1.5	—	ns
Output Hold from Clock High	t <sub>oH</sub>	1.5	—	1.5	—	1.5	—	1.5	—	ns
Output Enable Low to output Low-Z	t <sub>lZOE</sub>	0.0	—	0.0	—	0.0	—	0.0	—	ns
Output Enable High to Output High-Z	t <sub>hZOE</sub>	—	3.0	—	3.0	—	3.5	—	3.5	ns
Clock High to Output High-Z	t <sub>hZC</sub>	—	3.0	—	3.0	—	3.5	—	3.5	ns
Clock High Pulse Width	t <sub>CH</sub>	2.2	—	2.5	—	3.0	—	3.0	—	ns
Clock Low Pulse Width	t <sub>CL</sub>	2.2	—	2.5	—	3.0	—	3.0	—	ns
Address Setup to Clock High	t <sub>AS</sub>	1.5	—	1.5	—	1.5	—	1.5	—	ns
CKE# Setup to Clock High	t <sub>CEs</sub>	1.5	—	1.5	—	1.5	—	1.5	—	ns
Data Setup to Clock High	t <sub>DS</sub>	1.5	—	1.5	—	1.5	—	1.5	—	ns
Write Setup to Clock High	t <sub>WS</sub>	1.5	—	1.5	—	1.5	—	1.5	—	ns
Address Advance to Clock High	t <sub>ADVs</sub>	1.5		1.5		1.5		1.5		ns
Chip Select Setup to Clock High	t <sub>CSS</sub>	1.5		1.5		1.5		1.5		ns
Address Hold to Clock high	t <sub>AH</sub>	0.5	—	0.5	—	0.5	—	0.5	—	ns
CKE# Hold to Clock High	t <sub>CEH</sub>	0.5	—	0.5	—	0.5	—	0.5	—	ns
Data Hold to Clock High	t <sub>DH</sub>	0.5	—	0.5	—	0.5	—	0.5	—	ns
Write Hold to Clock High	t <sub>WH</sub>	0.5	—	0.5	—	0.5	—	0.5	—	ns
Address Advance to Clock High	t <sub>ADVH</sub>	0.5	—	0.5	—	0.5	—	0.5	—	ns
Chip Select Hold to Clock High	t <sub>CsH</sub>	0.5	—	0.5	—	0.5	—	0.5	—	ns

NOTES:

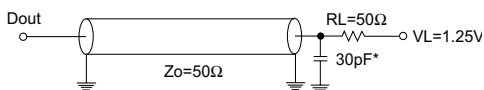
1. All Address inputs must meet the specified setup and hold times for all rising clock (CK) edges when ADV is sampled low and CE# is sampled valid. All other synchronous inputs must meet the specified setup and hold times whenever this device is chip selected.
2. Chip enable must be valid at each rising edge of CK (when ADV is Low) to remain enabled.
3. A write cycle is defined by WE# low having been registered into the device at ADV Low. A Read cycle is defined by WE# High with ADV Low. Both cases must meet setup and hold times.
4. Applies to each of the independent arrays.

AC TEST CONDITIONS

(0 ≤ T<sub>A</sub> ≤ 70°C, V<sub>CC</sub> = 2.5V ± 5%, Unless Otherwise Specified)

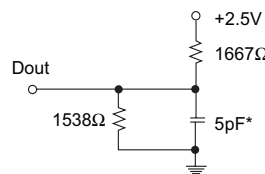
Parameter	Value
Input Pulse Level	0 to 2.5V
Input Rise and Fall Time (Measured at 20% to 80%)	1.0V/ns
Input and Output Timing Reference Levels	1.25V
Output Load	See Output Load (A)

OUTPUT LOAD (A)



OUTPUT LOAD (B)

(for t<sub>lZC</sub>, t<sub>lZOE</sub>, t<sub>hZOE</sub>, and t<sub>hZC</sub>)



\*Including Scope and Jig Capacitance



### SNOOZE MODE

SNOOZE MODE is a low-current, “power-down” mode in which the device is deselected and current is reduced to  $I_{SBZ}$ . The duration of SNOOZE MODE is dictated by the length of time Z is in a HIGH state. After the device enters SNOOZE MODE, all inputs except ZZ become gated inputs and are ignored. ZZ is an asynchronous, active HIGH input that causes the device to enter SNOOZE MODE.

When ZZ becomes a logic HIGH,  $I_{SBZ}$  is guaranteed after the setup time  $t_{ZZ}$  is met. Any READ or WRITE operation pending when the device enters SNOOZE MODE is not guaranteed to complete successfully. Therefore, SNOOZE MODE must not be initiated until valid pending operations are completed.

### SNOOZE MODE

Description	Conditions	Symbol	Min	Max	Units	Notes
Current during SNOOZE MODE	$ZZ \geq V_{IH}$	$I_{SBZ}$		10	mA	
ZZ active to input ignored		$t_{ZZ}$		$2(t_{kc})$	ns	1
ZZ inactive to input sampled		$t_{RZZ}$	$2(t_{kc})$		ns	1
ZZ active to snooze current		$t_{ZZI}$		$2(t_{kc})$	ns	1
ZZ inactive to exit snooze current		$t_{RZZI}$			ns	1

FIG. 2 SNOOZE MODE TIMING DIAGRAM

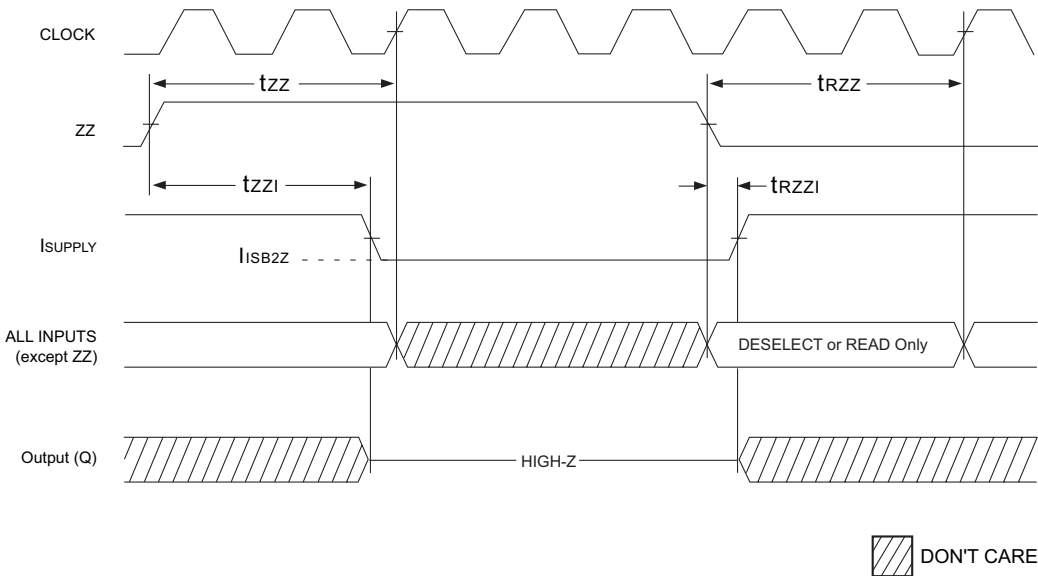
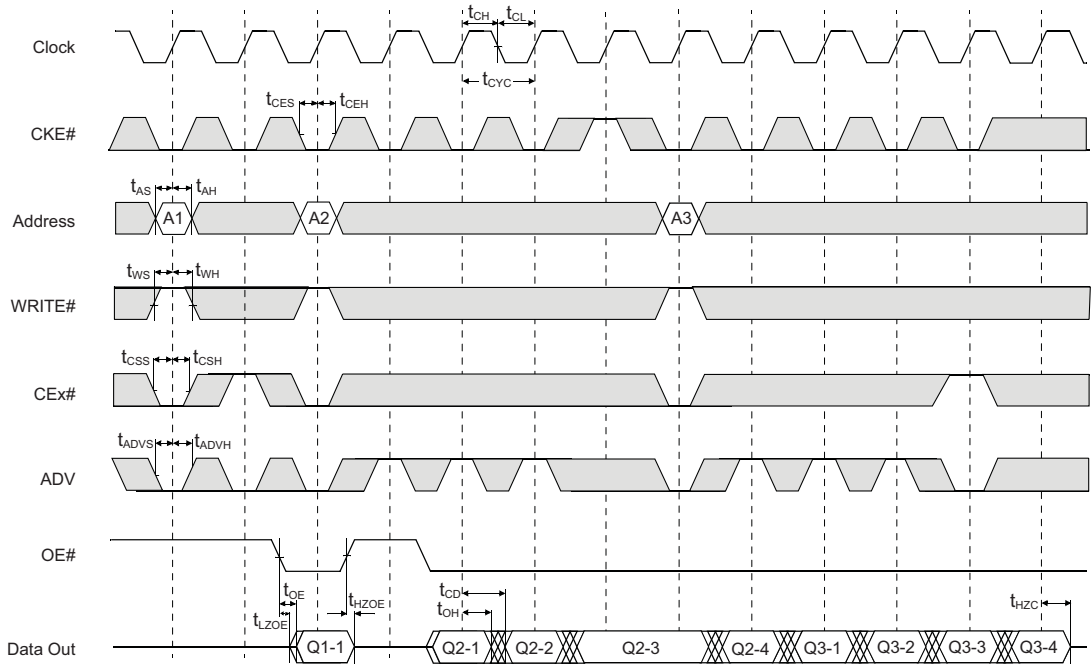




FIG. 3 TIMING WAVEFORM OF READ CYCLE



NOTES: WRITE# = L means WE# = L, and BWx# = L  
 CEx# refers to the combination of CE1#, CE2 and CE2#.

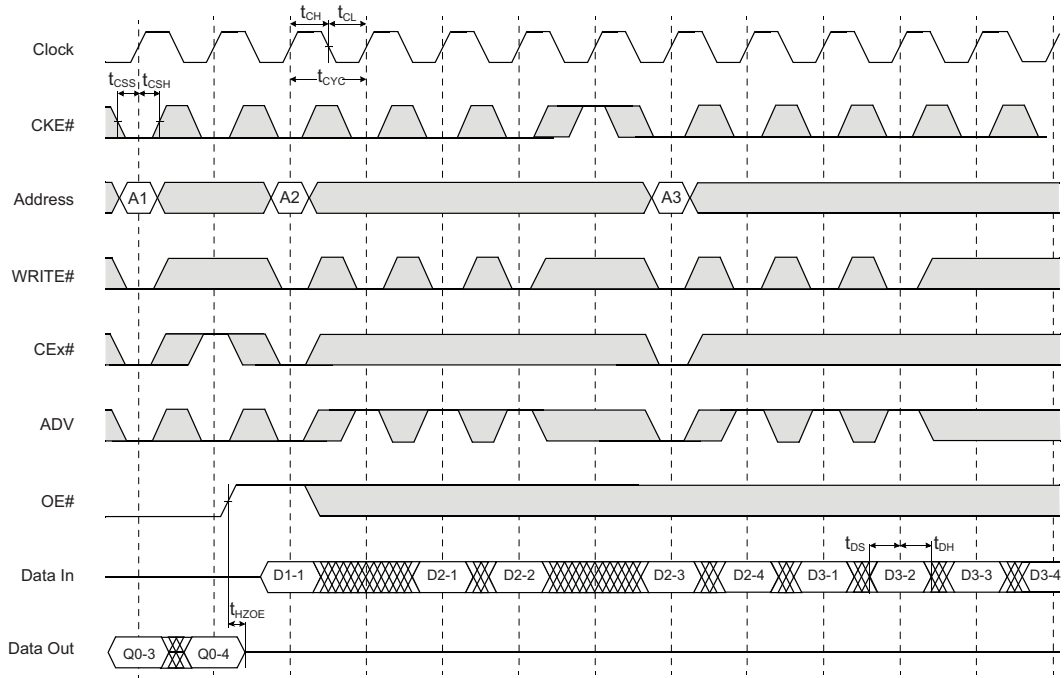
□ Dont Care  
 ⊞ Undefined

Note:  
 Applies to both independent arrays.





FIG. 4 TIMING WAVEFORM OF WRITE CYCLE



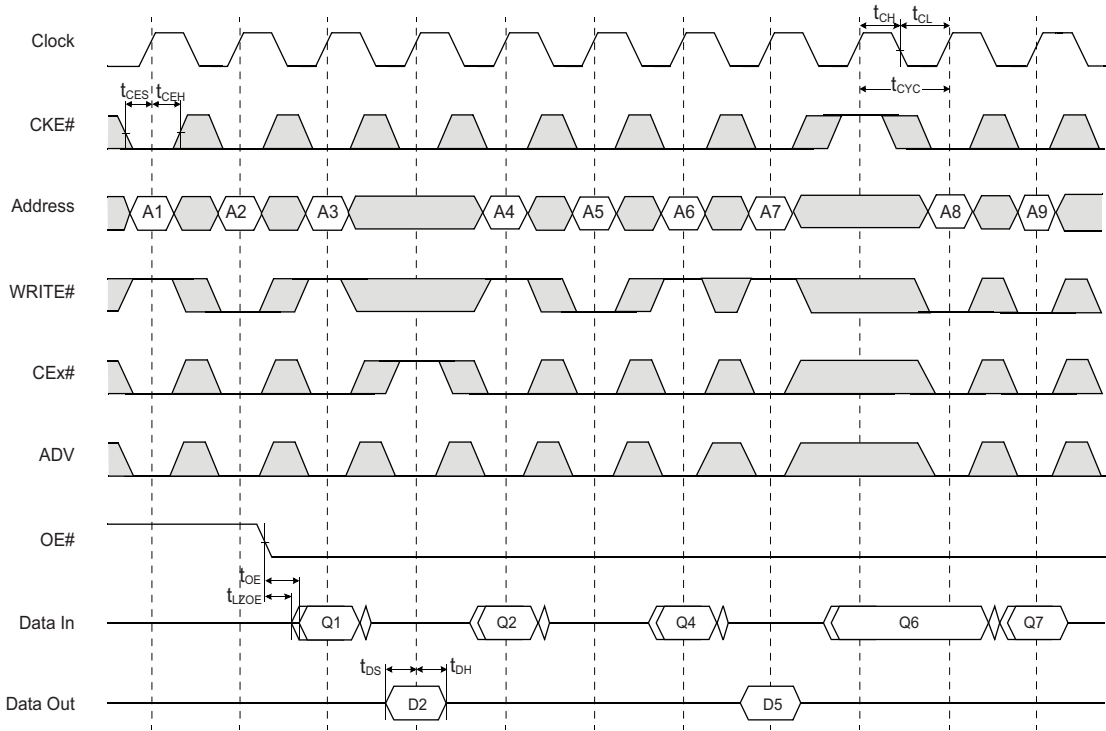
NOTES: WRITE# = L means WE# = L, and BWx# = L  
CEx# refers to the combination of CE1#, CE2 and CE2#.

□ Dont Care  
⊗ Undefined

Note:  
Applies to both independent arrays.



FIG. 5 TIMING WAVEFORM OF SINGLE READ/WRITE



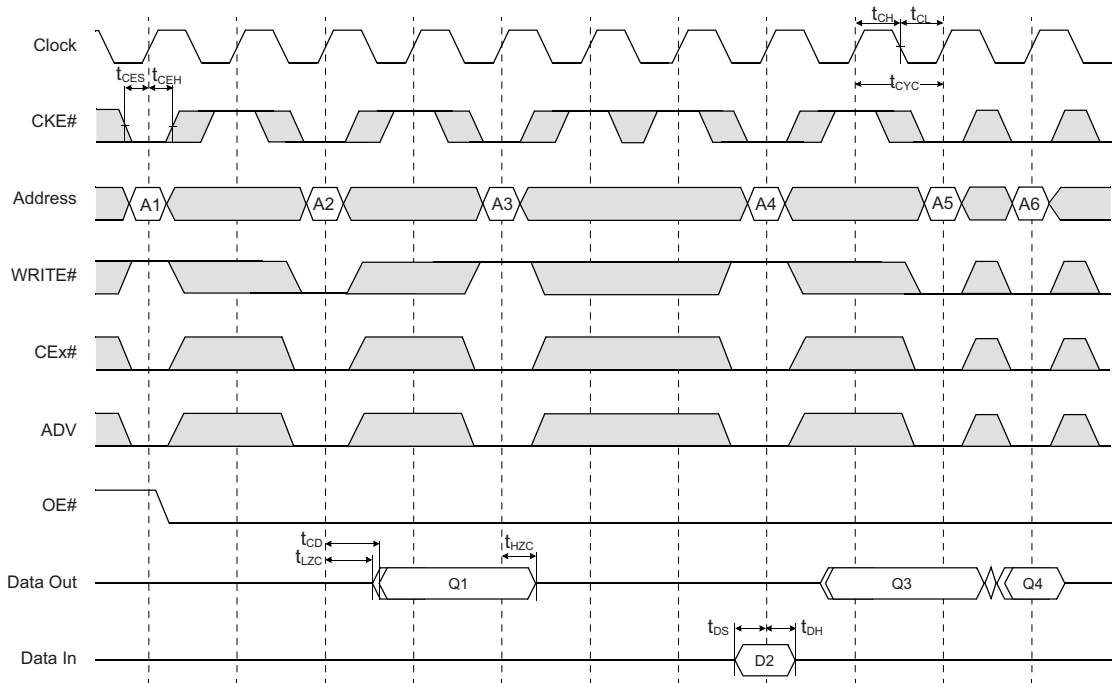
NOTES: WRITE# = L means WE# = L, and BWx# = L  
CEx# refers to the combination of CE1#, CE2 and CE2#.

□ Dont Care  
⊗ Undefined

Note:  
Applies to both independent arrays.



FIG. 6 TIMING WAVEFORM OF CKE# OPERATION



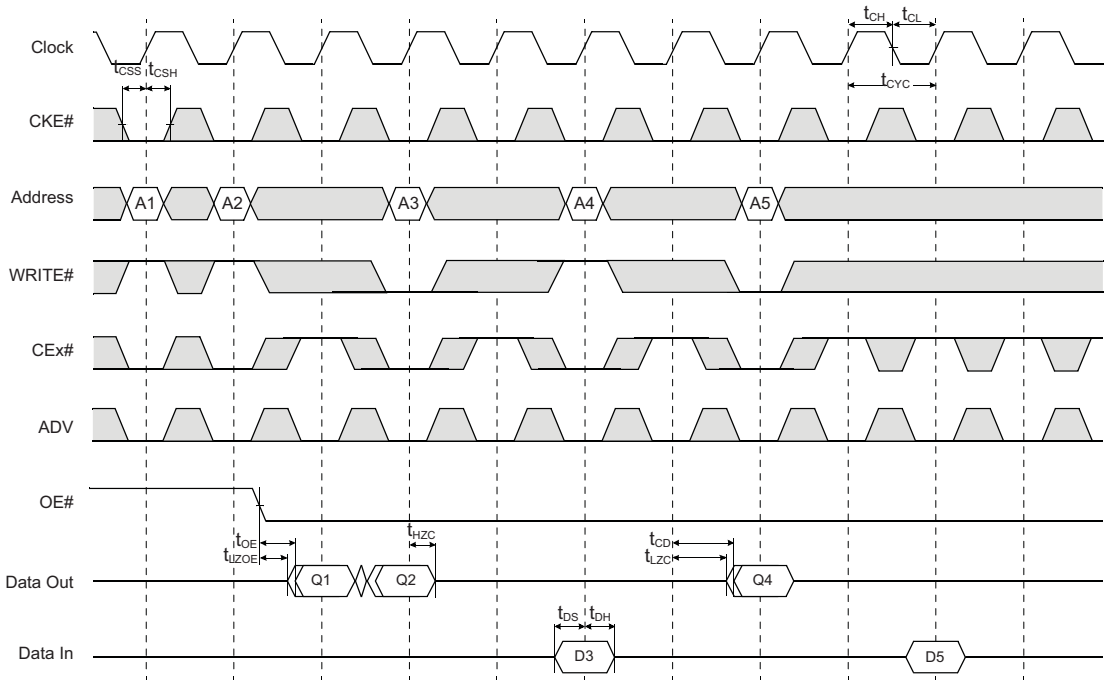
NOTES: WRITE# = L means WE# = L, and BWx# = L  
CEx# refers to the combination of CE1#, CE2 and CE2#.

□ Dont Care  
⊗ Undefined

Note:  
Applies to both independent arrays.



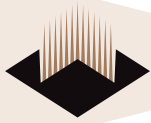
FIG. 7 TIMING WAVEFORM OF CE# OPERATION



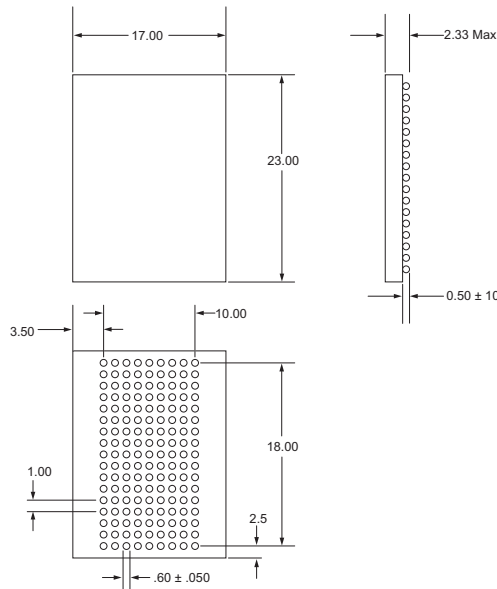
NOTES: WRITE# = L means WE# = L, and BWx# = L.  
 CEEx# refers to the combination of CE1#, CE2 and CE2#.

□ Dont Care  
 ⊞ Undefined

Note:  
 Applies to both independent arrays.



**PACKAGE DIMENSION: 153 BUMP PBGA**



ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

**NOTE:** Ball attach pad for above BGA package is 620 microns in diameter. Pad is solder mask defined.

**ORDERING INFORMATION**

Commercial Temp Range (0°C to 70°C)

Part Number	Configuration	tCD (ns)	Clock (MHz)	Operating Range	Temperature Range
WED2ZLRSP01S35BC	512K x 32/256K x 32	3.5	166	Commercial	0° - 70° C
WED2ZLRSP01S38BC	512K x 32/256K x 32	3.8	150	Commercial	0° - 70° C
WED2ZLRSP01S42BC	512K x 32/256K x 32	4.2	133	Commercial	0° - 70° C
WED2ZLRSP01S50BC	512K x 32/256K x 32	5.0	100	Commercial	0° - 70° C
WED2ZLRSP01S38BI	512K x 32/256K x 32	3.8	150	Industrial	-40° - 85° C
WED2ZLRSP01S42BI	512K x 32/256K x 32	4.2	133	Industrial	-40° - 85° C
WED2ZLRSP01S50BI	512K x 32/256K x 32	5.0	100	Industrial	-40° - 85° C