



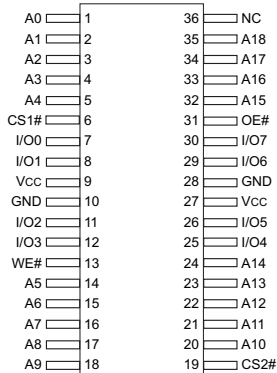
2x512Kx8 DUALITHIC™ SRAM

FEATURES

- Access Times 17, 20, 25, 35, 45, 55ns
- Revolutionary, Center Power/Ground Pinout
- Packaging:
 - 32 pin, Hermetic Ceramic DIP (Package 300)
 - 36 lead Ceramic SOJ (Package 100)
 - 36 lead Ceramic Flatpack (Package 226)
- Organized as two banks of 512Kx8
- Commercial, Industrial and Military Temperature Ranges
- 5 Volt Power Supply
- Low Power CMOS
- TTL Compatible Inputs and Outputs

PIN CONFIGURATION FOR WS1M8-XDJX AND WS1M8-XFX

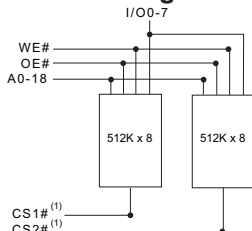
36 CSOJ
36 FLATPACK
TOP VIEW



Pin Description

A0-18	Address Inputs
I/O0-7	Data Input/Output
CS1-2#	Chip Selects
OE#	Output Enable
WE#	Write Enable
Vcc	+5.0V Power
GND	Ground

Block Diagram

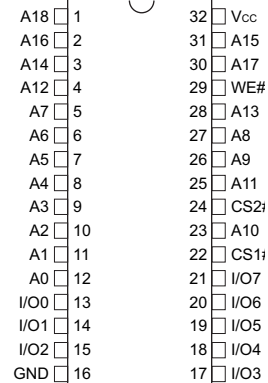


NOTE:

1. CS1# and CS2# are used to select the lower and upper 512Kx8 of the device. CS1# and CS2# must not be enabled at the same time.

PIN CONFIGURATION FOR WS1M8-XCX

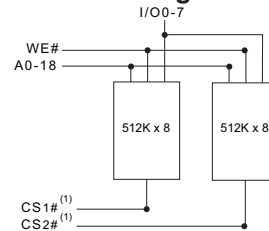
32 DIP
TOP VIEW



Pin Description

A0-18	Address Inputs
I/O0-7	Data Input/Output
CS1-2#	Chip Selects
WE#	Write Enable
Vcc	+5.0V Power
GND	Ground

Block Diagram





ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Unit
Operating Temperature	T _A	-55	+125	°C
Storage Temperature	T _{STG}	-65	+150	°C
Signal Voltage Relative to GND	V _G	-0.5	V _{CC} +0.5	V
Junction Temperature	T _J		150	°C
Supply Voltage	V _{CC}	-0.5	7.0	V

TRUTH TABLE

CS#	OE#	WE#	Mode	Data I/O	Power
H	X	X	Standby	High Z	Standby
L	L	H	Read	Data Out	Active
L	X	L	Write	Data In	Active
L	H	H	Out Disable	High Z	Active

NOTE: OE# is internally tied to the GND and not accessible on the WS1M8-XXCX.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V _{CC}	4.5	5.5	V
Input High Voltage	V _{IH}	2.2	V _{CC} + 0.3	V
Input Low Voltage	V _{IL}	-0.3	+0.8	V
Operating Temp. (Mil.)	T _A	-55	+125	°C

CAPACITANCE

T_A = +25°C

Parameter	Symbol	Condition	Max	Unit
Input capacitance	C _{IN}	V _{IN} = 0V, f = 1.0MHz	20	pF
Output capacitance	C _{OUT}	V _{OUT} = 0V, f = 1.0MHz	20	pF

This parameter is guaranteed by design but not tested.

DC CHARACTERISTICS

V_{CC} = 5.0V, V_{SS} = 0V, -55°C ≤ T_A ≤ +125°C

Parameter	Sym	Conditions	Min	Max	Units
Input Leakage Current	I _{LI}	V _{CC} = 5.5, V _{IN} = GND to V _{CC}		10	µA
Output Leakage Current	I _{LO} ¹	CS# = V _{IH} , OE# = V _{IH} , V _{OUT} = GND to V _{CC}		10	µA
Operating Supply Current	I _{CC} ¹	CS# = V _{IL} , OE# = V _{IH} , f = 5MHz, V _{CC} = 5.5		180	mA
Standby Current	I _{SB} ¹	CS# = V _{IH} , OE# = V _{IH} , f = 5MHz, V _{CC} = 5.5		40	mA
Output Low Voltage	V _{OL}	I _{OL} = 6mA		0.4	V
Output High Voltage	V _{OH}	I _{OH} = -4.0mA	2.4		V

NOTE: DC test conditions: V_{IH} = V_{CC} - 0.3V, V_{IL} = 0.3V

1. OE# is internally tied to the GND and not accessible on the WS1M8-XXCX.



AC CHARACTERISTICS

V_{CC} = 5.0V, V_{SS} = 0V, -55°C ≤ T_A ≤ +125°C

Parameter Read Cycle	Symbol	-17		-20		-25		-35		-45		-55		Units
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle Time	t _{RC}	17		20		25		35		45		55		ns
Address Access Time	t _{AA}		17		20		25		35		45		55	ns
Output Hold from Address Change	t _{OH}	0		0		0		0		0		0		ns
Chip Select Access Time	t _{ACS}		17		20		25		35		45		55	ns
Output Enable to Output Valid	t _{OE²}		9		10		12		25		25		25	ns
Chip Select to Output in Low Z	t _{CLZ¹}	2		2		2		4		4		4		ns
Output Enable to Output in Low Z	t _{OLZ²}	0		0		0		0		0		0		ns
Chip Disable to Output in High Z	t _{CHZ¹}		9		10		12		15		20		20	ns
Output Disable to Output in High Z	t _{OHZ²}		9		10		12		15		20		20	ns

1. This parameter is guaranteed by design but not tested.
2. OE# is internally tied to the GND and not accessible on the WS1M8-XXXX.

AC CHARACTERISTICS

V_{CC} = 5.0V, V_{SS} = 0V, -55°C ≤ T_A ≤ +125°C

Parameter Write Cycle	Symbol	-17		-20		-25		-35		-45		-55		Units
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle Time	t _{WC}	17		20		25		35		45		55		ns
Chip Select to End of Write	t _{CW}	14		14		15		25		35		50		ns
Address Valid to End of Write	t _{AW}	14		14		15		25		35		50		ns
Data Valid to End of Write	t _{DW}	9		10		10		20		25		25		ns
Write Pulse Width	t _{WP}	14		14		15		25		35		40		ns
Address Setup Time	t _{AS}	0		0		0		0		0		0		ns
Address Hold Time	t _{AH}	0		0		0		0		5		5		ns
Output Active from End of Write	t _{OW¹}	2		3		4		4		5		5		ns
Write Enable to Output in High Z	t _{WHZ¹}		9		9		10		15		15		25	ns
Data Hold Time	t _{DH}	0		0		0		0		0		0		ns

1. This parameter is guaranteed by design but not tested.

AC TEST CIRCUIT

The diagram shows a Device Under Test (D.U.T.) connected to a bridge circuit. The bridge consists of four diodes. Two current sources are connected to the bridge nodes, labeled I_{OL} and I_{OH}. A bipolar supply V_Z ≈ 1.5V is connected across the bridge. A capacitor C_{eff} = 50 pf is connected to the D.U.T. input.

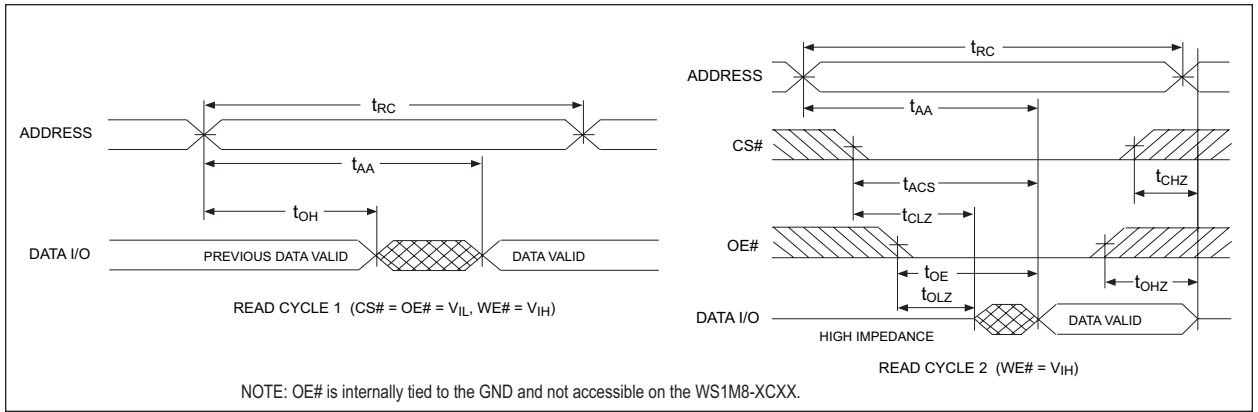
AC TEST CONDITIONS

Parameter	Typ	Unit
Input Pulse Levels	V _{IL} = 0, V _{IH} = 3.0	V
Input Rise and Fall	5	ns
Input and Output Reference Level	1.5	V
Output Timing Reference Level	1.5	V

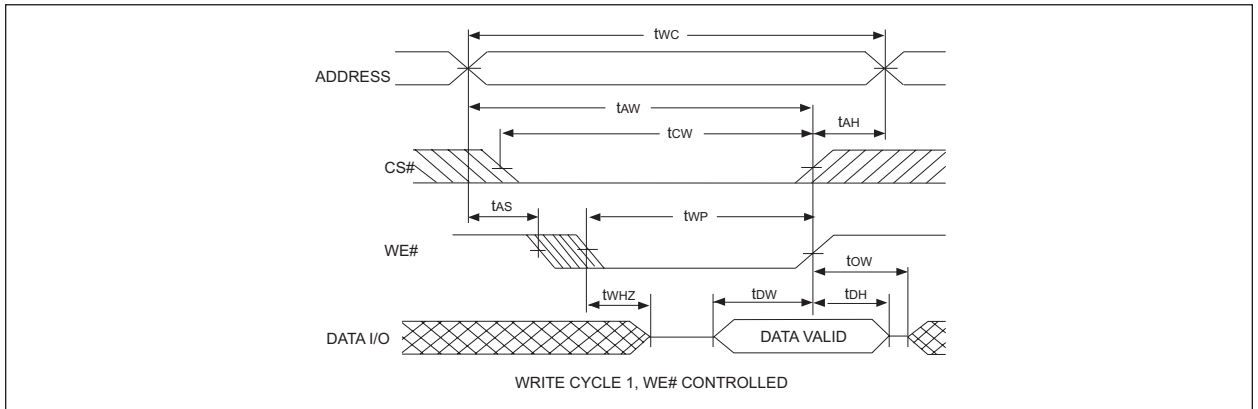
Notes:
V_Z is programmable from -2V to +7V.
I_{OL} & I_{OH} programmable from 0 to 16mA.
Tester Impedance Z₀ = 75 Ω.
V_Z is typically the midpoint of V_{OH} and V_{OL}.
I_{OL} & I_{OH} are adjusted to simulate a typical resistive load circuit.
ATE tester includes jig capacitance.



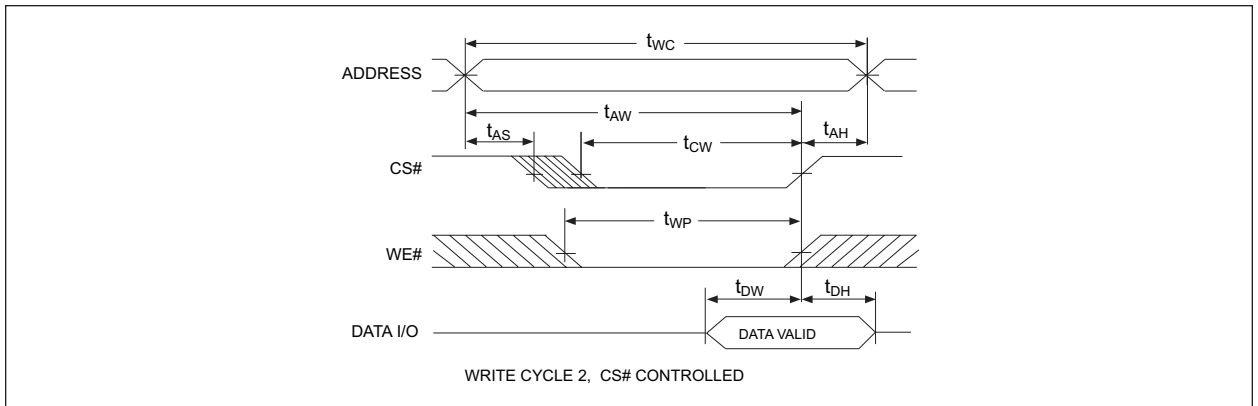
TIMING WAVEFORM – READ CYCLE



WRITE CYCLE – WE# CONTROLLED

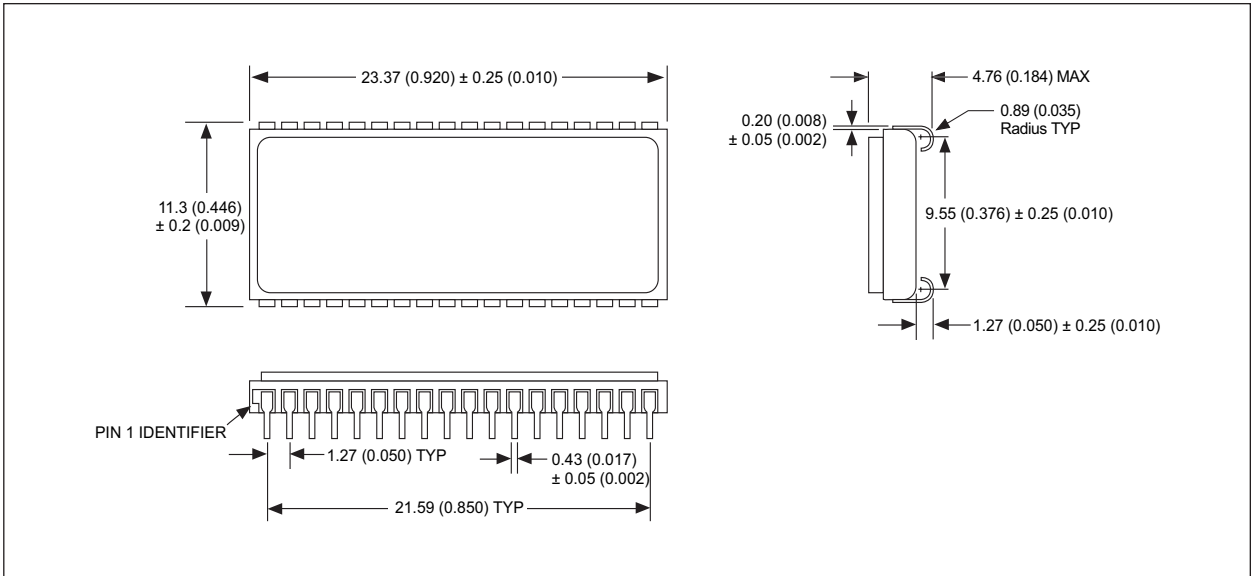


WRITE CYCLE – CS# CONTROLLED



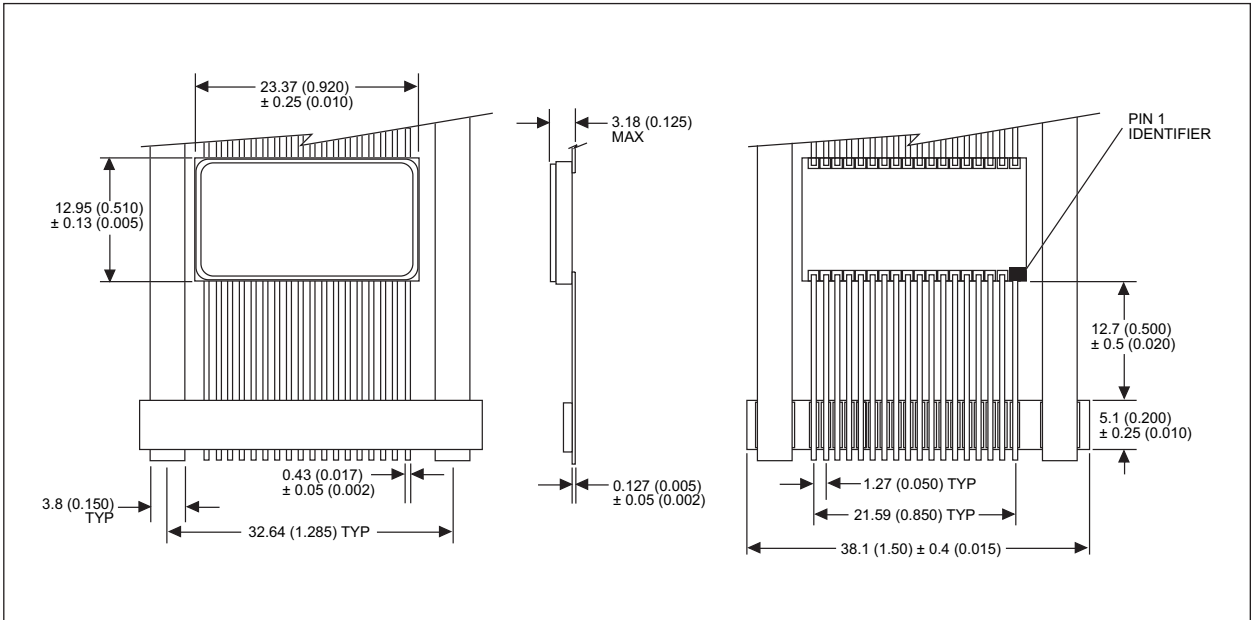


PACKAGE 100: 36 LEAD, CERAMIC SOJ



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

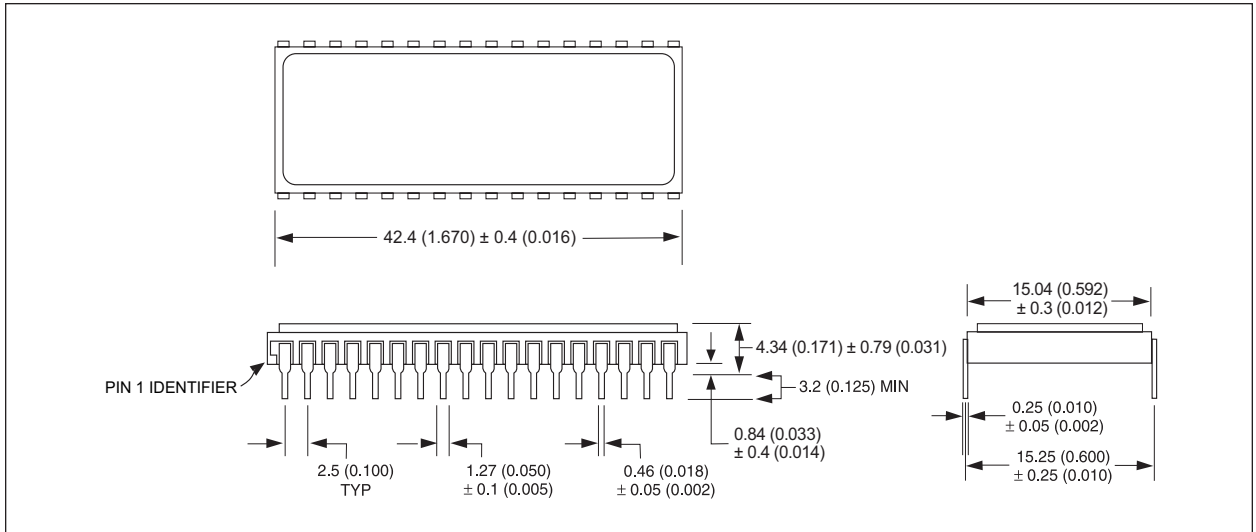
PACKAGE 226: 36 LEAD, CERAMIC FLAT PACK



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PACKAGE 300: 32 PIN, CERAMIC DIP, SINGLE CAVITY SIDE BRAZED



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

ORDERING INFORMATION

