



# 128Kx32 SRAM/FLASH MODULE PRELIMINARY\*

## FEATURES

- Access Times of 25ns (SRAM) and 70, 90 and 120ns (FLASH)
- Packaging:
  - 66-pin, PGA Type, 1.385 inch square HIP, Hermetic Ceramic HIP (Package 402)
- 128Kx32 SRAM
- 128Kx32 5V Flash
- Organized as 128Kx32 of SRAM and 128Kx32 of Flash Memory with common Data Bus
- Low Power CMOS
- Commercial, Industrial and Military Temperature Ranges
- TTL Compatible Inputs and Outputs
- Built-in Decoupling Caps and Multiple Ground Pins for Low Noise Operation
- Weight - 13 grams typical

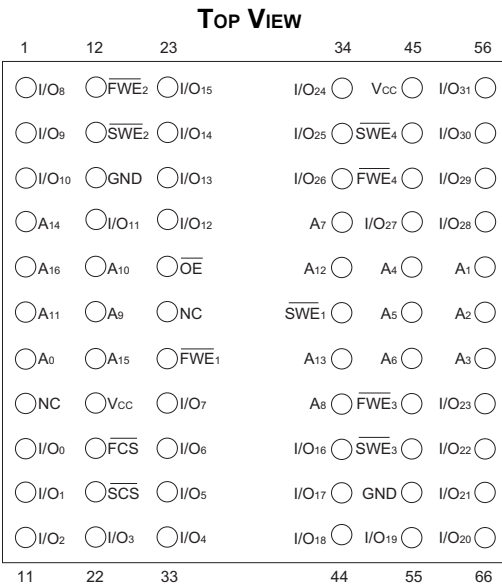
## FLASH MEMORY FEATURES

- 10,000 Erase/Program Cycles
- Sector Architecture
  - 8 equal size sectors of 16K bytes each
  - Any combination of sectors can be concurrently erased. Also supports full chip erase
- 5 Volt Programming; 5V ± 10% Supply
- Embedded Erase and Program Algorithms
- Hardware Write Protection
- Page Program Operation and Internal Program Control Time.

*\* This data sheet describes a product under development, not fully characterized, and is subject to change without notice.*

*Note: Programming information available upon request.*

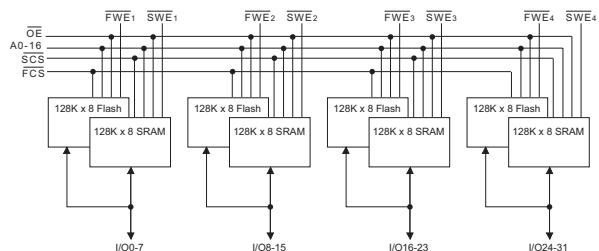
**FIG. 1 PIN CONFIGURATION FOR WSF128K32-XH2X**



**PIN DESCRIPTION**

|                    |                     |
|--------------------|---------------------|
| D <sub>0</sub> -31 | Data Inputs/Outputs |
| A <sub>0</sub> -16 | Address Inputs      |
| SWE <sub>1-4</sub> | SRAM Write Enables  |
| SCS                | SRAM Chip Select    |
| OE                 | Output Enable       |
| V <sub>CC</sub>    | Power Supply        |
| GND                | Ground              |
| NC                 | Not Connected       |
| FWE <sub>1-4</sub> | Flash Write Enables |
| FCS                | Flash Chip Select   |

**BLOCK DIAGRAM**





**ABSOLUTE MAXIMUM RATINGS**

| Parameter                      | Symbol           | Min  | Max  | Unit |
|--------------------------------|------------------|------|------|------|
| Operating Temperature          | T <sub>A</sub>   | -55  | +125 | °C   |
| Storage Temperature            | T <sub>STG</sub> | -65  | +150 | °C   |
| Signal Voltage Relative to GND | V <sub>G</sub>   | -0.5 | 7.0  | V    |
| Junction Temperature           | T <sub>J</sub>   |      | 150  | °C   |
| Supply Voltage                 | V <sub>CC</sub>  | -0.5 | 7.0  | V    |

| Parameter                            |          |
|--------------------------------------|----------|
| Flash Data Retention                 | 10 years |
| Flash Endurance (write/erase cycles) | 10,000   |

**NOTE:**

1. Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

**RECOMMENDED OPERATING CONDITIONS**

| Parameter          | Symbol          | Min  | Max                   | Unit |
|--------------------|-----------------|------|-----------------------|------|
| Supply Voltage     | V <sub>CC</sub> | 4.5  | 5.5                   | V    |
| Input High Voltage | V <sub>IH</sub> | 2.2  | V <sub>CC</sub> + 0.3 | V    |
| Input Low Voltage  | V <sub>IL</sub> | -0.5 | +0.8                  | V    |

**SRAM TRUTH TABLE**

| $\overline{SCS}$ | $\overline{OE}$ | $\overline{SWE}$ | Mode    | Data I/O | Power   |
|------------------|-----------------|------------------|---------|----------|---------|
| H                | X               | X                | Standby | High Z   | Standby |
| L                | L               | H                | Read    | Data Out | Active  |
| L                | H               | H                | Read    | High Z   | Active  |
| L                | X               | L                | Write   | Data In  | Active  |

**NOTE:**

1. FCS must remain high when  $\overline{SCS}$  is low.

**CAPACITANCE  
(T<sub>A</sub> = +25°C)**

| Test   | Symbol           | Condition                        | Max | Unit |
|--|------------------|----------------------------------|-----|------|
| $\overline{OE}$ Capacitance                  | C <sub>OE</sub>  | V <sub>IN</sub> = 0V, f = 1.0MHz | 80  | pF   |
| F/S $\overline{WE}$ 1-4 Capacitance          | C <sub>WE</sub>  | V <sub>IN</sub> = 0V, f = 1.0MHz | 30  | pF   |
| F/S $\overline{CS}$ Capacitance              | C <sub>CS</sub>  | V <sub>IN</sub> = 0V, f = 1.0MHz | 50  | pF   |
| D <sub>0-31</sub> Capacitance                | C <sub>I/O</sub> | V <sub>IN</sub> = 0V, f = 1.0MHz | 30  | pF   |
| A <sub>0</sub> - A <sub>16</sub> Capacitance | C <sub>AD</sub>  | V <sub>IN</sub> = 0V, f = 1.0MHz | 80  | pF   |

This parameter is guaranteed by design but not tested.

**DC CHARACTERISTICS**

(V<sub>CC</sub> = 5.0V, V<sub>SS</sub> = 0V, T<sub>A</sub> = -55°C TO +125°C)

| Parameter   | Symbol             | Conditions   | Min                    | Max  | Unit |
|---|--------------------|--|------------------------|------|------|
| Input Leakage Current   | I <sub>LI</sub>    | V <sub>CC</sub> = 5.5, V <sub>IN</sub> = GND to V <sub>CC</sub>  |                        | 10   | µA   |
| Output Leakage Current  | I <sub>LO</sub>    | $\overline{SCS}$ = V <sub>IH</sub> , $\overline{OE}$ = V <sub>IH</sub> , V <sub>OUT</sub> = GND to V <sub>CC</sub> |                        | 10   | µA   |
| SRAM Operating Supply Current x 32 Mode                       | I <sub>CCx32</sub> | $\overline{SCS}$ = V <sub>IL</sub> , $\overline{OE}$ = FCS = V <sub>IH</sub> , f = 5MHz, V <sub>CC</sub> = 5.5     |                        | 670  | mA   |
| Standby Current   | I <sub>SB</sub>    | FCS = $\overline{SCS}$ = V <sub>IH</sub> , $\overline{OE}$ = V <sub>IH</sub> , f = 5MHz, V <sub>CC</sub> = 5.5     |                        | 80   | mA   |
| SRAM Output Low Voltage                                       | V <sub>OL</sub>    | I <sub>OL</sub> = 8mA, V <sub>CC</sub> = 4.5   |                        | 0.4  | V    |
| SRAM Output High Voltage                                      | V <sub>OH</sub>    | I <sub>OH</sub> = -4.0mA, V <sub>CC</sub> = 4.5  | 2.4                    |      | V    |
| Flash V <sub>CC</sub> Active Current for Read (1)             | I <sub>CC1</sub>   | FCS = V <sub>IL</sub> , $\overline{OE}$ = $\overline{SCS}$ = V <sub>IH</sub>                                       |                        | 220  | mA   |
| Flash V <sub>CC</sub> Active Current for Program or Erase (2) | I <sub>CC2</sub>   | FCS = V <sub>IL</sub> , $\overline{OE}$ = $\overline{SCS}$ = V <sub>IH</sub>                                       |                        | 280  | mA   |
| Flash Output Low Voltage                                      | V <sub>OL</sub>    | I <sub>OL</sub> = 8.0mA, V <sub>CC</sub> = 4.5   |                        | 0.45 | V    |
| Flash Output High Voltage                                     | V <sub>OH1</sub>   | I <sub>OH</sub> = -2.5 mA, V <sub>CC</sub> = 4.5   | 0.85 x V <sub>CC</sub> |      | V    |
| Flash Output High Voltage                                     | V <sub>OH2</sub>   | I <sub>OH</sub> = -100 µA, V <sub>CC</sub> = 4.5   | V <sub>CC</sub> - 0.4  |      | V    |
| Flash Low V <sub>CC</sub> Lock Out Voltage                    | V <sub>LKO</sub>   |  | 3.2                    |      | V    |

**NOTES:**

- The I<sub>CC</sub> current listed includes both the DC operating current and the frequency dependent component (@ 5 MHz). The frequency component typically is less than 2 mA/MHz, with OE at V<sub>IH</sub>.
- I<sub>CC</sub> active while Embedded Algorithm (program or erase) is in progress.
- DC test conditions: V<sub>IL</sub> = 0.3V, V<sub>IH</sub> = V<sub>CC</sub> - 0.3V



**SRAM AC CHARACTERISTICS**  
( $V_{CC} = 5.0V$ ,  $T_A = -55^{\circ}C$  TO  $+125^{\circ}C$ )

| Parameter                          | Symbol      | -25 |     | Unit |
|------------------------------------|-------------|-----|-----|------|
|                                    |             | Min | Max |      |
| <b>Read Cycle</b>                  |             |     |     |      |
| Read Cycle Time                    | $t_{RC}$    | 25  |     | ns   |
| Address Access Time                | $t_{AA}$    |     | 25  | ns   |
| Output Hold from Address Change    | $t_{OH}$    | 0   |     | ns   |
| Chip Select Access Time            | $t_{ACS}$   |     | 25  | ns   |
| Output Enable to Output Valid      | $t_{OE}$    |     | 15  | ns   |
| Chip Select to Output in Low Z     | $t_{CLZ}^1$ | 3   |     | ns   |
| Output Enable to Output in Low Z   | $t_{OLZ}^1$ | 0   |     | ns   |
| Chip Disable to Output in High Z   | $t_{CHZ}^1$ |     | 12  | ns   |
| Output Disable to Output in High Z | $t_{OHZ}^1$ |     | 12  | ns   |

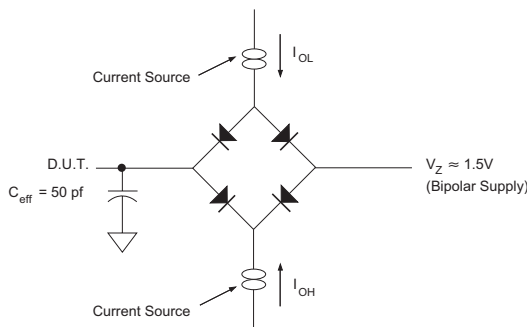
1. This parameter is guaranteed by design but not tested.

**SRAM AC CHARACTERISTICS**  
( $V_{CC} = 5.0V$ ,  $T_A = -55^{\circ}C$  TO  $+125^{\circ}C$ )

| Parameter                        | Symbol      | -25 |     | Unit |
|----------------------------------|-------------|-----|-----|------|
|                                  |             | Min | Max |      |
| <b>Write Cycle</b>               |             |     |     |      |
| Write Cycle Time                 | $t_{WC}$    | 25  |     | ns   |
| Chip Select to End of Write      | $t_{CW}$    | 20  |     | ns   |
| Address Valid to End of Write    | $t_{AW}$    | 20  |     | ns   |
| Data Valid to End of Write       | $t_{DW}$    | 15  |     | ns   |
| Write Pulse Width                | $t_{WP}$    | 20  |     | ns   |
| Address Setup Time               | $t_{AS}$    | 0   |     | ns   |
| Address Hold Time                | $t_{AH}$    | 0   |     | ns   |
| Output Active from End of Write  | $t_{OW}^1$  | 3   |     | ns   |
| Write Enable to Output in High Z | $t_{WHZ}^1$ |     | 15  | ns   |
| Data Hold from Write Time        | $t_{DH}$    | 0   |     | ns   |

1. This parameter is guaranteed by design but not tested.

**FIG. 2 AC TEST CIRCUIT**



**AC TEST CONDITIONS**

| Parameter                        | Typ                           | Unit |
|----------------------------------|-------------------------------|------|
| Input Pulse Levels               | $V_{IL} = 0$ , $V_{IH} = 3.0$ | V    |
| Input Rise and Fall              | 5                             | ns   |
| Input and Output Reference Level | 1.5                           | V    |
| Output Timing Reference Level    | 1.5                           | V    |

**Notes:**

- $V_Z$  is programmable from  $-2V$  to  $+7V$ .
- $I_{OL}$  &  $I_{OH}$  programmable from  $0$  to  $16mA$ .
- Tester Impedance  $Z_0 = 75 \Omega$ .
- $V_Z$  is typically the midpoint of  $V_{OH}$  and  $V_{OL}$ .
- $I_{OL}$  &  $I_{OH}$  are adjusted to simulate a typical resistive load circuit.
- ATE tester includes jig capacitance.



FIG. 3 SRAM TIMING WAVEFORM - READ CYCLE

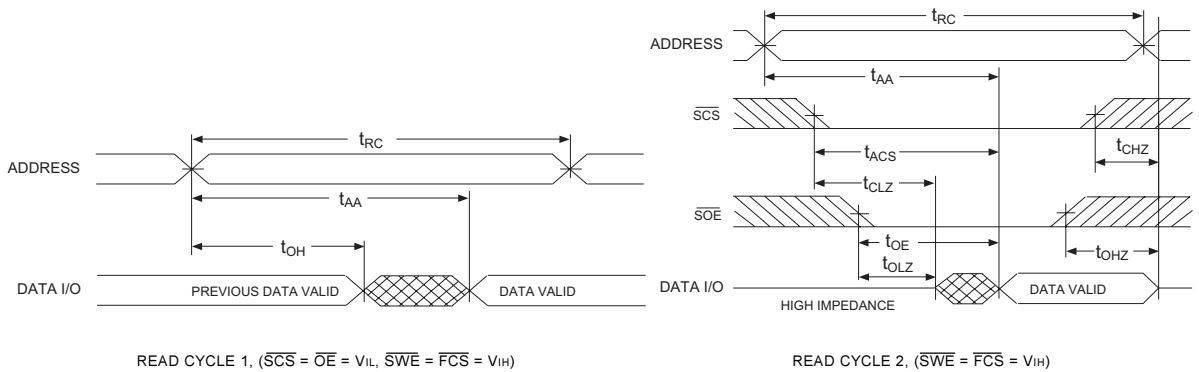


FIG. 4 SRAM WRITE CYCLE -  $\overline{SWE}$  CONTROLLED

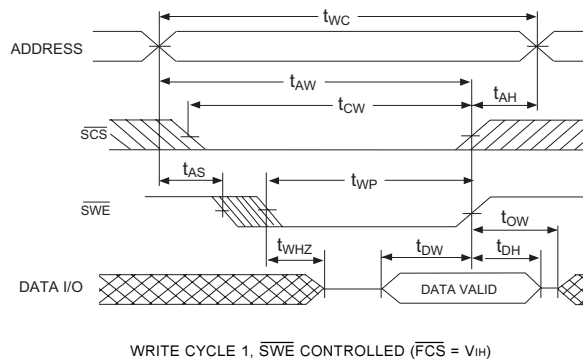
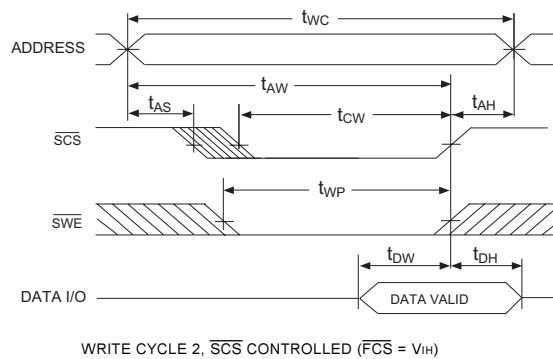


FIG. 5 SRAM WRITE CYCLE -  $\overline{SCS}$  CONTROLLED





**FLASH AC CHARACTERISTICS – WRITE/ERASE/PROGRAM OPERATIONS, FWE CONTROLLED**  
**(V<sub>CC</sub> = 5.0V, T<sub>A</sub> = -55°C TO +125°C)**

| Parameter                                    | Symbol |      | -70 |      | -90 |      | -120 |      | Unit |
|--|--------|------|-----|------|-----|------|------|------|------|
|  |        |      | Min | Max  | Min | Max  | Min  | Max  |      |
| Write Cycle Time                             | tAVAV  | tWC  | 70  |      | 90  |      | 120  |      | ns   |
| Chip Select Setup Time                       | tELWL  | tCS  | 0   |      | 0   |      | 0    |      | ns   |
| Write Enable Pulse Width                     | tWLWH  | tWP  | 35  |      | 45  |      | 50   |      | ns   |
| Address Setup Time                           | tAVWL  | tAS  | 0   |      | 0   |      | 0    |      | ns   |
| Data Setup Time                              | tDVWH  | tDS  | 30  |      | 45  |      | 50   |      | ns   |
| Data Hold Time                               | tWHDX  | tDH  | 0   |      | 0   |      | 0    |      | ns   |
| Address Hold Time                            | tWLAX  | tAH  | 45  |      | 45  |      | 50   |      | ns   |
| Chip Select Hold Time                        | tWHEH  | tCH  | 0   |      | 0   |      | 0    |      | ns   |
| Write Enable Pulse Width High                | tWHWL  | tWPH | 20  |      | 20  |      | 20   |      | ns   |
| Duration of Byte Programming Operation (min) | tWHWH1 |      | 14  |      | 14  |      | 14   |      | µs   |
| Chip and Sector Erase Time                   | tWHWH2 |      | 2.2 | 60   | 2.2 | 60   | 2.2  | 60   | sec  |
| Read Recovery Time Before Write              | tGHWL  |      | 0   |      | 0   |      | 0    |      | µs   |
| V <sub>CC</sub> Set-up Time                  |        | tVCS | 50  |      | 50  |      | 50   |      | µs   |
| Chip Programming Time                        |        |      |     | 12.5 |     | 12.5 |      | 12.5 | sec  |
| Output Enable Setup Time                     |        | tOES | 0   |      | 0   |      | 0    |      | ns   |
| Output Enable Hold Time (1)                  |        | tOEH | 10  |      | 10  |      | 10   |      | ns   |

1. For Toggle and Data Polling.

**FLASH AC CHARACTERISTICS – READ ONLY OPERATIONS**  
**(V<sub>CC</sub> = 5.0V, T<sub>A</sub> = -55°C TO +125°C)**

| Parameter  | Symbol |      | -70 |     | -90 |     | -120 |     | Unit |
|--|--------|------|-----|-----|-----|-----|------|-----|------|
|  |        |      | Min | Max | Min | Max | Min  | Max |      |
| Read Cycle Time  | tAVAV  | tRC  | 70  |     | 90  |     | 120  |     | ns   |
| Address Access Time  | tAVQV  | tACC |     | 70  |     | 90  |      | 120 | ns   |
| Chip Select Access Time  | tELQV  | tCE  |     | 70  |     | 90  |      | 120 | ns   |
| OE to Output Valid   | tGLQV  | tOE  |     | 35  |     | 40  |      | 50  | ns   |
| Chip Select to Output High Z (1)                               | tEHQZ  | tDF  |     | 20  |     | 25  |      | 30  | ns   |
| OE High to Output High Z (1)                                   | tGHQZ  | tDF  |     | 20  |     | 25  |      | 30  | ns   |
| Output Hold from Address, FCS or OE Change, whichever is first | tAXQX  | tOH  | 0   |     | 0   |     | 0    | ns  |      |

1. Guaranteed by design, not tested.

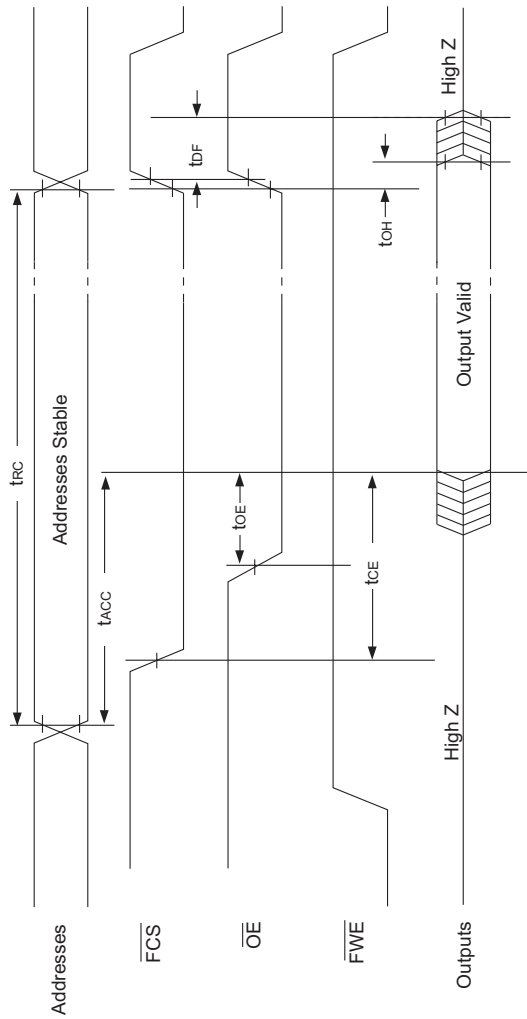


FLASH AC CHARACTERISTICS – WRITE/ERASE/PROGRAM OPERATIONS, FCS CONTROLLED  
(V<sub>CC</sub> = 5.0V, T<sub>A</sub> = -55°C TO +125°C)

| Parameter                         | Symbol |      | -70 |      | -90 |      | -120 |      | Unit |
|-----------------------------------|--------|------|-----|------|-----|------|------|------|------|
|                                   |        |      | Min | Max  | Min | Max  | Min  | Max  |      |
| Write Cycle Time                  | tAVAV  | tWC  | 70  |      | 90  |      | 120  |      | ns   |
| FWE Setup Time                    | tWLEL  | tWS  | 0   |      | 0   |      | 0    |      | ns   |
| FCS Pulse Width                   | tELEH  | tCP  | 35  |      | 45  |      | 50   |      | ns   |
| Address Setup Time                | tAVEL  | tAS  | 0   |      | 0   |      | 0    |      | ns   |
| Data Setup Time                   | tDVEH  | tDS  | 30  |      | 45  |      | 50   |      | ns   |
| Data Hold Time                    | tEHDH  | tDH  | 0   |      | 0   |      | 0    |      | ns   |
| Address Hold Time                 | tELAX  | tAH  | 45  |      | 45  |      | 50   |      | ns   |
| FWE Hold from FWE High            | tEHHH  | tWH  | 0   |      | 0   |      | 0    |      | ns   |
| FCS Pulse Width High              | tEHEL  | tCPH | 20  |      | 20  |      | 20   |      | ns   |
| Duration of Programming Operation | tWHWH1 |      | 14  |      | 14  |      | 14   |      | µs   |
| Duration of Erase Operation       | tWHWH2 |      | 2.2 | 60   | 2.2 | 60   | 2.2  | 60   | sec  |
| Read Recovery before Write        | tGHHL  |      | 0   |      | 0   |      | 0    |      | ns   |
| Chip Programming Time             |        |      |     | 12.5 |     | 12.5 |      | 12.5 | sec  |



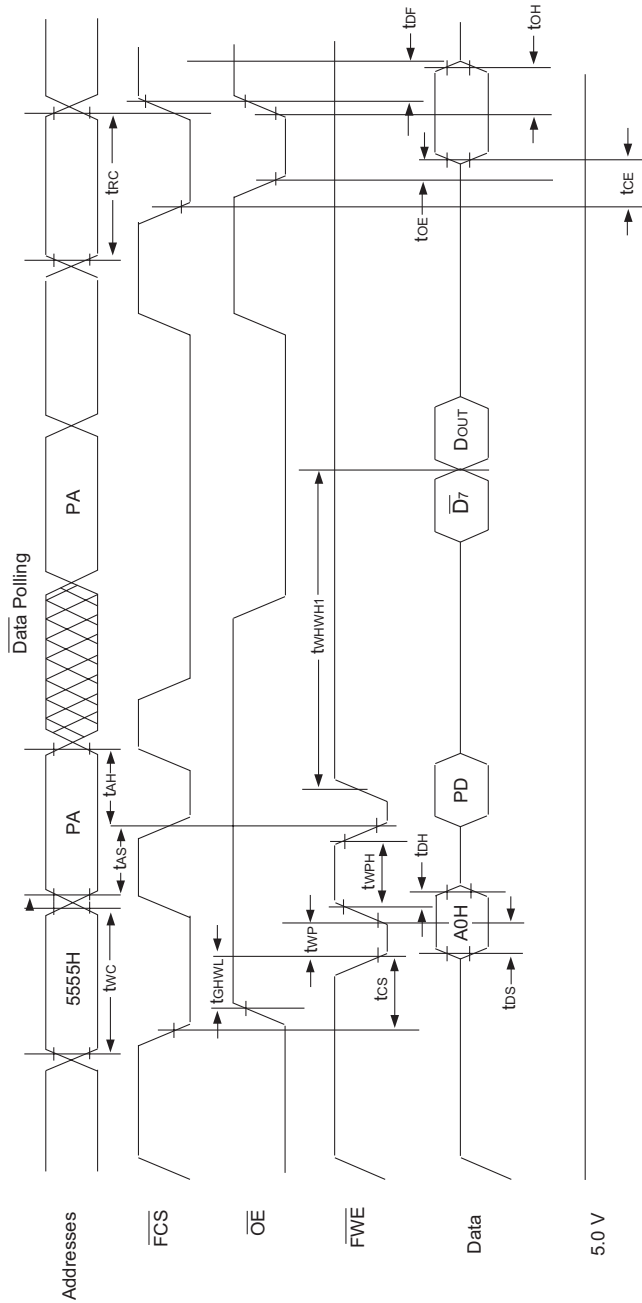
FIG. 6 AC WAVEFORMS FOR FLASH MEMORY READ OPERATIONS



NOTE:  $\overline{SCS} = V_{IH}$



FIG. 7 WRITE/ERASE/PROGRAM OPERATION, FLASH MEMORY FWE CONTROLLED



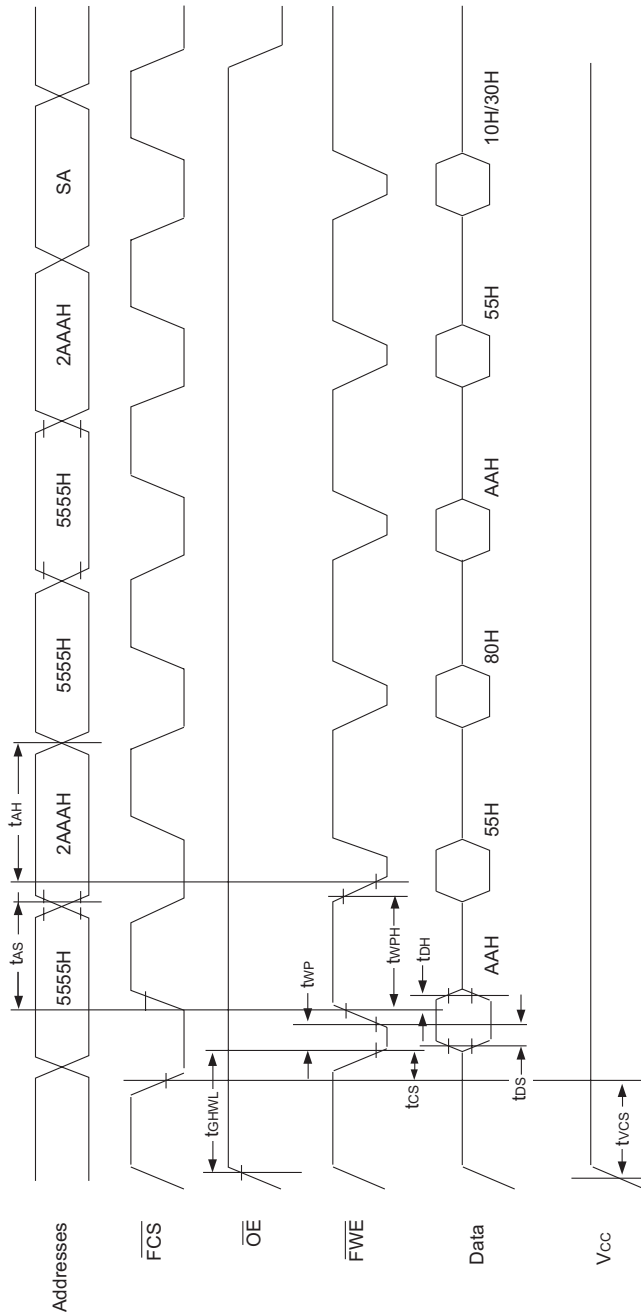
NOTES:

1. PA is the address of the memory location to be programmed.
2. PD is the data to be programmed at byte address.
3.  $\overline{D}_7$  is the output of the complement of the data written to the device.
4.  $D_{OUT}$  is the output of the data written to the device.
5. Figure indicates last two bus cycles of four bus cycle sequence.
6.  $SCS = V_{IH}$





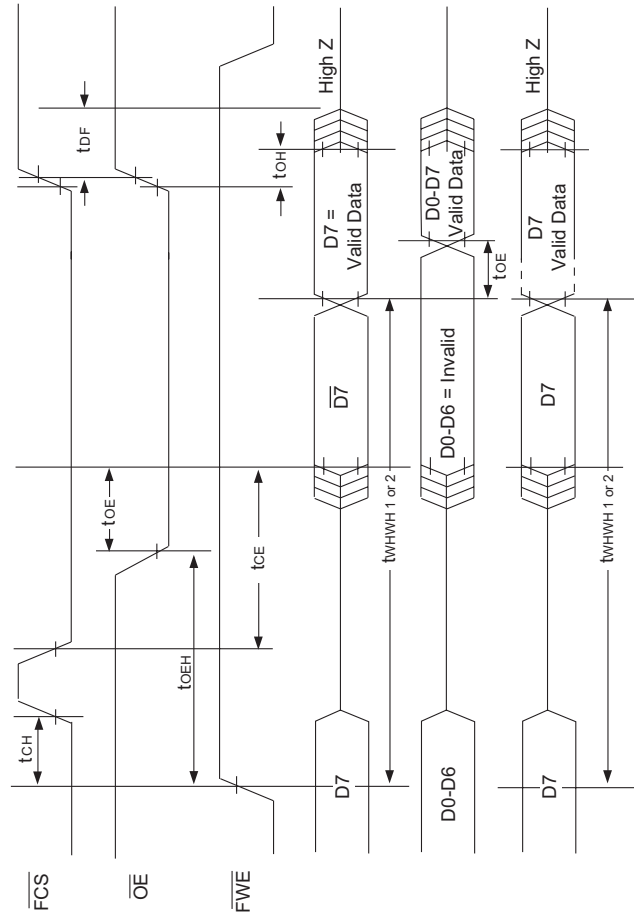
FIG. 8 AC WAVEFORMS CHIP/SECTOR ERASE OPERATIONS FOR FLASH MEMORY



- Notes:
1. SA is the sector address for Sector Erase.
  2. SCS =  $V_{IH}$



FIG. 9 AC WAVEFORMS FOR DATA POLLING DURING EMBEDDED ALGORITHM OPERATIONS FOR FLASH MEMORY

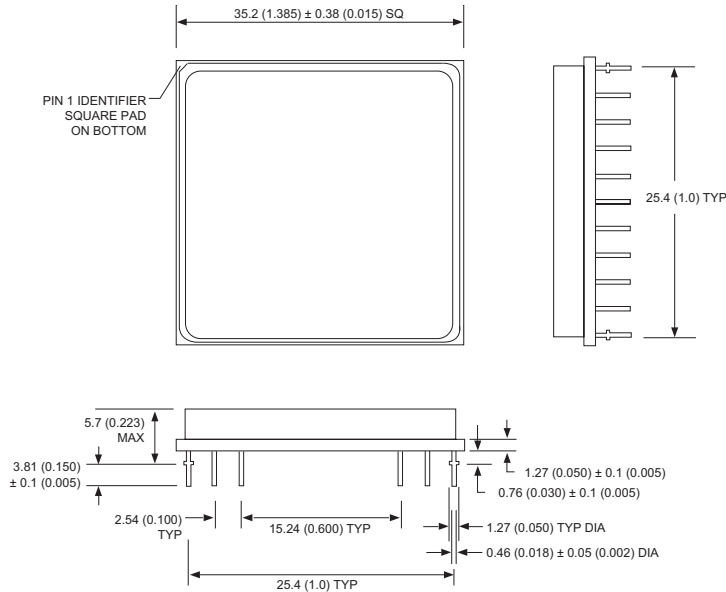


Note:  $\overline{SCS} = V_{IH}$





PACKAGE 402: 66 PIN, PGA TYPE, CERAMIC HEX-IN-LINE PACKAGE, HIP (H2)



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

ORDERING INFORMATION

WSF 128K32 - XX H2 X X

LEAD FINISH:

- Blank = Gold plated leads
- A = Solder dip leads

DEVICE GRADE:

- M = Military Screened -55°C to +125°C
- I = Industrial -40°C to +85°C
- C = Commercial 0°C to +70°C

PACKAGE TYPE:

- H2 = Ceramic Hex In-line Package, HIP (Package 402)

ACCESS TIME (ns)

- 22 = 25ns SRAM and 120ns FLASH
- 29 = 25ns SRAM and 90ns FLASH
- 27 = 25ns SRAM and 70ns FLASH

ORGANIZATION, 128K x 32

Flash PROM

SRAM

WHITE ELECTRONIC DESIGNS CORP.