256MB – 32Mx64 DDR SDRAM UNBUFFERED, w/PLL

FEATURES

- DDR266 and DDR333
- Double-data-rate architecture
- Bi-directional data strobes (DQS)
- Differential clock inputs (CK & CK#)
- Programmable Read Latency 2,2.5 (clock)
- Programmable Burst Length (2,4,8)
- Programmable Burst type (sequential & interleave)
- Edge aligned data output, center aligned data input
- Auto and self refresh
- Serial presence detect
- Power supply: 2.5V ± 0.20V
- Standard 200 pin SO-DIMM package
  - Package height options:
    BD4: 31.75mm (1.25")

NOTE: Consult factory for availability of:
- Lead-Free or RoHS Products
- Vendor source control options
- Industrial temperature option

DESCRIPTION

The WV3EG6434S is a 32Mx64 Double Data Rate SDRAM memory module based on 256Mb DDR SDRAM component. The module consists of eight 32Mx8 DDR SDRAMs in BGA package mounted on a 200 Pin FR4 substrate.

Synchronous design allows precise cycle control with the use of system clock. Data I/O transactions are possible on both edges and Burst Lenths allow the same device to be useful for a variety of high bandwidth, high performance memory system applications.

* This product is under development, is not qualified or characterized and is subject to change or cancellation without notice.

OPERATING FREQUENCIES

	DDR333 @CL=2.5	DDR266 @CL=2	DDR266 @CL=2.5
Clock Speed	166MHz	133MHz	133MHz
CL-t_{RCD}-t_{RP}	2.5-3-3	2-2-2	2.5-3-3

PIN CONFIGURATIONS

Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
1	VREF	51	VSS	101	A9	151	DQ42
2	VREF	52	VSS	102	A8	152	DQ46
3	VSS	53	DQ19	103	VSS	153	DQ43
4	VSS	54	DQ23	104	VSS	154	DQ47
5	DQ0	55	DQ24	105	A7	155	VCC
6	DQ4	56	DQ28	106	A6	156	VCC
7	DQ1	57	VCC	107	A5	157	VCC
8	DQ5	58	VCC	108	A4	158	*CK1#
9	VCC	59	DQ25	109	A3	159	VSS
10	VCC	60	DQ29	110	A2	160	*CK1
11	DQS0	61	DQS3	111	A1	161	VSS
12	DM0	62	DM3	112	A0	162	VSS
13	DQ2	63	VSS	113	VCC	163	DQ48
14	DQ6	64	VSS	114	VCC	164	DQ52
15	VSS	65	DQ26	115	A10/AP	165	DQ49
16	VSS	66	DQ30	116	BA1	166	DQ53
17	DQ3	67	DQ27	117	BA0	167	VCC
18	DQ7	68	DQ31	118	RAS#	168	VCC
19	DQ8	69	VCC	119	WE#	169	DQS6
20	DQ12	70	VCC	120	CAS#	170	DM6
21	VCC	71	NC	121	CS0	171	DQ50
22	VCC	72	NC	122	*CS1#	172	DQ54
23	DQ9	73	NC	123	NC	173	VSS
24	DQ13	74	NC	124	NC	174	VSS
25	DQS1	75	VSS	125	VSS	175	DQ51
26	DM1	76	VSS	126	VSS	176	DQ55
27	VSS	77	*DQS8	127	DQ32	177	DQ56
28	VSS	78	*DM8	128	DQ36	178	DQ60
29	DQ10	79	NC	129	DQ33	179	VCC
30	DQ14	80	NC	130	DQ37	180	VCC
31	DQ11	81	VCC	131	VCC	181	DQ57
32	DQ15	82	VCC	132	VCC	182	DQ61
33	VCC	83	NC	133	DQS4	183	DQS7
34	VCC	84	NC	134	DM4	184	DM7
35	CK0	85	NC	135	DQ34	185	VSS
36	VCC	86	NC	136	DQ38	186	VSS
37	CK0#	87	VSS	137	VSS	187	DQ58
38	VSS	88	VSS	138	VSS	188	DQ62
39	VSS	89	*CK2	139	DQ35	189	DQ59
40	VSS	90	VSS	140	DQ39	190	DQ63
41	DQ16	91	*CK2#	141	DQ40	191	VCC
42	DQ20	92	VCC	142	DQ44	192	VCC
43	DQ17	93	VCC	143	VCC	193	SDA
44	DQ21	94	VCC	144	VCC	194	SA0
45	VCC	95	*CKE1	145	DQ41	195	SCL
46	VCC	96	CKE0	146	DQ45	196	SA1
47	DQS2	97	NC	147	DQS5	197	VCCSPD
48	DM2	98	NC	148	DM5	198	SA2
49	DQ18	99	A12	149	VSS	199	NC
50	DQ22	100	A11	150	VSS	200	NC

PIN NAMES

A0 – A12	Address input (Multiplexed)
BA0-BA1	Bank Select Address
DQ0-DQ63	Data Input/Output
DQS0-DQS7	Data Strobe Input/Output
CK0	Clock input
CK0#	Clock input
CKE0	Clock Enable Input
CS0#	Chip select Input
RAS#	Row Address Strobe
CAS#	Column Address Strobe
WE#	Write Enable
DM0-DM7	Data-In Mask
VCC	Power Supply
VCCQ	Power Supply for DQS
VSS	Ground
VREF	Power Supply for Reference
VCCSPD	Serial EEPROM Power Supply
SDA	Serial data I/O
SCL	Serial clock
SA0-SA2	Address in EEPROM
VCCID	VCC Identification Flag
NC	No Connect

* These pins are not used in this module.

White Electronic Designs Corp. reserves the right to change products or specifications without notice.

FUNCTIONAL BLOCK DIAGRAM

S0# CKE0

Signal	SDRAM pin	Signal	SDRAM pin
DQS0	DQS (S0#)	DQS4	DQS (S0#)
DM0	DM	DM4	DM
DQ0	I/0 0	DQ32	I/0 0
DQ1	I/0 1	DQ33	I/0 1
DQ2	I/0 2	DQ34	I/0 2
DQ3	I/0 3	DQ35	I/0 3
DQ4	I/0 4	DQ36	I/0 4
DQ5	I/0 5	DQ37	I/0 5
DQ6	I/0 6	DQ38	I/0 6
DQ7	I/0 7	DQ39	I/0 7
DQS1	DQS (S1#)	DQS5	DQS (S1#)
DM1	DM	DM5	DM
DQ8	I/0 0	DQ40	I/0 0
DQ9	I/0 1	DQ41	I/0 1
DQ10	I/0 2	DQ42	I/0 2
DQ11	I/0 3	DQ43	I/0 3
DQ12	I/0 4	DQ44	I/0 4
DQ13	I/0 5	DQ45	I/0 5
DQ14	I/0 6	DQ46	I/0 6
DQ15	I/0 7	DQ47	I/0 7
DQS2	DQS (S0#)	DQS6	DQS (S0#)
DM2	DM	DM6	DM
DQ16	I/0 0	DQ48	I/0 0
DQ17	I/0 1	DQ49	I/0 1
DQ18	I/0 2	DQ50	I/0 2
DQ19	I/0 3	DQ51	I/0 3
DQ20	I/0 4	DQ52	I/0 4
DQ21	I/0 5	DQ53	I/0 5
DQ22	I/0 6	DQ54	I/0 6
DQ23	I/0 7	DQ55	I/0 7
DQS3	DQS (S1#)	DQS7	DQS (S1#)
DM3	DM	DM7	DM
DQ24	I/0 0	DQ56	I/0 0
DQ25	I/0 1	DQ57	I/0 1
DQ26	I/0 2	DQ58	I/0 2
DQ27	I/0 3	DQ59	I/0 3
DQ28	I/0 4	DQ60	I/0 4
DQ29	I/0 5	DQ61	I/0 5
DQ30	I/0 6	DQ62	I/0 6
DQ31	I/0 7	DQ63	I/0 7

BA0 - BA1 → BA0-BA1: DDR SDRAMs
A0 - A12 → A0-A12: DDR SDRAMs
RAS# → RAS#: SDRAMs
CAS# → CAS#: SDRAMs
WE# → WE#: SDRAMs

Serial PD
SCL, WP, SDA
A0 A1 A2
SA0 SA1 SA2

VCCSPD — SPD
VCC/VCCQ — DDR SDRAM
VREF — DDR SDRAM
VSS — DDR SDRAM

CK0, CK0# → PLL → DDR SDRAM, DDR SDRAM, DDR SDRAM, DDR SDRAM

NOTE: All resistor values are 22 ohms unless otherwise specified.

White Electronic Designs Corp. reserves the right to change products or specifications without notice.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Units
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	-0.5 to 3.6	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}, V_{CCQ}	-1.0 to 3.6	V
Storage Temperature	T_{STG}	-55 to +150	°C
Power Dissipation	P_D	8	W
Short Circuit Current	I_{OS}	50	mA

Note:

Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded.

Functional operation should be restricted to recommended operating condition.

Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS

T_A = 0°C to 70°C

Parameter	Symbol	Min	Max	Unit	Note
Supply voltage(for device with a nominal V_{CC} of 2.5V)	V_{CC}	2.3	2.7	V	
I/O Supply voltage	V_{CCQ}	2.3	2.7	V	
I/O Reference voltage	V_{REF}	V_{CCQ}/2-50mV	V_{CCQ}/2+50mV	V	1
I/O Termination voltage (system)	V_{TT}	V_{REF}-0.04	V_{REF}+0.04	V	2
Input logic high voltage	V_{IH}(DC)	V_{REF}+0.15	V_{CCQ}+0.3	V	4
Input logic low voltage	V_{IL}(DC)	-0.3	V_{REF}-0.15	V	4
Input Voltage Level, CK and CK# inputs	V_{IN}(DC)	-0.3	V_{CCQ}+0.3	V	
Input Differential Voltage, CK and CK# inputs	V_{ID}(DC)	0.3	V_{CCQ}+0.6	V	3
Input crossing point voltage, CK and CK# inputs	V_{IX}(DC)	1.15	1.35	V	5
Input leakage current	I_I	-2	2	uA	
Output leakage current	I_{OZ}	-5	5	uA	
Output High Current(Normal strengh driver); V_{OUT} = V_{TT} + 0.84V	I_{OH}	-16.8		mA	
Output High Current(Normal strengh driver); V_{OUT} = V_{TT} - 0.84V	I_{OL}	16.8		mA	
Output High Current(Half strengh driver); V_{OUT} = V_{TT} + 0.45V	I_{OH}	-9		mA	
Output High Current(Half strengh driver); V_{OUT} = V_{TT} - 0.45V	I_{OL}	9		mA	

Notes:

1. Includes ± 25mV margin for DC offset on V_{REF}, and a combined total of ± 50mV margin for all AC noise and DC offset on V_{REF}, bandwidth limited to 20MHz. The DRAM must accommodate DRAM current spikes on V_{REF} and internal DRAM noise coupled TO V_{REF}, both of which may result in V_{REF} noise. V_{REF} should be de-coupled with an inductance of ≤ 3nH.
2. V_{TT} is not applied directly to the device. V_{TT} is a system supply for signal termination resistors, is expected to be set equal to V_{REF}, and must track variations in the DC level of V_{REF}
3. V_{ID} is the magnitude of the difference between the input level on CK and the input level on CK.
4. These parameters should be tested at the pin on actual components and may be checked at either the pin or the pad in simulation. The AC and DC input specifications are relative to a V_{REF} envelop that has been bandwidth limited to 200MHZ.
5. The value of V_{IX} is expected to equal 0.5*V_{CCQ} of the transmitting device and must track variations in the dc level of the same.

CAPACITANCE

T_A = 25°C, f = 1MHz, V_{CC} = 2.5V, V_{REF} =2.5V ± 200mV

Parameter	Symbol	Max	Unit
Input Capacitance (A0-A12)	C_{IN1}	21	pF
Input Capacitance (RAS#, CAS#, WE#)	C_{IN2}	21	pF
Input Capacitance (CKE0)	C_{IN3}	21	pF
Input Capacitance (CK0,CK0#)	C_{IN4}	3	pF
Input Capacitance (CS0#)	C_{IN5}	12	pF
Input Capacitance (DQM0-DQM8)	C_{IN6}	10	pF
Input Capacitance (BA0-BA1)	C_{IN7}	21	pF
Data input/output capacitance (DQ0-DQ63)(DQS)	C_{OUT}	10	pF

White Electronic Designs Corp. reserves the right to change products or specifications without notice.

I_{DD} SPECIFICATIONS AND TEST CONDITIONS

Recommended operating conditions, 0°C ≤ T_A ≤ 70°C, V_{CCQ} = 2.5V ±0.2V, V_{CC} = 2.5V ±0.2V

			DDR333@ CL=2.5	DDR266@ CL=2	DDR266@ CL=2.5	
Parameter	Symbol	Conditions	Max	Max	Max	Units
Operating Current	I_{DD0}	One device bank; Active - Precharge; t_{RC}=t_{RC}(MIN); t_{CK}=t_{CK}(MIN); DQ,DM and DQS inputs changing once per clock cycle; Address and control inputs changing once every two cycles.	720	640	640	mA
Operating Current	I_{DD1}	One device bank; Active-Read-Precharge; Burst = 2; t_{RC}=t_{RC}(MIN);t_{CK}=t_{CK}(MIN); Iout = 0mA; Address and control inputs changing once per clock cycle.	920	840	840	mA
Precharge Power-Down Standby Current	I_{DD2P}	All device banks idle; Power- down mode; t_{CK}=t_{CK}(MIN); CKE=(low)	24	24	24	mA
Idle Standby Current	I_{DD2F}	CS# = High; All device banks idle; t_{CK}=t_{CK}(MIN); CKE = high; Address and other control inputs changing once per clock cycle. Vin = Vref for DQ, DQS and DM.	240	200	200	mA
Precharge Quiet Standby Current	I_{DD2Q}	CS# > = V_{IH}(min); All banks idle; CKE > = V_{IH}(min); t_{CK} = 100Mhz for DDR200, 133Mhz for DDR266A & DDR266B; Address and other control inputs stable with keeping >= V_{IH}(min) or = < V_{IL}(max); V_{IN} = V_{REF} for DQ, DQS and DM	200	185	185	mA
Active Power-Down Standby Current	I_{DD3P}	One device bank active; Power-down mode; t_{CK}(MIN); CKE=(low)	280	240	240	mA
Active Standby Current	I_{DD3N}	CS# = High; CKE = High; One device bank; Active-Precharge; t_{RC}=t_{RAS}(MAX); t_{CK}=t_{CK}(MIN); DQ, DM and DQS inputs changing twice per clock cycle; Address and other control inputs changing once per clock cycle.	440	360	360	mA
Operating Current	I_{DD4R}	Burst = 2; Reads; Continous burst; One device bank active;Address and control inputs changing once per clock cycle; t_{CK}=t_{CK}(MIN); Iout = 0mA.	1280	1120	1120	mA
Operating Current	I_{DD4W}	Burst = 2; Writes; Continous burst; One device bank active; Address and control inputs changing once per clock cycle; t_{CK}=t_{CK}(MIN); DQ,DM and DQS inputs changing twice per clock cycle.	1280	1080	1080	mA
Auto Refresh Current	I_{DD5}	t_{RC}=t_{RC}(MIN)	1360	1280	1280	mA
Self Refresh Current	I_{DD6}	CKE ≤ 0.2V	24	24	24	mA
Operating Current	I_{DD7A}	Four bank interleaving Reads (BL=4) with auto precharge with t_{RC}=t_{RC} (MIN); t_{CK}=t_{CK}(MIN); Address and control inputs change only during Active Read or Write commands.	2240	2080	2080	mA

Note: I_{DD} speicification is based on Samsung components. Other DRAM manufacturers specification may be different.

White Electronic Designs Corp. reserves the right to change products or specifications without notice.

DETAILED TEST CONDITIONS FOR DDR SDRAM I_{DD1} & I_{DD7A}

I_{DD1} : OPERATING CURRENT : ONE BANK

1. Typical Case : V_{CC}=2.5V, T=25°C
2. Worst Case : V_{CC}=2.7V, T=10°C
3. Only one bank is accessed with t_{RC} (min), Burst Mode, Address and Control inputs on NOP edge are changing once per clock cycle. I_{OUT} = 0mA
4. Timing Patterns :
   - DDR200 (100 MHz, CL=2) : t_{CK}=10ns, CL2, BL=4, t_{RCD}=2*t_{CK}, t_{RAS}=5*t_{CK}
     Read : A0 N R0 N N P0 N A0 N - repeat the same timing with random address changing; 50% of data changing at every burst
   - DDR266 (133MHz, CL=2.5) : t_{CK}=7.5ns, CL=2.5, BL=4, t_{RCD}=3*t_{CK}, t_{RC}=9*t_{CK}, t_{RAS}=5*t_{CK}
     Read : A0 N N R0 N P0 N N N A0 N - repeat the same timing with random address changing; 50% of data changing at every burst
   - DDR266 (133MHz, CL=2) : t_{CK}=7.5ns, CL=2, BL=4, t_{RCD}=3*t_{CK}, t_{RC}=9*t_{CK}, t_{RAS}=5*t_{CK}
     Read : A0 N N R0 N P0 N N N A0 N - repeat the same timing with random address changing; 50% of data changing at every burst
   - DDR333 (166MHz, CL=2.5) : t_{CK}=6ns, BL=4, t_{RCD}=10*t_{CK}, t_{RAS}=7*t_{CK}
     Read : A0 N N R0 N P0 N N N A0 N - repeat the same timing with random address changing; 50% of data changing at every burst

I_{DD7A} : OPERATING CURRENT : FOUR BANKS

1. Typical Case : V_{CC}=2.5V, T=25°C
2. Worst Case : V_{CC}=2.7V, T=10°C
3. Four banks are being interleaved with t_{RC} (min), Burst Mode, Address and Control inputs on NOP edge are not changing. Iout=0mA
4. Timing Patterns :
   - DDR200 (100 MHz, CL=2) : t_{CK}=10ns, CL2, BL=4, t_{RRD}=2*t_{CK}, t_{RCD}=3*t_{CK}, Read with Autoprecharge
     Read : A0 N A1 R0 A2 R1 A3 R2 A0 R3 A1 R0 - repeat the same timing with random address changing; 100% of data changing at every burst
   - DDR266 (133MHz, CL=2.5) : t_{CK}=7.5ns, CL=2.5, BL=4, t_{RRD}=3*t_{CK}, t_{RCD}=3*t_{CK}
     Read with Autoprecharge
     Read : A0 N A1 R0 A2 R1 A3 R2 N R3 A0 N A1 R0 - repeat the same timing with random address changing; 100% of data changing at every burst
   - DDR266 (133MHz, CL=2) : t_{CK}=7.5ns, CL2=2, BL=4, t_{RRD}=2*t_{CK}, t_{RCD}=2*t_{CK}
     Read : A0 N A1 R0 A2 R1 A3 R2 N R3 A0 N A1 R0 - repeat the same timing with random address changing; 100% of data changing at every burst
   - DDR333 (166MHz, CL=2.5) : t_{CK}=6ns, BL=4, t_{RRD}=3*t_{CK}, t_{RCD}=3*t_{CK}, Read with Autoprecharge
     Read : A0 N A1 R0 A2 R1 A3 R2 N R3 A0 N A1 R0 - repeat the same timing with random address changing; 100% of data changing at every burst

Legend : A = Activate, R = Read, W = Write, P = Precharge, N = NOP

A (0-3) = Activate Bank 0-3
R (0-3) = Read Bank 0-3

White Electronic Designs Corp. reserves the right to change products or specifications without notice.

DDR SDRAM COMPONENT ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

0°C ≤ T_A ≤ 70°C, V_{CC} = +2.5V ±0.2V, V_{CCQ} = +2.5V ±0.2V

Parameter		Symbol	335		262		265		Unit	Note
			Min	Max	Min	Max	Min	Max		
Row cycle time		t_{RC}	60		65		65		ns	
Refresh row cycle time		t_{RFC}	72		75		75		ns	
Row active time		t_{RAS}	42	70K	45	120K	45	120K	ns	
RAS to CAS delay		t_{RCD}	18		20		20		ns	
Row precharge time		t_{RP}	18		20		20		ns	
Row active to Row active delay		t_{RRD}	12		15		15		ns	
Write recovery time		t_{WR}	15		15		15		ns	
Last data in to Read command		t_{WTR}	1		1		1		t_{CK}	
Col. address to Col. address delay		t_{CCD}	1		1		1		t_{CK}	
Clock cycle time	CL=2.0	t_{CK}	7.5	12	7.5	12	10	12	ns	5
	CL=2.5		6	12	7.5	12	7.5	12	ns	5
Clock high level width		t_{CH}	0.45	0.55	0.45	0.55	0.45	0.55	t_{CK}	
Clock low level width		t_{CL}	0.45	0.55	0.45	0.55	0.45	0.55	t_{CK}	
DQS-out access time from CK/CK#		t_{DQSCK}	-0.6	+0.6	-0.75	+0.75	-0.75	+0.75	ns	
Output data access time from CK/CK#		t_{AC}	-0.7	+0.7	-0.75	+0.75	-0.75	+0.75	ns	
Data strobe edge to ouput data edge		t_{DQSQ}	-	0.45	-	0.5	-	0.5	ns	5
Read Preamble		t_{RPRE}	0.9	1.1	0.9	1.1	0.9	1.1	t_{CK}	
Read Postamble		t_{RPST}	0.4	0.6	0.4	0.6	0.4	0.6	t_{CK}	
CK to valid DQS-in		t_{DQSS}	0.75	1.25	0.75	1.25	0.75	1.25	t_{CK}	
DQS-in setup time		t_{WPRES}	0		0		0		ns	2
DQS-in hold time		t_{WPRE}	0.25		0.25		0.25		t_{CK}	
DQS falling edge to CK rising-setup time		t_{DSS}	0.2		0.2		0.2		t_{CK}	
DQS falling edge from CK rising-hold time		t_{DSH}	0.2		0.2		0.2		t_{CK}	
DQS-in high level width		t_{DQSH}	0.35		0.35		0.35		t_{CK}	
DQS-in low level width		t_{DQSL}	0.35		0.35		0.35		t_{CK}	
DQS-in cycle time		t_{DSC}	0.9	1.1	0.9	1.1	0.9	1.1	t_{CK}	
Address and Control Input setup time (fast)		t_{IS}	0.75		0.9		0.9		ns	6
Address and Control Input hold time (fast)		t_{IH}	0.75		0.9		0.9		ns	6
Address and Control Input setup time (slow)		t_{IS}	0.8		1.0		1.0		ns	6
Address and Control Input hold time (slow)		t_{IH}	0.8		1.0		1.0		ns	6
Data-out high impedence time from CK/CK#		t_{HZ}	-0.7	+0.7	-0.75	+0.75	-0.75	+0.75	ns	
Data-out low impedence time from CK/CK#		t_{LZ}	-0.7	+0.7	-0.75	+0.75	-0.75	+0.75	ns	
Input Slew Rate (for input only pins)		$t_{SL(I)}$	0.5		0.5		0.5		V/ns	6
Input Slew Rate (for I/O pins)		$t_{SL(IO)}$	0.5		0.5		0.5		V/ns	7
Output Slew Rate (x4,x8)		$t_{SL(O)}$	1.0	4.5	1.0	4.5	1.0	4.5	V/ns	
Output Slew Rate Matching Ratio (rise to fall)		t_{SLMR}	0.67	1.5	0.67	1.5	0.67	1.5		

Note: AC Timing Parameters are based on Samsung components. Other DRAM Manufacturers parameters may be different.

DDR SDRAM COMPONENT ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (Continued)

0°C ≤ T_A ≤ 70°C, V_{CC} = +2.5V ±0.2V, V_{CCQ} = +2.5V ±0.2V

Parameter	Symbol	335		262		265		Unit	Note
		Min	Max	Min	Max	Min	Max		
Mode register set cycle time	t_{MRD}	12		15		15		ns	
DQ & DM setup time to DQS	t_{DS}	0.45		0.5		0.5		ns	7
DQ & DM hold time to DQS	t_{DH}	0.45		0.5		0.5		ns	7
Control & Address input pulse width	t_{IPW}	2.2		2.2		2.2		ns	
DQ & DM input pulse width	t_{DIPW}	1.75		1.75		1.75		ns	
Power down exit time	t_{PDEX}	6		7.5		7.5		ns	
Exit self refresh to non-Read command	t_{XSNR}	75		75		75		ns	4
Exit self refresh to read command	t_{XSRD}	200		200		200		t_{CK}	
Refresh interval time	t_{REFI}	7.8		7.8		7.8		us	1
Output DQS valid window	t_{QH}	t_{HP}-t_{QHS}	—	t_{HP}-t_{QHS}	—	t_{HP}-t_{QHS}	—	ns	5
Clock half period	t_{HP}	t_{CLmin} or t_{CHmin}	—	t_{CLmin} or t_{CHmin}	—	t_{CLmin} or t_{CHmin}	—	ns	
Data hold skew factor	t_{QHS}		0.55		0.75		0.75	ns	
DQS write postamble time	t_{WPST}	0.4	0.6	0.4	0.6	0.4	0.6	t_{CK}	3
Active to Read with Auto precharge command	t_{RAP}	18		20		20			
Autoprecharge write recovery + Precharge time	t_{DAL}	(t_{WR}/t_{CK}) + (t_{RP}/t_{CK})		(t_{WR}/t_{CK}) + (t_{RP}/t_{CK})		(t_{WR}/t_{CK}) + (t_{RP}/t_{CK})		t_{CK}	

1. Maximum burst refresh cycle : 8
2. The specific requirement is that DQS be valid(High or Low) on or before this CK edge. The case shown(DQS going from High_Z to logic Low) applies when no writes were previously in progress on the bus. If a previous write was in progress, DQS could be High at this time, depending on tDQSS.
3. The maximum limit for this parameter is not a device limit. The device will operate with a great value for this parameter, but system performance (bus turnaround) will degrade accordingly.
4. A write command can be applied with tRCD satisfied after this command.
5. For registered DIMMs, tCL and tCH are >_ 45% of the period including both the half period jitter (tJIT(HP)) of the PLL and the half period jitter due to crosstalk (tJIT(crosstalk)) on the DIMM.
6. Input Setup/Hold Slew Rate Derating

Input Setup/Hold Slew Rate	Δt_{IS}	Δt_{IH}
(V/ns)	(ps)	(ps)
0.5	0	0
0.4	+50	+50
0.3	+100	+100

This derating table is used to increase t_{IS}/t_{IH} in the case where the input slew rate is below 0.5V/ns. Input setup/hold slew rate based on the lesser of AC-AC slew rate and DC-DC slew rate.

7. I/O Setup/Hold Slew Rate Derating

I/O Setup/Hold Slew Rate	Δt_{DS}	Δt_{DH}
(V/ns)	(ps)	(ps)
0.5	0	0
0.4	+75	+75
0.3	+150	+150

This derating table is used to increase t_{DS}/t_{DH} in the case where the I/O slew rate is below 0.5V/ns. I/O setup/hold slew rate based on the lesser of AC-AC slew rate and DC-DC slew rate.

ORDERING INFORMATION FOR BD4

Part Number	Speed	CAS Latency	tRCD	tRP	Height*
WV3EG6434S335BD4	166MHz/333Mb/s	2.5	3	3	31.75 (1.25")
WV3EG6434S262BD4	133MHz/266Mb/s	2	2	2	31.75 (1.25")
WV3EG6434S265BD4	133MHz/266Mb/s	2.5	3	3	31.75 (1.25")

NOTES:

- Consult Factory for availability of Lead-Free or RoHS products. (F = Lead-Free, G = RoHS Compliant)
- Vendor specific part numbers are used to provide memory components source control. The place holder for this is shown as lower case "x" in the part numbers above and is to be replaced with the respective vendors code. Consult factory for qualified sourcing options. (M = Micron, S = Samsung & consult factory for others)
- Consult factory for availability of industrial temperature (-40°C to 85°C) option

PACKAGE DIMENSIONS FOR BD4

67.56
(2.66)
63.60
(2.50)
Full R 2X
2.54
(0 .100)
MAX.
4.00 ±0.10
(0.16 ±0.039)
31.75
(1.25)
20.00
(0.79)
6.00
(0.24)
1
39
41
199
3.98
(0.157)
MIN.
2.15
(0.086)
11.40
(0.456)
47.40
(1.896)
2- 1.80
(0.07)
1.0 ± 0.1
(0.039 ± 0.004)
4.20
(0.17)
2.40
(0.096)
1.80
(0.07)

* ALL DIMENSIONS ARE IN MILLIMETERS AND (INCHES)
TOLERANCES: ± 0.15 (0.006) UNLESS OTHERWISE SPECIFIED

Document Title

256MB – 32Mx64 DDR SDRAM UNBUFFERED, w/PLL

Revision History

Rev #	History	Release Date	Status
Rev 0	Created	4-05	Advanced