



2GB – 2x128Mx72 DDR2 SDRAM REGISTERED, w/PLL

FEATURES

- 240-pin, dual in-line memory module
- Fast data transfer rates: PC2-4200 and PC2-3200
- Utilizes 533 and 400 Mb/s DDR2 SDRAM components
- $V_{CC} = V_{CCQ} = 1.8V \pm 0.1V$
- $V_{CCSPD} = 1.7V$ to 3.6V
- JEDEC standard 1.8V I/O (SSTL_18-compatible)
- Differential data strobe (DQS, DQS#) option
- Four-bit prefetch architecture
- DLL to align DQ and DQS transitions with CK
- Multiple internal device banks for concurrent operation
- Supports duplicate output strobe (RDQS/RDQS#)
- Programmable CAS# latency (CL): 3 and 4
- Adjustable data-output drive strength
- On-die termination (ODT)
- Serial Presence Detect (SPD) with EEPROM
- 64ms: 8,192 cycle refresh
- Gold edge contacts
- Product is lead-free
- RoHS compliant
- Dual Rank
- Package option
 - 240 Pin DIMM
 - PCB – 29.97mm (1.18")

DESCRIPTION

The WV3HG2128M72AER is a 128Mx72 Double Data Rate DDR2 SDRAM high density module. This memory module consists of thirty six 128Mx4 bit with 4 banks DDR2 Synchronous DRAMs in FBGA packages, mounted on a 240-pin DIMM FR4 substrate.

* This product is under development, is not qualified or characterized and is subject to change or cancellation without notice.

NOTE: Consult factory for availability of:

- Vendor source control options
- Industrial temperature option

OPERATING FREQUENCIES

	PC2-3200	PC2-4200
Clock Speed	200MHz	266MHz
CL-tRCD-tRP	3-3-3	4-4-4



PIN CONFIGURATION

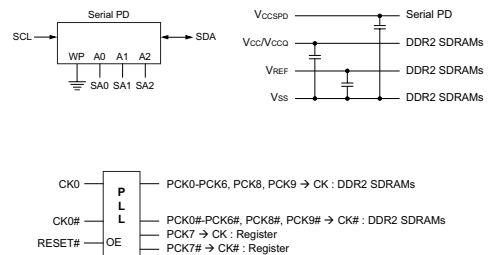
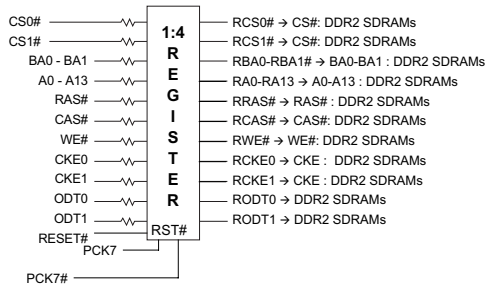
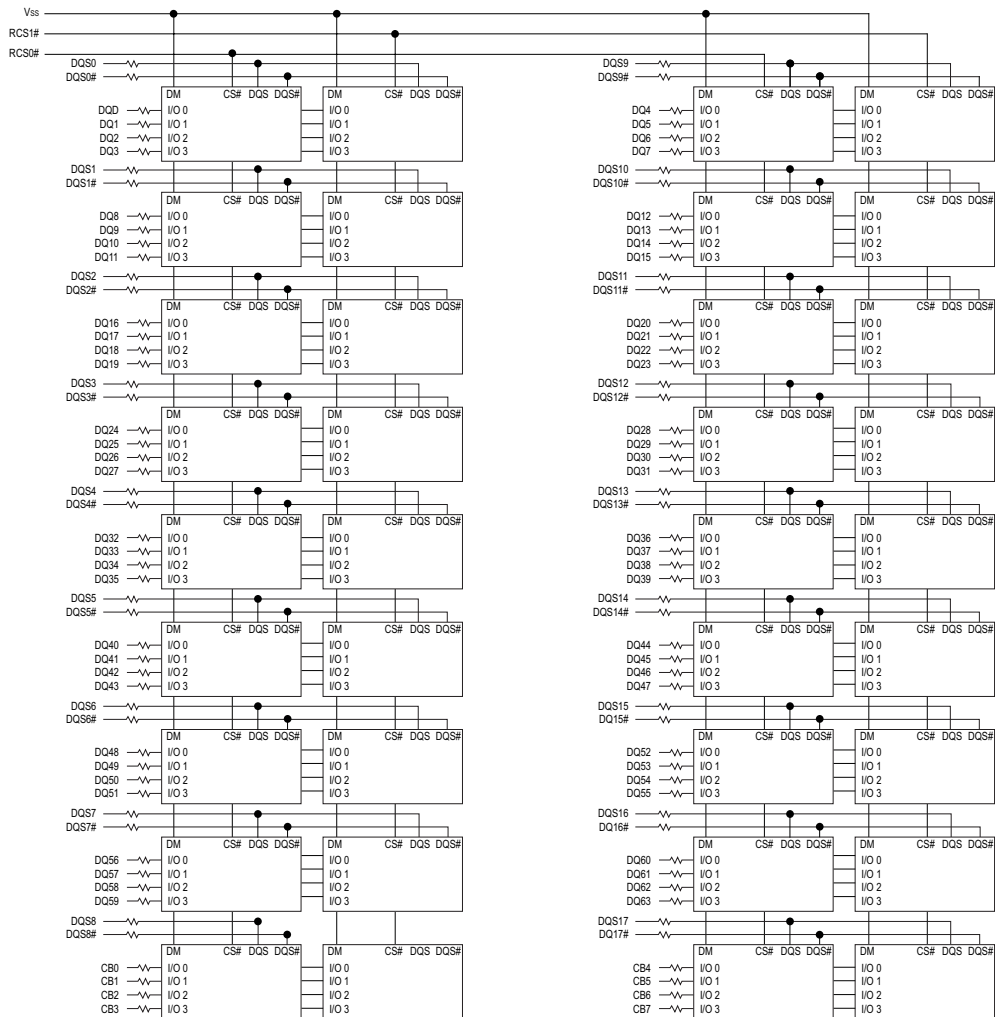
Pin No.	Symbol	Pin No.	Symbol	Pin No.	Symbol	Pin No.	Symbol
1	VREF	61	A4	121	Vss	181	Vccq
2	Vss	62	Vccq	122	DQ4	182	A3
3	DQ0	63	A2	123	DQ5	183	A1
4	DQ1	64	Vcc	124	Vss	184	Vcc
5	Vss	65	Vss	125	DQS9	185	CK0
6	DQS0#	66	Vss	126	DQS9#	186	CK0#
7	DQS0	67	Vcc	127	Vss	187	Vcc
8	Vss	68	NC	128	DQ6	188	A0
9	DQ2	69	Vcc	129	DQ7	189	Vcc
10	DQ3	70	A10/AP	130	Vss	190	BA1
11	Vss	71	BA0	131	DQ12	191	Vccq
12	DQ8	72	Vccq	132	DQ13	192	RAS#
13	DQ9	73	WE#	133	Vss	193	S0#
14	Vss	74	CAS#	134	DQS10	194	Vccq
15	DQS1#	75	Vccq	135	DQS10#	195	ODT0
16	DQS1	76	CS1#	136	Vss	196	A13
17	Vss	77	ODT1	137	NC	197	Vcc
18	RESET#	78	Vccq	138	NC	198	Vss
19	NC	79	Vss	139	Vss	199	DQ36
20	Vss	80	DQ32	140	DQ14	200	DQ37
21	DQ10	81	DQ33	141	DQ15	201	Vss
22	DQ11	82	Vss	142	Vss	202	DQS13
23	Vss	83	DQS4#	143	DQ20	203	DQS13#
24	DQ16	84	DQS4	144	DQ21	204	Vss
25	DQ17	85	Vss	145	Vss	205	DQ38
26	Vss	86	DQ34	146	DQS11	206	DQ39
27	DQS2#	87	DQ35	147	DQS11#	207	Vss
28	DQS2	88	Vss	148	Vss	208	DQ44
29	Vss	89	DQ40	149	DQ22	209	DQ45
30	DQ18	90	DQ41	150	DQ23	210	Vss
31	DQ19	91	Vss	151	Vss	211	DQS14
32	Vss	92	DQS5#	152	DQ28	212	DQS14#
33	DQ24	93	DQS5	153	DQ29	213	Vss
34	DQ25	94	Vss	154	Vss	214	DQ46
35	Vss	95	DQ42	155	DQS12	215	DQ47
36	DQS3#	96	DQ43	156	DQS12#	216	Vss
37	DQS3	97	Vss	157	Vss	217	DQ52
38	Vss	98	DQ48	158	DQ30	218	DQ53
39	DQ26	99	DQ49	159	DQ31	219	Vss
40	DQ27	100	Vss	160	Vss	220	NC
41	Vss	101	SA2	161	CB4	221	NC
42	CB0	102	NC	162	CB5	222	Vss
43	CB1	103	Vss	163	Vss	223	DQS15
44	Vss	104	DQS6#	164	DQS17	224	DQS15#
45	DQS8#	105	DQS6	165	DQS17#	225	Vss
46	DQS8	106	Vss	166	Vss	226	DQ54
47	Vss	107	DQ50	167	CB6	227	DQ55
48	CB2	108	DQ51	168	CB7	228	Vss
49	CB3	109	Vss	169	Vss	229	DQ60
50	Vss	110	DQ56	170	Vccq	230	DQ61
51	Vccq	111	DQ57	171	CKE1	231	Vss
52	CKE0	112	Vss	172	Vcc	232	DQS16
53	Vcc	113	DQS7#	173	NC	233	DQS16#
54	NC	114	DQS7	174	NC	234	Vss
55	NC	115	Vss	175	Vccq	235	DQ62
56	Vccq	116	DQ58	176	A12	236	DQ63
57	A11	117	DQ59	177	A9	237	Vss
58	A7	118	Vss	178	Vcc	238	VccSPD
59	Vcc	119	SDA	179	A8	239	SA0
60	A5	120	SCL	180	A6	240	SA1

PIN NAMES

Pin Name	Function
A0-A13	Address Inputs
BA0,BA1	SDRAM Bank Address
DQ0-DQ63	Data Input/Output
CB0-CB7	Check Bits
DQS0-DQS17	Data strobes
DQS0#-DQS17#	Data strobes complement
ODT0, ODT1	On-die termination control
CK0,CK0#	Clock Inputs, positive line
CKE0, CKE1	Clock Enables
CS0#, CSI#	Chip Selects
RAS#	Row Address Strobe
CAS#	Column Address Strobe
WE#	Write Enable
SA0-SA2	SPD Address
Vcc	Core and I/O Power (1.8V)
Vccq	I/O Power (1.8V)
Vss	Ground
A10/AP	Address input/ autoprecharge
VREF	Input/Output Reference
VccSPD	SPD Power
NC	Spare pins, No connect



FUNCTIONAL BLOCK DIAGRAM



NOTE: All resistor values are 22 ohms unless otherwise specified.



DC OPERATING CONDITIONS

All voltages referenced to V_{SS}

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Supply voltage	V _{CC}	1.7	1.8	1.9	V	1
I/O Supply voltage	V _{CCQ}	1.7	1.8	1.9	V	4
V _{CCCL} Supply voltage	V _{CCCL}	1.7	1.8	1.9	V	4
I/O Reference voltage	V _{REF}	0.49 x V _{CCQ}	0.50 x V _{CCQ}	0.51 x V _{CCQ}	V	2
I/O Termination voltage	V _{TT}	V _{REF} -0.04	V _{REF}	V _{REF} + 0.04	V	3

Notes:

- V_{CC} V_{CCQ} must track each other. V_{CCQ} must be less than or equal to V_{CC}.
- V_{REF} is expected to equal V_{CCQ}/2 of the transmitting device and to track variations in the DC level of the same. Peak-to-peak noise on V_{REF} may not exceed ±1 percent of the DC value. Peak-to-peak AC noise on V_{REF} may not exceed ±2 percent of V_{REF}. This measurement is to be taken at the nearest V_{REF} bypass capacitor.
- V_{TT} is not applied directly to the device. V_{TT} is a system supply for signal termination resistors, is expected to be set equal to V_{REF} and must track variations in the DC level of V_{REF}.
- V_{CCQ} tracks with V_{CC}; V_{CCCL} track with V_{CC}.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	MIN	MAX	Unit
V _{CC}	Voltage on V _{CC} pin relative to V _{SS}	-1.0	2.3	V
V _{CCQ}	Voltage on V _{CCQ} pin relative to V _{SS}	-0.5	2.3	V
V _{CCCL}	Voltage on V _{CCCL} pin relative to V _{SS}	-0.5	2.3	V
V _{IN} , V _{OUT}	Voltage on any pin relative to V _{SS}	-0.5	2.3	V
T _{STG}	Storage temperature	-55	100	°C
I _L	Input leakage current; Any input 0V < V _{IN} < V _{CC} ; V _{REF} input 0V < V _{IN} < 0.95V; Other pins not under test = 0V	-5	5	µA
I _{OZ}	Output leakage current; 0V < V _{OUT} < V _{CCQ} ; DQs and ODT are disable	-10	-10	µA
I _{VREF}	V _{REF} leakage current; V _{REF} = Valid V _{REF} level	-72	72	µA

CAPACITANCE

T_A=25°C, f=1MHz, V_{CC}=V_{CCQ}= 1.8V

Parameter	Symbol	Min	Max	Unit
Input capacitance (A0 ~ A13, BA0 ~ BA1, RAS#, CAS#, WE#)	C _{IN1}	9	11	pF
Input capacitance (CKE0, CKE1), (ODT0, ODT1)	C _{IN2}	9	11	pF
Input capacitance (CS0#, CS1#)	C _{IN3}	14	18	pF
Input capacitance (CK0, CK0#)	C _{IN4}	6	7	pF
Input capacitance (DQS0 ~ DQS8)	C _{IN5}	9	12	pF
Input capacitance (DQ0 ~ DQ63), (CB0 ~ CB7)	C _{OUT1}	9	12	pF

**OPERATING TEMPERATURE CONDITION**

Parameter	Symbol	Rating	Units	Notes
Operating temperature	T _{OPER}	0 to 85	°C	1, 2

Notes:

1. Operating temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JEDEC JESD51.2
2. At 0 - 85°C, operation temperature range, all DRAM specification will be supported.

INPUT DC LOGIC LEVELAll voltages referenced to V_{SS}

Parameter	Symbol	Min	Max	Unit
Input High (Logic 1) Voltage	V _{IH} (DC)	V _{REF} + 0.125	V _{REF} + 0.300	V
Input Low (Logic 0) Voltage	V _{IL} (DC)	-0.300	V _{REF} - 0.125	V

INPUT AC LOGIC LEVELAll voltages referenced to V_{SS}

Parameter	Symbol	Min	Max	Unit
AC Input High (Logic 1) Voltage	V _{IH} (AC)	V _{REF} + 0.250	—	V
AC Input Low (Logic 0) Voltage DDR2-400 & DDR2-533	V _{IL} (AC)	—	V _{REF} - 0.250	V



DDR2 I_{DD} SPECIFICATIONS AND CONDITIONS

Includes DDR2 SDRAM components only

Symbol	Proposed Conditions	534	403	Units	
I _{DD0*}	Operating one bank active-precharge current; t _{CK} = t _{CK} (I _{DD}), t _{RC} = t _{RC} (I _{DD}), t _{RAS} = t _{RASmin} (I _{DD}); CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING	2284	2284	mA	
I _{DD1*}	Operating one bank active-read-precharge current; I _{OUT} = 0mA; BL = 4, CL = CL(I _{DD}), AL = 0; t _{CK} = t _{CK} (I _{DD}), t _{RC} = t _{RC} (I _{DD}), t _{RAS} = t _{RASmin} (I _{DD}), t _{RCD} = t _{RCD} (I _{DD}); CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus input are switching; Data pattern is same as I _{DD6W}	2554	2554	mA	
I _{DD2P**}	Precharge power-down current; All banks idle; t _{CK} = t _{CK} (I _{DD}); CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	988	988	mA	
I _{DD2Q**}	Precharge quiet standby current; All banks idle; t _{CK} = t _{CK} (I _{DD}); CKE is HIGH, CS# is HIGH; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	1780	1780	mA	
I _{DD2N**}	Precharge standby current; All banks idle; t _{CK} = t _{CK} (I _{DD}); CKE is HIGH, CS# is HIGH; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING	1960	1960	mA	
I _{DD3P**}	Active power-down current; All banks open; t _{CK} = t _{CK} (I _{DD}); CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	Fast PDN Exit MRS(12) = 0mA	1780	1780	mA
		Slow PDN Exit MRS(12) = 1mA	1132	1132	mA
I _{DD3N**}	Active standby current; All banks open; t _{CK} = t _{CK} (I _{DD}), t _{RC} = t _{RC} (I _{DD}); t _{RAS} = t _{RASmax} (I _{DD}); CKE is HIGH, CS# is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING	2500	2500	mA	
I _{DD4W*}	Operating burst write current; All banks open, Continuous burst writes; BL = 4, CL = CL(I _{DD}), AL = 0; t _{CK} = t _{CK} (I _{DD}), t _{RAS} = t _{RASmax} (I _{DD}), t _{RP} = t _{RP} (I _{DD}); CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING	2824	2644	mA	
I _{DD4R*}	Operating burst read current; All banks open, Continuous burst reads, I _{OUT} = 0mA; BL = 4, CL = CL(I _{DD}), AL = 0; t _{CK} = t _{CK} (I _{DD}), t _{RAS} = t _{RASmax} (I _{DD}), t _{RP} = t _{RP} (I _{DD}); CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as I _{DD4W}	2914	2734	mA	
I _{DD5**}	Burst auto refresh current; t _{CK} = t _{CK} (I _{DD}); Refresh command at every t _{RFC} (I _{DD}) interval; CKE is HIGH, CS# is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING	5740	5740	mA	
I _{DD6**}	Self refresh current; CK and CK# at 0V; CKE 0.2V; Other control and address bus inputs are FLOATING; Data bus inputs are FLOATING	Normal	288	288	mA
I _{DD7*}	Operating bank interleave read current; All bank interleaving reads, I _{OUT} = 0mA; BL = 4, CL = CL(I _{DD}), AL = t _{RCD} (I _{DD}) - 1 * t _{CK} (I _{DD}); t _{CK} = t _{CK} (I _{DD}), t _{RC} = t _{RC} (I _{DD}), t _{RRD} = t _{RRD} (I _{DD}), t _{RCD} = 1 * t _{CK} (I _{DD}); CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are STABLE during DESELECTs; Data bus inputs are switching.	4804	4804	mA	

Notes:

I_{DD} specification is based on **SAMSUNG** components. Other DRAM manufacturers specification may be different.

* Value calculated as one module rank in this operating condition, and all other module ranks in I_{DD2P} (CKE LOW) mode.

** Value calculated reflects all module ranks in this operating condition.



AC TIMING PARAMETERS & SPECIFICATIONS

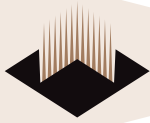
0°C ≤ T_A ≤ +70°C; V_{CCQ} = + 1.8V ± 0.1V, V_{CC} = +1.8V ± 0.1V

AC CHARACTERISTICS			534		403			
PARAMETER			SYMBOL	MIN	MAX	MIN	MAX	UNIT
Clock	Clock cycle time	CL = 4	t _{CK(4)}	3,750	8,000	5,000	8,000	ps
		CL = 3	t _{CK(3)}	5,000	8,000	5,000	8,000	ps
	CK high-level width		t _{CH}	0.45	0.55	0.45	0.55	t _{CK}
	CK low-level width		t _{CL}	0.45	0.55	0.45	0.55	t _{CK}
	Half clock period		t _{HP}	MIN (t _{CH} , t _{CL})		MIN (t _{CH} , t _{CL})		ps
	Clock jitter		t _{JIT}	TBD		TBD		ps
Data	DQ output access time from CK/CK#		t _{AC}	-500	+500	-600	+600	ps
	Data-out high-impedance window from CK/CK#		t _{HZ}		t _{AC} MAX		t _{AC} MAX	ps
	Data-out low-impedance window from CK/CK#		t _{LZ}	t _{AC} MIN	t _{AC} MAX	t _{AC} MIN	t _{AC} MAX	ps
	DQ and DM input setup time relative to DQS		t _{DS}	100		150		
	DQ and DM input hold time relative to DQS		t _{DH}	225		275		
	A DQ and DM input pulse width (for each input)		t _{DLPW}	0.35		0.35		t _{CK}
	Data hold skew factor		t _{QHS}		400		450	ps
	DQ...DQS hold, DQS to first DQ to go nonvalid, per access		t _{QH}	t _{HP} - t _{QHS}		t _{HP} - t _{QHS}		ps
	Data valid output window (DVW)		t _{DVW}	t _{QH} - t _{DQSQ}		t _{QH} - t _{DQSQ}		ns
Data Strobe	DQS input high pulse width		t _{DQSH}	0.35		0.35		t _{CK}
	DQS input low pulse width		t _{DQSL}	0.35		0.35		t _{CK}
	DQS output access time from CK/CK#		t _{DQSCK}	-450	+450	-500	+500	ps
	DQS falling edge to CK rising ... setup time		t _{DSS}	0.2		0.2		t _{CK}
	DQS falling edge from CK rising ... hold time		t _{DSH}	0.2		0.2		t _{CK}
	DQS...DQ skew, DQS to last DQ valid, per group, per access		t _{DQSQ}		300		350	ps
	DQS read preamble		t _{RPRE}	0.9	1.1	0.9	1.1	t _{CK}
	DQS read postamble		t _{RPST}	0.4	0.6	0.4	0.6	t _{CK}
	DQS write preamble setup time		t _{WPRES}	0		0		ps
	DQS write preamble		t _{WPRE}	0.35		0.35		t _{CK}
	DQS write postamble		t _{WPST}	0.4	0.6	0.4	0.6	t _{CK}
	Write command to first DQS latching transition		t _{DQSS}	WL - 0.25	WL + 0.25	WL - 0.25	WL + 0.25	t _{CK}

Notes:

AC specification is based on **SAMSUNG** components. Other DRAM manufacturers specification may be different.

Continued on next page



AC TIMING PARAMETERS (cont'd)
 $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$; $V_{CCQ} = +1.8\text{V} \pm 0.1\text{V}$, $V_{CC} = +1.8\text{V} \pm 0.1\text{V}$

AC CHARACTERISTICS		534		403			
PARAMETER	SYMBOL	MIN	MAX	MIN	MAX	UNIT	
Command and Address	Address and control input pulse width for each input	t _{IPW}	0.6		0.6	t _{CK}	
	Address and control input setup time	t _{IS}	250		250	ps	
	Address and control input hold time	t _{IH}	375		475	ps	
	CAS# to CAS# command delay	t _{CCD}	2		2	t _{CK}	
	ACTIVE to ACTIVE (same bank) command	t _{RC}	60		65	ns	
	ACTIVE bank a to ACTIVE bank b command	t _{RRD}	7.5		7.5	ns	
	ACTIVE to READ or WRITE delay	t _{RCD}	15		15	ns	
	Four Bank Activate period	t _{FAW}	37.5	37.5	37.5	37.5	ns
	ACTIVE to PRECHARGE command	t _{RAS}	45	70,000	45	70,000	ns
	Internal READ to precharge command delay	t _{RTP}	7.5		7.5		ns
	Write recovery time	t _{WR}	15		15		ns
	Auto precharge write recovery + precharge time	t _{DAL}	t _{WR} + t _{RP}		t _{WR} + t _{RP}		ns
	Internal WRITE to READ command delay	t _{WTR}	7.5		10		ns
	PRECHARGE command period	t _{RP}	15		15		ns
	PRECHARGE all command period	t _{RPA}	t _{RP} + t _{CK}		t _{RP} + t _{CK}		ns
	LOAD MODE command cycle time	t _{MRD}	2		2		t _{CK}
	CKE low to CK,CK# uncertainty	t _{DELAY}	4,375		4,375		ns
Self Refresh	REFRESH to REFRESH command interval	t _{RFC}	127.5	70,000	127.5	70,000	ns
	Average periodic refresh interval	t _{REFI}		7.8		7.8	μs
	Exit self refresh to non-READ command	t _{XSNR}	t _{RFC} (MIN) + 10		t _{RFC} (MIN) + 10		ns
	Exit self refresh to READ command	t _{XSRD}	200		200		t _{CK}
	Exit self refresh timing reference	t _{ISXR}	t _{IS}		t _{IS}		ps
ODT	ODT turn-on delay	t _{AO_{ND}}	2		2		t _{CK}
	ODT turn-on	t _{AO_N}	t _{AC} (MIN)	t _{AC} (MAX) + 1000	t _{AC} (MIN)	t _{AC} (MAX) + 1000	ps
	ODT turn-off delay	t _{AO_{FD}}	2.5	2.5	2.5	2.5	t _{CK}
	ODT turn-off	t _{AO_F}	t _{AC} (MIN)	t _{AC} (MAX) + 600	t _{AC} (MIN)	t _{AC} (MAX) + 600	ps
	ODT turn-on (power-down mode)	t _{AO_{NP_D}}	t _{AC} (MIN) + 2000	2 x t _{CK} + t _{AC} (MAX) + 1000	t _{AC} (MIN) + 2000	2 x t _{CK} + t _{AC} (MAX) + 1000	ps
	ODT turn-off (power-down mode)	t _{AO_{FP_D}}	t _{AC} (MIN) + 2000	2.5 x t _{CK} + t _{AC} (MAX) + 1000	t _{AC} (MIN) + 2000	2.5 x t _{CK} + t _{AC} (MAX) + 1000	ps
	ODT to power-down entry latency	t _{AN_{PD}}	3		3		t _{CK}
	ODT power-down exit latency	t _{AX_{PD}}	8		8		t _{CK}
Power-Down	Exit active power-down to READ command, MR[bit12=0]	t _{XARD}	2		2		t _{CK}
	Exit active power-down to READ command, MR[bit12=1]	t _{XARDS}	6 - AL		6 - AL		t _{CK}
	A Exit precharge power-down to any non-READ command.	t _{XP}	2		2		t _{CK}
	CKE minimum high/low time	t _{CKE}	3		3		t _{CK}

Notes:
 AC specification is based on **SAMSUNG** components. Other DRAM manufacturers specification may be different.



ORDERING INFORMATION FOR D6

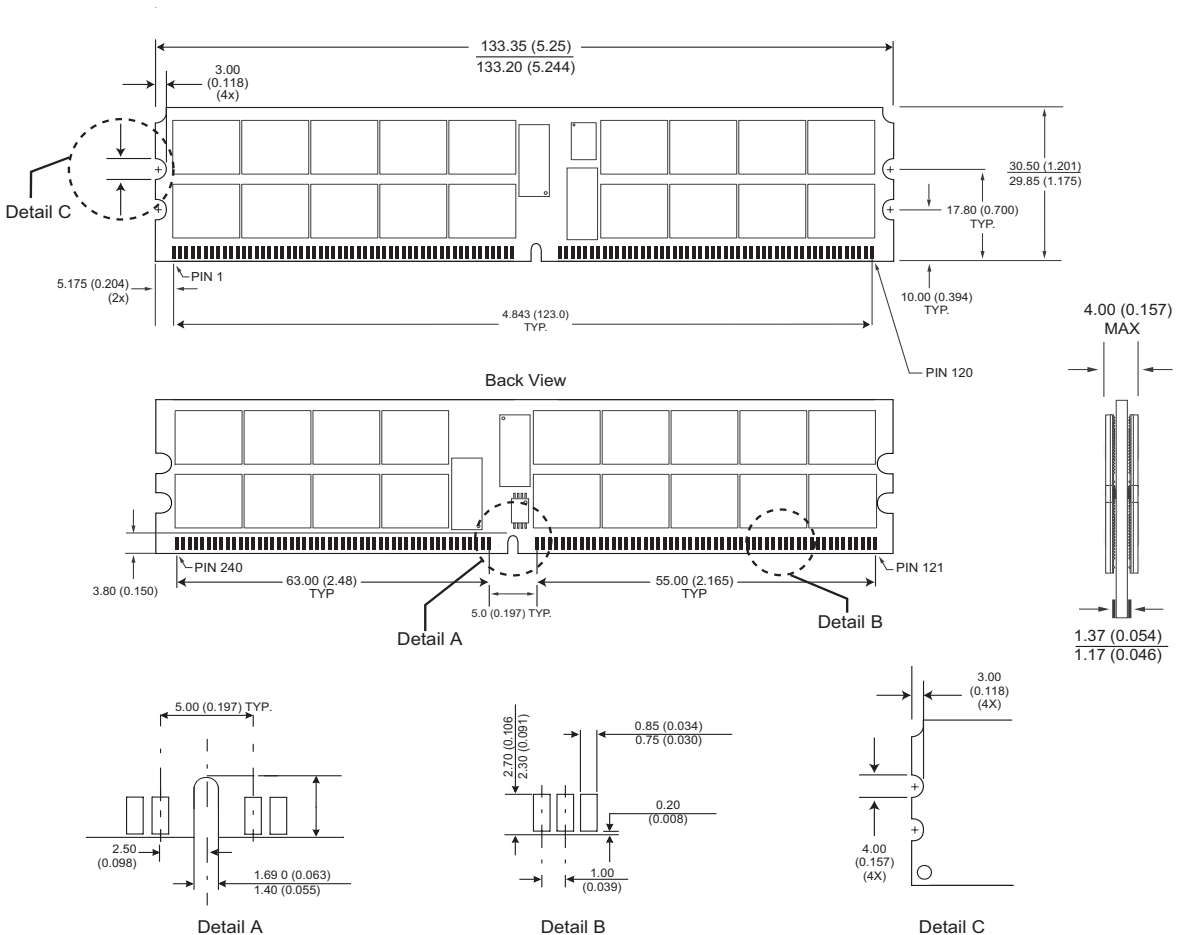
Part Number	Speed	CAS Latency	t _{RC} D	t _{RP}	Height*
WV3HG2128M72AER534D6xG	266MHz/533Mb/s	4	4	4	29.97mm (1.18")
WV3HG2128M72AER403D6xG	200MHz/400Mb/s	3	3	3	29.97mm (1.18")

NOTES:

- RoHS products. ("G" = RoHS Compliant)
- Vendor specific part numbers are used to provide memory component source control. The place holder for this is shown as a lower case "x" in the part numbers above and is to be replaced with respective vendors code. Consult factory for qualified sourcing options. (M = Micron, S = Samsung & consult factory for others)
- Consult factory for availability of industrial temperature (-40°C to 85°C) option

PACKAGE DIMENSIONS FOR D6

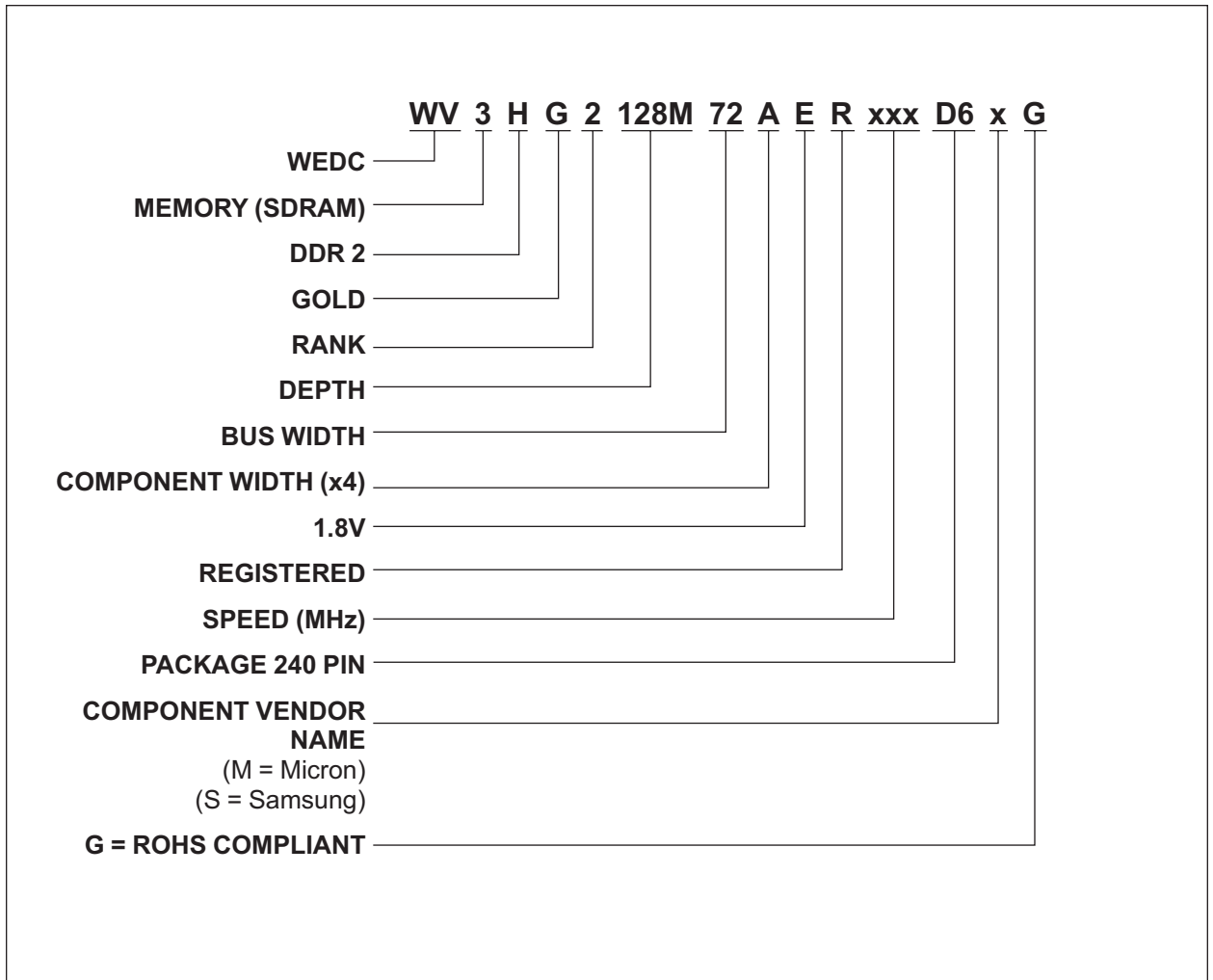
Front View

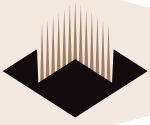


* ALL DIMENSIONS ARE IN MILLIMETERS AND (INCHES)



PART NUMBERING GUIDE





Document Title

2GB – 2x128Mx72 DDR2 SDRAM REGISTERED, w/PLL

Revision History

Rev #	History	Release Date	Status
Rev 0	Created	September 2005	Advanced