Long Distance Digital Display Link Transmitter & Receiver

GigaSTaR® Digital Display Link

The GigaSTaR® Digital Display Link 166/331-series is an innovative high-speed link featuring simultaneous transmission of digital video, audio and bi-directional sideband data over one standard shielded twisted pair cable up to 50 m (500 m with fiber optics). It supports VGA…UXGA as well as Digital TV (DTV) and High-Definition TV (HDTV) formats up to 720p or HDTV1080i with up to 16.7 million colors. The sideband channels provide bandwidth up to 264 Mbps to connect peripheral components like keyboard, mouse, disc drive and audio devices.
Compared to the 165/330-series the 166/331 offer additional features like a tristate pixel interface (Rx only) and an integrated pixel buffer to reducing pixel clock variations. The 166/331 may be used as direct drop-in replacement for the 165/330 under specified conditions.

	VESA Format at 18bit/60Hz	VESA Format at 24bit/60Hz
INDT/R166B	**VGA…WXGA**	**VGA…XGA**
INDT/R331B	**VGA…UXGA**	**VGA…SXGA**
	HDTV (24 bit)	
INDT/R166B	**480p (60fps), 720p (30fps)**	
INDT/R331B	**480p (60fps), 720p (60fps), 1080i (30fps)**	

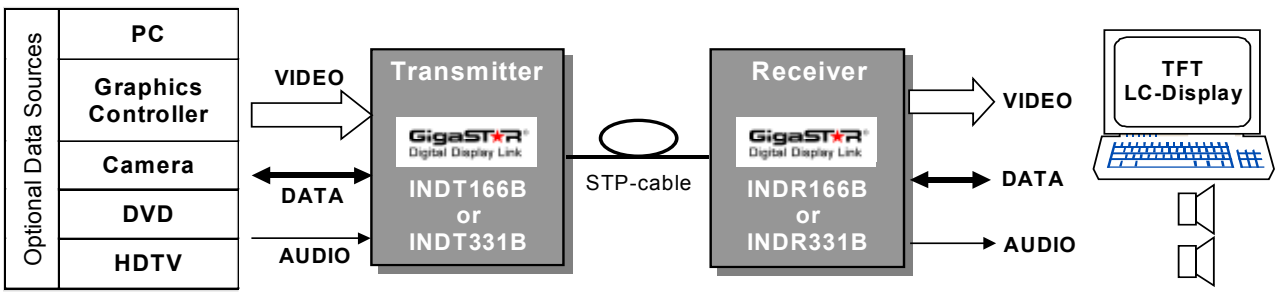
Features:

- Parallel graphics controller and LC-display interfaces:
  – 18- / 24-bit (1 pixel/clock)
  – 36- / 48-bit (2 pixel/clock)
- Pixel data clocking on rising/falling/both clock edges
- Pixel Clock frequency: 24 – 161 MHz
- Direct adaptation to DVI and LDI/LVDS standard interface devices
- 4 channel audio interface (IEC958 compliant S/P-DIF)
- High- and low-speed bi-directional sideband data channels
- Single + 3.3 V power supply
- Extended temperature range: -40 – +85 °C

Applications:

- Long distance multimedia consoles
- High resolution industrial remote terminals
- Video broadcast systems
- Long distance camera links
- Machine vision systems
- Digital TV equipment
- Video Projectors and Home Cinemas
- DVI Extension products

Typical Application:



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1 General Description

The GigaSTaR® Digital Display Link is a high-speed serial and long distance link for video, audio and digital data, which supports the popular VESA and Digital TV standards as well as proprietary video formats from VGA to UXGA with color depth up to 24 bits.

1.1 Link Interface

The INDT/R166B link requires one single twisted pair cable for the high-speed downlink. The INDT/R331B provides double bandwidth by using two twisted pairs. Both devices offer an uplink connection using a twisted pair. The downlink must be established before the uplink can be activated.

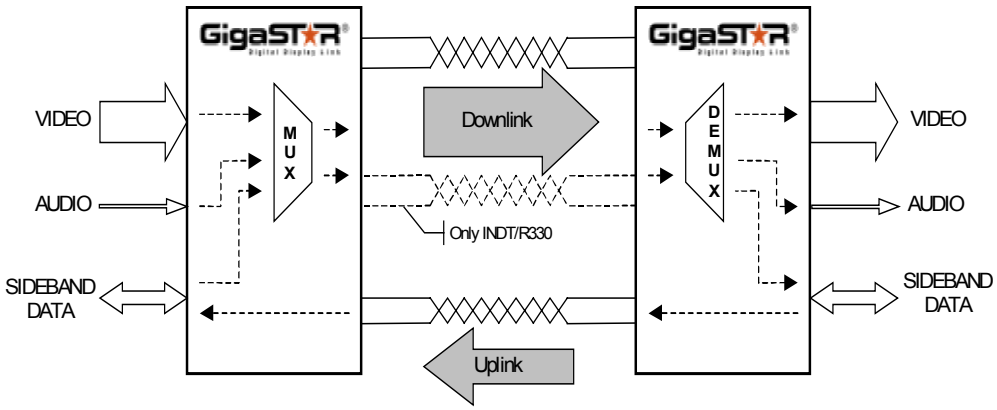


Figure 1.1: GigaSTaR® Digital Display Link Interfaces

The transmitter's and receiver's generic parallel RGB interfaces (CMOS/TTL compatible) support direct connection to the parallel data port of any graphic controller or to any flat panel display with a parallel pixel data port. The bit width of the pixel data path can be scaled to support the 18- or 24-bit mode with 1 pixel/clock, the 36- or 48-bit mode with 2 pixel/clock. Pixel data can be clocked into the transmitter on the rising, falling or on both edges (18-, 24-bit mode) of the pixel clock. Pixel data are provided at the receiver on the rising, falling or on both edges (18-, 24-bit mode) of the pixel clock.

1.1.1 Link Interface Bandwidth

The bandwidth of the downlink is shared between video, audio and sideband data. Disabling audio and/or sideband channels, even partially, increases the available bandwidth for the video data. The video configuration required for VESA or Digital TV (DTV) / High-Definition TV (HDTV) standard compatible video resolutions is shown in **Table 1.1** and **Table 1.2**.

Mode	INDT/R166B configurations			Up to VESA-/DTV-Mode
	High-speed Sideband	Low-speed Sideband	Audio	
1	X	X	X/–	XGA 18 color bits
2	–	X	X	XGA 18 color bits
3	–	–	–	XGA 24 color bits
4	X	X	X	480p(60fps), 720p (30fps)

Table 1.1: INDT/R166B Video Configuration

Mode	INDT/R331B configurations			Up to VESA-/DTV-Mode
	High-speed Sideband	Low-speed Sideband	Audio	
1	X	X	X/–	SXGA 24 color bits
2	–	X	X	UXGA 18 color bits
3	–	–	–	UXGA 18 color bits
4	X	X	X	720p (60fps)
5	X	X	X	1080i (30fps)

Table 1.2: INDT/R331B Video Configuration

Note: Implementation of video modes other than VESA or DTV/HDTV is possible. Special modes may need evaluation.

1.2 Pixel Interface

1.2.1 General Information

The pixel interface is designed to support direct interfacing to any digital graphics device with a parallel data port such as graphic-cards/controllers, CCD cameras or flat panel TFT displays. With standard interface devices the data port can also be adapted to systems with non-generic parallel interfaces such as DVI or LVDS/OpenLDI.

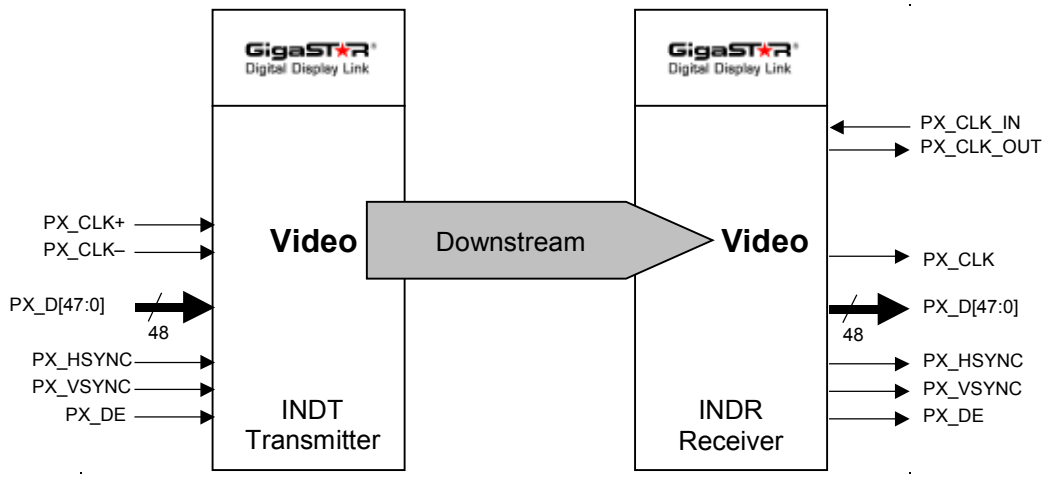


Figure 1.2: Pixel Interface

Signal	Tx[1]	Rx	Description
PX_D[47:0]	IN	OUT	Configurable parallel pixel data interface
PX_CLK+	IN	OUT	Tx Pixel clock 24 – 161 MHz, diff + or single-ended
PX_CLK–	IN	OUT	Tx Pixel clock 24 – 161 MHz, diff –
PX_CLK		OUT	Rx Pixel clock 24 – 161 MHz
PX_CLK_OUT		OUT	Rx Pixel clock 24 – 161 MHz, de-jitter
PC_CLK_IN		IN	Rx Pixel clock 24 – 161 MHz, de-jitter
PX_HSYNC	IN	OUT	Pixel data framing – Horizontal sync pulse
PX_VSYNC	IN	OUT	Pixel data framing – Vertical sync pulse
PX_DE	IN	OUT	Pixel data framing – Data enable

Table 1.3: Pixel Interface Signals

[1] Configurable to 3.3V or 1.8V input levels via V_{REF}-pin.

The transmitter's pixel interface accepts pixel data with a pixel clock frequency of 24 – 161 MHz (full pixel mode). For the Tx side in single-ended mode, PX_CLK+ is the clock input and PX_CLK– has to be tied to GND. A differential pixel clcok mode on the Rx side is not available. All pixel data and pixel clock inputs of the transmitter can be selected through the V_{REF}-pin to either work with conventional graphic controllers with 3.3 V output voltage swing or to work with latest controllers with low voltage swing (1.0 – 2.0 V, see **Figure 3.3: VREF Reference Circuitry**). The pixel data and pixel clock outputs of the receiver provide a 3.3 V CMOS compliant output.

1.2.2 Pixel Interface Modes

The pixel interface is configurable to accommodate all the various graphic interface standards in the market. The width of the pixel interface is a function of the selected operating mode.

- In **full-pixel mode** the bit width of the pixel interface can be set to support an **18- or 24-bit** wide parallel video interface. 1 pixel per sampling edge is transmitted.
- In **double-pixel mode** the bit width of the pixel interface can be set to support a **36- or 48-bit** wide parallel video interface. 2 pixels per sampling edge are transmitted.

1.2.3 Pixel Clock Sampling Modes

The pixel interface can be set to support data sampling at the **rising, falling** or at **both edges** of the pixel clock, depending on the selected mode.

Table 1.4 and , **Figure 1.4**, **Figure 1.5** summarize the various options for configuring the pixel interface.

Pixel Mode	Clock Edge	PX_CLK+	PX_CLK-	Description
18-bit (Full Pixel)	rising	↑	–	18 bits of pixel(n) sampled at rising edge of PX_CLK+
	falling	↓	–	18 bits of pixel(n) sampled at falling edge of PX_CLK+
	both	↑↓	–	18 bits of pixel(n) sampled at both edges of PX_CLK+
24-bit (Full Pixel)	rising	↑	–	24 bits of pixel(n) sampled at rising edge of PX_CLK+
	falling	↓	–	24 bits of pixel(n) sampled at falling edge of PX_CLK+
	both	↑↓	–	24 bits of pixel(n) sampled at both edges of PX_CLK+
36-bit (Double Pixel)	rising	↑	–	18 bits of pixel(n) and 18 bits of pixel(n+1) sampled at rising edge of PX_CLK+
	falling	↓	–	18 bits of pixel(n) and 18 bits of pixel(n+1) sampled at falling edge of PX_CLK+
48-bit (Double Pixel)	rising	↑	–	24 bits of pixel(n) and 24 bits of pixel(n+1) sampled at rising edge of PX_CLK+
	falling	↓	–	24 bits of pixel(n) and 24 bits of pixel(n+1) sampled at falling edge of PX_CLK+

Table 1.4: Overview – Pixel Interface Configurations

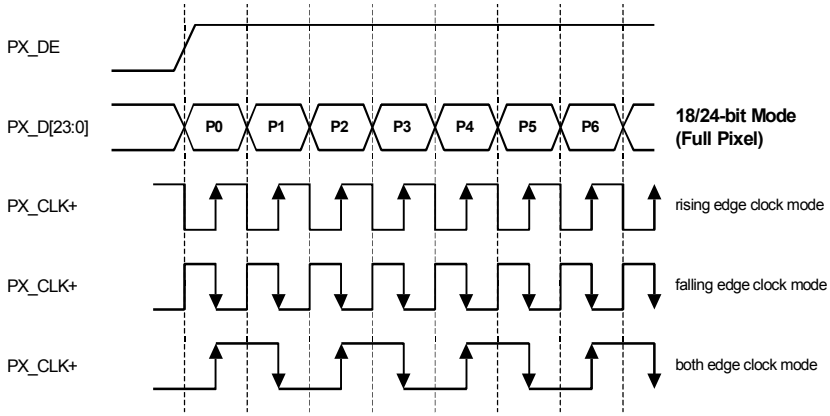


Figure 1.4: Pixel Interface – Full Pixel Modes

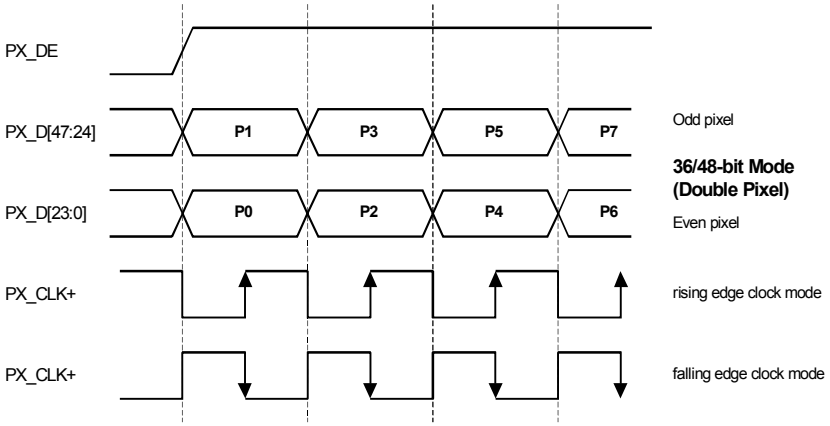


Figure 1.5: Pixel Interface – Double Pixel Modes

1.2.4 Pixel Data I/O Color Bit Mapping

The color bits are mapped to the parallel I/Os as a function of the selected pixel clock (R = Red, G = Green, B = Blue, O = Odd, E = Even).

Data	Full Pixel		Double Pixel	
	18-bit Mode	24-bit Mode	36-bit Mode	48-bit Mode
PX_D47	–	–	RO[5]	RO[7]
PX_D46	–	–	RO[4]	RO[6]
PX_D45	–	–	RO[3]	RO[5]
PX_D44	–	–	RO[2]	RO[4]
PX_D43	–	–	RO[1]	RO[3]
PX_D42	–	–	RO[0]	RO[2]
PX_D41	–	–	–	RO[1]
PX_D40	–	–	–	RO[0]
PX_D39	–	–	GO[5]	GO[7]
PX_D38	–	–	GO[4]	GO[6]
PX_D37	–	–	GO[3]	GO[5]
PX_D36	–	–	GO[2]	GO[4]
PX_D35	–	–	GO[1]	GO[3]
PX_D34	–	–	GO[0]	GO[2]
PX_D33	–	–	–	GO[1]
PX_D32	–	–	–	GO[0]
PX_D31	–	–	BO[5]	BO[7]
PX_D30	–	–	BO[4]	BO[6]
PX_D29	–	–	BO[3]	BO[5]
PX_D28	–	–	BO[2]	BO[4]
PX_D27	–	–	BO[1]	BO[3]
PX_D26	–	–	BO[0]	BO[2]
PX_D25	–	–	–	BO[1]
PX_D24	–	–	–	BO[0]
PX_D23	R[5]	R[7]	RE[5]	RE[7]
PX_D22	R[4]	R[6]	RE[4]	RE[6]
PX_D21	R[3]	R[5]	RE[3]	RE[5]
PX_D20	R[2]	R[4]	RE[2]	RE[4]
PX_D19	R[1]	R[3]	RE[1]	RE[3]
PX_D18	R[0]	R[2]	RE[0]	RE[2]
PX_D17	–	R[1]	–	RE[1]
PX_D16	–	R[0]	–	RE[0]
PX_D15	G[5]	G[7]	GE[5]	GE[7]
PX_D14	G[4]	G[6]	GE[4]	GE[6]
PX_D13	G[3]	G[5]	GE[3]	GE[5]
PX_D12	G[2]	G[4]	GE[2]	GE[4]
PX_D11	G[1]	G[3]	GE[1]	GE[3]
PX_D10	G[0]	G[2]	GE[0]	GE[2]
PX_D9	–	G[1]	–	GE[1]
PX_D8	–	G[0]	–	GE[0]
PX_D7	B[5]	B[7]	BE[5]	BE[7]
PX_D6	B[4]	B[6]	BE[4]	BE[6]
PX_D5	B[3]	B[5]	BE[3]	BE[5]
PX_D4	B[2]	B[4]	BE[2]	BE[4]
PX_D3	B[1]	B[3]	BE[1]	BE[3]
PX_D2	B[0]	B[2]	BE[0]	BE[2]
PX_D1	–	B[1]	–	BE[1]
PX_D0	–	B[0]	–	BE[0]

Table 1.5: Pixel Interface Bit Mapping

1.3 Sideband Interface

1.3.1 General Information

The sideband interfaces provide a bi-directional data path subdivided into several **logical** data streams with different bandwidth in both directions:

Downstream: Data direction from Transmitter (INDT) --> to Receiver (INDR)
Upstream: Data direction to Transmitter (INDT) <-- from Receiver (INDR)

Activating the upstream sideband data transmission necessitates an additional pair of wires to establish the physical uplink (see 1.1 Link Interface). STP cables usually contain 4 pairs of wires; thus this extra connection is available in most cases. If the upstream sideband data channel is not used, it has to be disabled. The downstream sideband data channels can be partially disabled to provide extra bandwidth for the pixel data transmission.

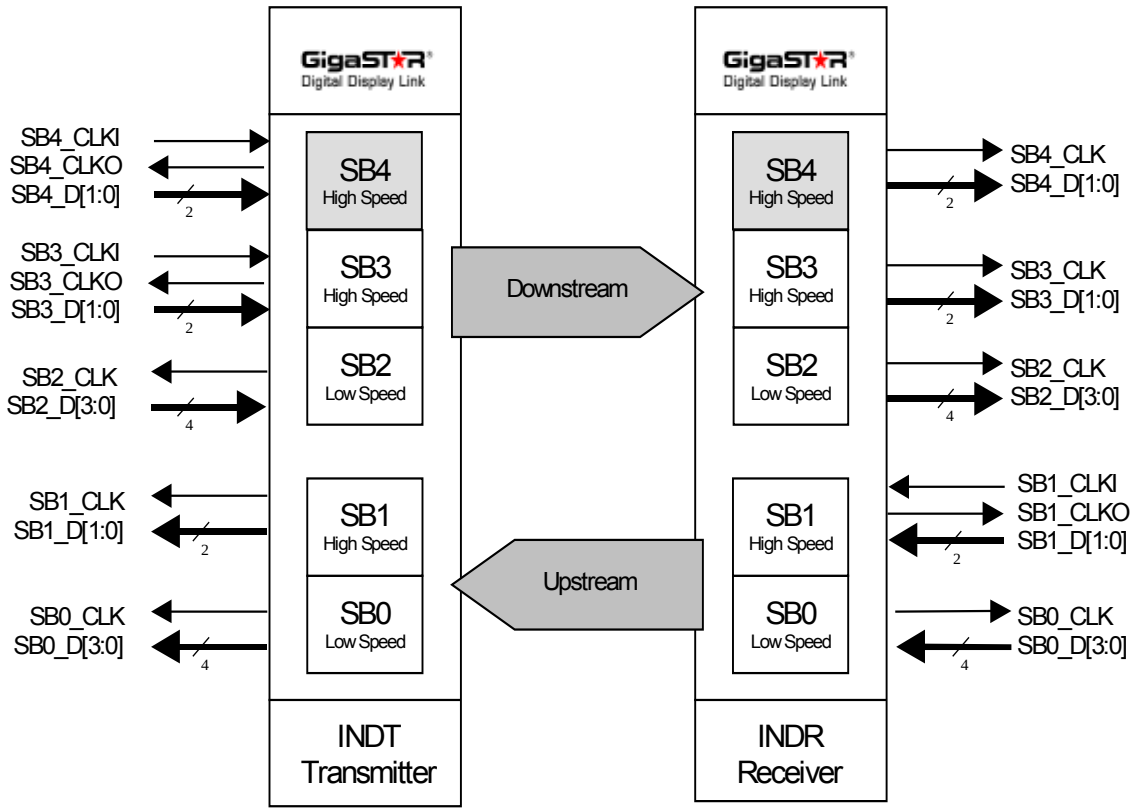


Figure 1.6: Sideband Data Interfaces

Note: SB4 available at INDT/R331B only.

Interface	Signals (D+Clk)		Speed	Direction	Width [bit]	Bandwidth [Mbps]	Asynchro-nous	Synchro-nous	Samp-ling
	INDT	INDR							
SB0	4+1	4+1	Low speed	Upstream	4	4.125	–	X	–
SB2	4+1	4+1	Low speed	Downstream	4	4.26	–	X	–
SB1	2+1	2+2	High speed	Upstream	2	111.375	X	X	–
SB3	2+2	2+1	High speed	Downstream	2	132	X	X	X
SB4[2]	2+2	2+1	High speed	Downstream	2	132	X	X	X

Table 1.6: Transfer Capabilities Sideband Data Interface Signals

1.3.2 Low-speed Upstream Sideband Data Channel (SB0)

The low-speed upstream sideband data channel consists of one 4 Mbps data channel with a 4-bit parallel interface (or 4 individual 1 Mbps data channels, each consisting of a 1-bit serial interface) and one synchronous clock output (SB0_CLK).

1.3.3 High-speed Upstream Sideband Data Channel (SB1)

The high-speed upstream sideband data channel has a 2-bit wide data interface. Different operating modes can be selected. The maximum bandwidth is 111 Mbps. This can be used for any generic data link e.g. a low-resolution graphics channel or a CMOS image sensor.

In *asynchronous* clocking mode an external clock can be applied into SB1_CLKI of the INDR. The range of the external acceptable clock frequency is 0 – 55 MHz. In *synchronous* mode data are read into the INDR using the synchronous clock frequency of 55 MHz being output at SB1_CLKO. In both cases the transferred data are available at the INDT with a fixed clock of 55 MHz.

1.3.4 Low-speed Downstream Sideband Data Channel (SB2)

The low-speed downstream sideband data channel consists of one 4 Mbps data channel with a 4-bit parallel interface (or 4 individual 1 Mbps data channels, each consisting of a 1-bit serial interface) and one synchronous clock output (SB2_CLK).

1.3.5 High-speed Downstream Sideband Data Channel (SB3, SB4[2]).

The INDT/R166B (INDT/R331B) features one (two) high-speed downstream sideband data channels, each with a 2-bit wide data interface. Different operating modes can be selected. The maximum bandwidth is 132 Mbps (2 x 132 Mbps).

In *asynchronous* clocking mode an external clock can be feed into SB3_CLKI (and SB4_CLKI[2]) of the INDT. The range of the external acceptable clock frequency is 0 – 66 MHz. In *synchronous* mode data are read into the INDT using the synchronous clock frequency of 66 MHz being output at SB3_CLKO (and SB4_CLKO[2]). In both cases the transferred data are available at the INDR with a fixed clock of 66 MHz. In *sampling* mode, the sideband data are sampled with an internal sampling clock at 66 MHz.

[2] Sideband Data Channel 4 (SB4) only available with INDT/R330B

1.3.6 Sideband Interface Signals

Sideband	Signal	Dir	Description
SB0	SB0_CLK	OUT	Sideband Data Channel 0 Upstream Synchronous Clock Output. Data is provided aligned to rising edge.
SB0	SB0_D[3:0]	OUT	Sideband Data Channel 0 Upstream Output
SB1	SB1_CLK	OUT	Sideband Data Channel 1 Upstream Synchronous Clock Output. Data is provided aligned to rising edge.
SB1	SB1_D[1:0]	OUT	Sideband Data Channel 1 Upstream Output
SB2	SB2_CLK	OUT	Sideband Data Channel 2 Downstream Synchronous Clock Output. Data is registered at rising edge.
SB2	SB2_D[3:0]	IN	Sideband Data Channel 2 Downstream Input
SB3	SB3_CLKI	IN	Sideband Data Channel 3 Downstream Asynchronous Clock Input. Data is registered at rising edge.
SB3	SB3_CLKO	OUT	Sideband Data Channel 3 Downstream Synchronous Clock Output. Data is registered at rising edge.
SB3	SB3_D[1:0]	IN	Sideband Data Channel 3 Downstream Input
SB4[3]	SB4_CLKI	IN	Sideband Data Channel 4 Downstream Asynchronous Clock Input. Data is registered at rising edge.
SB4[3]	SB4_CLKO	OUT	Sideband Data Channel 4 Downstream Synchronous Clock Output. Data is registered at rising edge.
SB4[3]	SB4_D[1:0]	IN	Sideband Data Channel 4 Downstream Input.

Table 1.7: Sideband Interface Signals (INDT, Transmitter)

Sideband	Signal	Dir	Description
SB0	SB0_CLK	OUT	Sideband Data Channel 0 Upstream Synchronous Clock Output. Data is registered at rising edge.
SB0	SB0_D[3:0]	IN	Sideband Data Channel 0 Upstream Input
SB1	SB1_CLKI	IN	Sideband Data Channel 1 Upstream Asynchronous Clock Input. Data is registered at rising edge.
SB1	SB1_CLKO	OUT	Sideband Data Channel 1 Upstream Synchronous Clock Output. Data is registered at rising edge.
SB1	SB1_D[1:0]	IN	Sideband Data Channel 1 Upstream Input
SB2	SB2_CLK	OUT	Sideband Data Channel 2 Downstream Synchronous Clock Output. Data is provided aligned to rising edge.
SB2	SB2_D[3:0]	OUT	Sideband Data Channel 2 Downstream Output
SB3	SB3_CLK	OUT	Sideband Data Channel 3 Downstream Synchronous Clock Output. Data is provided aligned to rising edge.
SB3	SB3_D[1:0]	OUT	Sideband Data Channel 3 Downstream Output
SB4[3]	SB4_CLK	OUT	Sideband Data Channel 4 Downstream Synchronous Clock Output. Data is provided aligned to rising edge.
SB4[3]	SB4_D[1:0]	OUT	Sideband Data Channel 4 Downstream Output.

Table 1.8: Sideband Interface Signals (INDR, Receiver)

[3] Sideband Data Channel 4 (SB4) only available with INDT/R330B

1.4 Audio Interface

The audio interface provides four serial audio channels, which are compliant to the Standard *IEC958 Digital audio interface* from the EBU (European Broadcasting Union), also known as *S/P-DIF Interface*. It supports sampling frequencies of 44,1 kHz and 48,0 kHz. The audio data interface can be disabled to free up bandwidth for pixel data transmission.

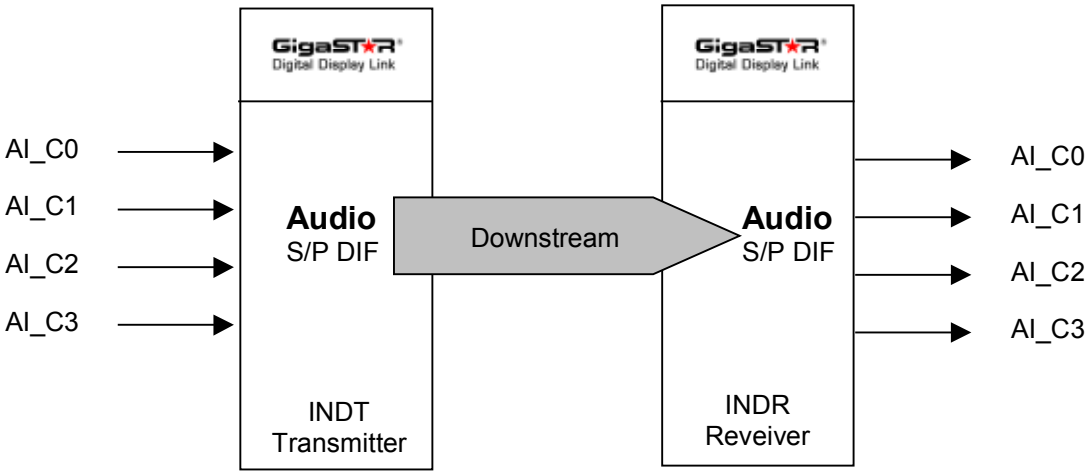


Figure 1.7: Audio Interface

Signal	Tx	Rx	Description
AI_C0	IN	OUT	S/P-DIF Audio Channel 0
AI_C1	IN	OUT	S/P-DIF Audio Channel 1
AI_C2	IN	OUT	S/P-DIF Audio Channel 2
AI_C3	IN	OUT	S/P-DIF Audio Channel 3

Table 1.9: Audio Interface Signals

2 Device Configuration

The GigaSTaR® Digital Display Link allows for configuring the pixel-, sideband- and audio-interface.

2.1 Pixel Clock Conditioning (Rx only)

In order to allow for interfacing with devices being susceptible to any clock variations the Rx device provides the capability to compensate for that.
PX_CLK_OUT holds the pixel clock signal as it has been created from the embedded clock in the data stream. Those signals are typically afflicted with jitter, which may cause invalid data on interfacing devices dependent on its PLL performance. By feeding back the PX_CLK_OUT via an external PLL into the PX_CLK_IN, the PX_CLK signal can be de-jittered. As soon the PX_CLK_IN receives a valid frequency of 20MHz or higher the pixel data outputs are enabled and the PX_CLK provides the valid and jitter-free pixel clock accordingly.

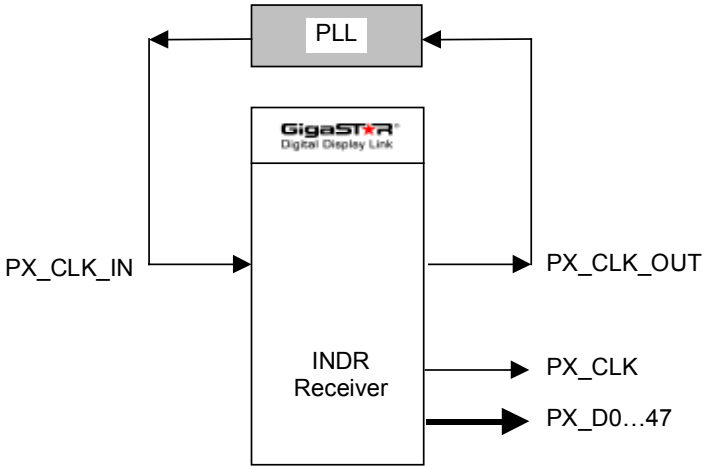


Figure 2.1: Pixel Clock conditioning

When PX_CLK_IN is tied to logic HIGH the pixel data outputs PX_D0…D47 are tri-stated.
When PX_CLK_IN is tied to logic LOW the Rx166/Rx331 operates as Rx165/Rx330, with the restriction that the PX_CLK- (signal provided by Rx165/Rx330) is not available. In this case the PX_CLK holds the pixel clock signal as it has been created from the embedded clock in the data stream. Though the 166/331series can be used in applications designed for 165/330-series, other combinations than pairs (Tx and Rx) of the same series are not compatible.

Note: The external PLL shall have an integrating characteristic to prepare the PX_CLK signal for proper and stable interfacing with devices (DVI/LVDS) whose internal PLL performance may cause data loss especially at higher frequencies and resolutions.

2.2 Configuration Vectors and Configuration Data

Four configuration vectors (cfg0 – cfg3, 4-bit each) must be loaded into the device through the low-speed sideband data interfaces SB0 and SB2. The Tx and the Rx device must be connected via the downlink.

SB0 and SB2 sideband data are multiplexed and are also used for device configuration. After de-assertion of RESET#, CFG_CYC is automatically being driven high and enables the configuration process.

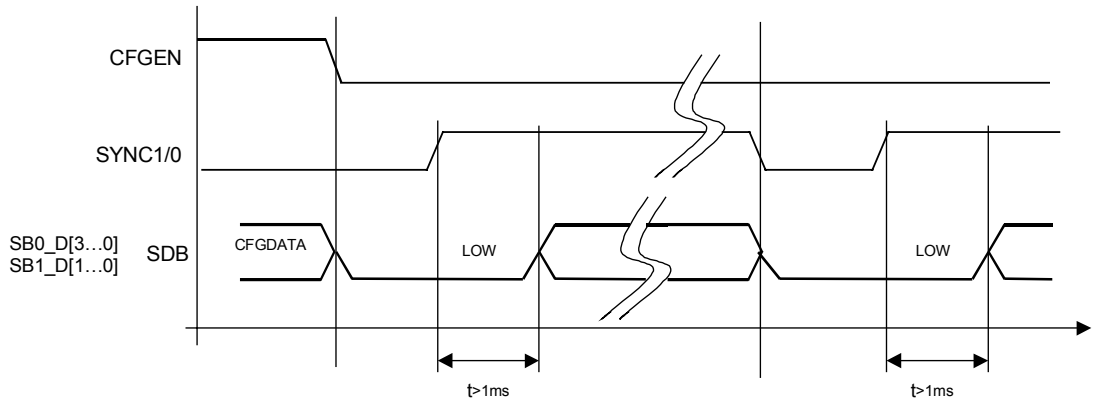
The configuration select signals (CFG_SEL[3:0]) are provided sequentially at SB0 (INDT) respectively at SB2 (INDR). These select signals enable e.g. an external logic which provides the configuration vectors (cfg0 – cfg3) via the configuration signals CFG_D[3:0]. These are read at SB2 (INDT) respectively at SB0 (INDR).

Sequence	Vector name	Configuration Select Signals CFG_SEL[3:0]	Configuration vector
1	**cfg0**	0001	Requests configuration vector 0
2	**cfg1**	0010	Requests configuration vector 1
3	**cfg2**	0100	Requests configuration vector 2
4	**cfg3**	1000	Requests configuration vector 3

Table 2.1: Configuration Vector Sequence

	Transmitter		Receiver	
Configuration mode (CFG_CYC = 1)	CFG_SEL[3:0]	CFG_D[3:0]	CFG_SEL[3:0]	CFG_D[3:0]
Normal mode (CFG_CYC = 0)	SB0_D[3:0]	SB2_D[3:0]	SB2_D[3:0]	SB0_D[3:0]

Table 2.2: Pin Naming Multiplex Matrix



For proper initialization of the upstream channel, the side band data input at the Rx needs to be kept low for >1ms after the SYNC1/0 went high.

Figure 2.2 shows how to perform the configuration with external logic.

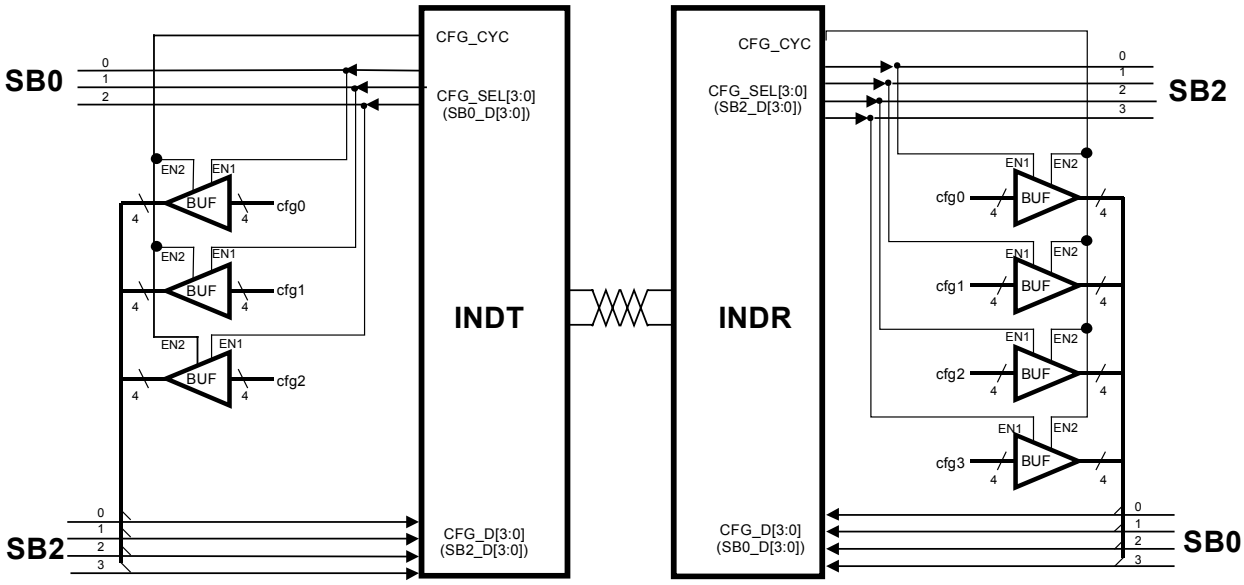


Figure 2.2: Configuration Logic

Each configuration vector's default setting is "**1111**". This popular operating mode (see light gray lines on following tables) can easily be established with pull-up resistors from the configuration inputs to V_{CC} instead of tri-state buffers. All configuration vectors are valid for transmitter and receiver, unless otherwise noted.

2.3 Configuration Process and Timing

Figure 2.3 shows the configuration process.

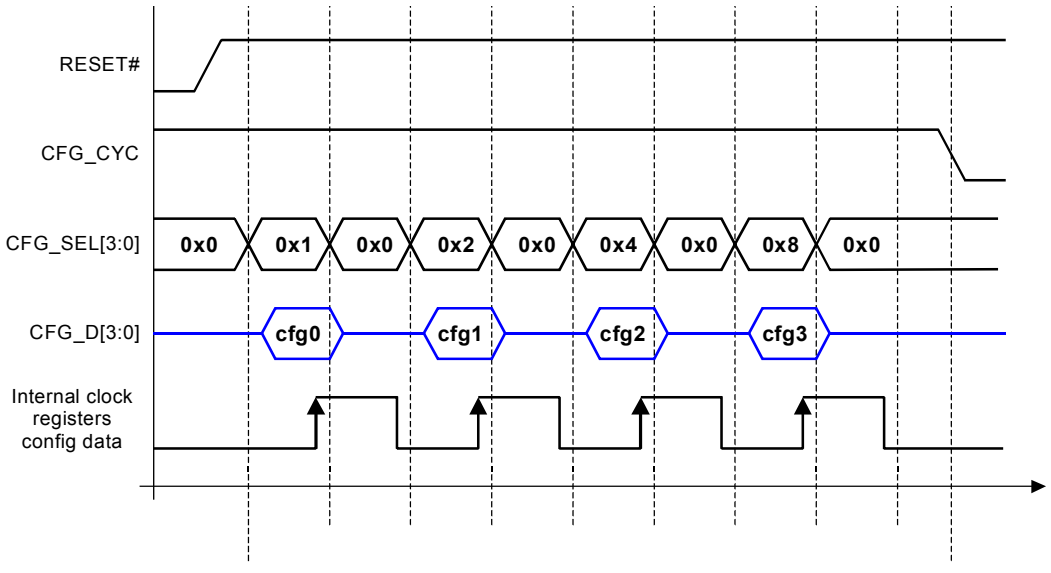


Figure 2.3: Timing of Configuration Process

2.4 Interface Configuration Scheme

Note: The low-speed downstream sideband is automatically enabled, when high-speed downstream sideband OR audio is enabled. INDT and INDR must be configured within the same group.

Interface	Vector Name	Vector Bits	Pixel Interface	Description	Group
Pixel Interface	cfg0	1111	24-bit	24 bits of pixel(n) sampled at rising edge of PX_CLK+	V1
		0100	24-bit	24 bits of pixel(n) sampled at falling edge of PX_CLK+	
		0101	24-bit	24 bits of pixel(n) sampled at both edges of PX_CLK+	
		1001	48-bit	24 bits of pixel(n) and 24 bits of pixel(n+1) sampled at rising edge of PX_CLK+	
		1010	48-bit	24 bits of pixel(n) and 24 bits of pixel(n+1) sampled at falling edge of PX_CLK+	
		0000	18-bit	18 bits of pixel(n) sampled at rising edge of PX_CLK+	V2
		0001	18-bit	18 bits of pixel(n) sampled at falling edge of PX_CLK+	
		0010	18-bit	18 bits of pixel(n) sampled at both edges of PX_CLK+	
		0110	36-bit	18 bits of pixel(n) and 18 bits of pixel(n+1) sampled at rising edge of PX_CLK+	
		0111	36-bit	18 bits of pixel(n) and 18 bits of pixel(n+1) sampled at falling edge of PX_CLK+	
Sideband Interface Tx	cfg1	0000		Disable high-speed downstream sideband data channel SB3 and SB4[4]	S1
		11XX		Enable high-speed downstream sideband data channel SB3 and SB4[4]	S2
		1100		Clocking: Asynchronous mode at downstream sideband data channels SB3 and SB4[4]	
		1111		Clocking: Synchronous mode at downstream sideband data channels SB3 and SB4[4]	
		1110	Tx only	Clocking: Sampling mode at downstream sideband data channels SB3 and SB4[4]	
Audio + High Speed Upstream SB1	cfg2	X100		Disable upstream sideband data	A
		X111		Enable upstream sideband data	
		01XX		Disable Audio	
		11XX		Enable Audio	
Pre-Emphasis For Serial Upstream Trans-mission	cfg3	0000	Rx only	Inom = x1.0, Ipre = x1.3, algorithm 1	
		0001		Inom = x1.0, Ipre = x1.3, algorithm 2	
		0010		Inom = x1.0, Ipre = x1.6, algorithm 1	
		0011		Inom = x1.0, Ipre = x1.6, algorithm 2	
		0100		Inom = x1.0, Ipre = x1.9, algorithm 1	
		0101		Inom = x1.0, Ipre = x1.9, algorithm 2	
		0110		Inom = x1.3, Ipre = x1.6, algorithm 1	
		0111		Inom = x1.3, Ipre = x1.6, algorithm 2	
		1000		Inom = x1.3, Ipre = x1.9, algorithm 1	
		1001		Inom = x1.3, Ipre = x1.9, algorithm 2	
		1010		Inom = x1.6, Ipre = x1.9, algorithm 1	
		1011		Inom = x1.6, Ipre = x1.9, algorithm 2	
		1100		Inom = Ipre = x1.9	
		1101		Inom = Ipre = x1.3	
		1110		Inom = Ipre = x1.0	
		1111		Inom = Ipre = x1.6	
Note: others than the above mentioned vector bit combinations are not allowed					

Table 2.3: Configuration of the Pixel Interface Mode

2.5 Error Handling and Reset

The chips provide an error detection signal (ERROR pin) indicating incorrect video timings. It is recommended to reset the chip after the ERROR pin went high.

[4] Sideband Data Channel 4 (SB4) only available with INDT/R330B

3 Electrical Specification

3.1 External Circuits

3.1.1 External Loop Filter Specification

The internal PLLs of the INDT166B/331B and the INDR166B/331B devices require an external RC loop filter (**Figure 3.1**).

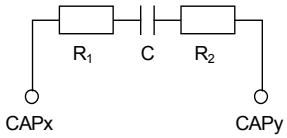


Figure 3.1: External Loop Filter Circuit

It is recommended to implement the 0-Ohm resistors R_1 and R_2 for the transmitter as real components, because their values may change in future versions. **Table 3.1** shows the optimal values for the INDT/R166B, **Table 3.2** for the INDT/R331B. It is recommended to use SMD ceramic chip capacitors and chip resistors.

Link	Signals	Pins	Parameter	Symbol	Value Tx (INDT166B)	Value Rx (INDR166B)
PLL0	CAP1 CAP2	C11 C12	Loop Filter Capacitor	C	1µF	1µF
			Loop Filter Resistor 1	R_1	0 Ω	47 Ω
			Loop Filter Resistor 2	R_2	0 Ω	47 Ω

Table 3.1: External Loop Filter Specification for INDT/R166B

Link	Signals	Pins	Parameter	Symbol	Value Tx (INDT331B)	Value Rx (INDR331B)
PLL0	CAP1 CAP2	A15 B15	Loop Filter Capacitor	C	1µF	1µF
			Loop Filter Resistor 1	R_1	0 Ω	47 Ω
			Loop Filter Resistor 2	R_2	0 Ω	47 Ω
PLL1	CAP3 CAP4	A8 B8	Loop Filter Capacitor	C	1µF	1µF
			Loop Filter Resistor 1	R_1	0 Ω	47 Ω
			Loop Filter Resistor 2	R_2	0 Ω	47 Ω

Table 3.2: External Loop Filter Specification for INDT/R331B

3.1.2 Serial Transmission Cable Interconnect

The serial lines have to be AC-coupled through 100 nF capacitors; RF ceramic capacitors shall be used. Values for R and L are dependent on the type of cable.

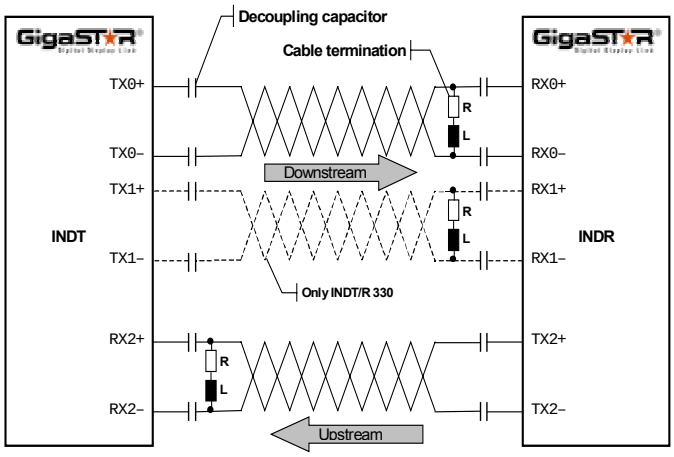


Figure 3.2: Decoupling and Cable Termination

3.1.3 Serial Transmission Cable Termination

Besides the AC coupling capacitors, a dedicated cable termination has to be provided on the receiver input (**Figure 3.2**). The termination values have to be matched for the type of cable and length.

3.1.4 Receiver Equalizer

The equalizer inside the receiver device compensates the frequency-dependant cable attenuation. For cable lengths[5] above 10m, it is recommended to activate the equalizer function (pin EQ = HIGH) to achieve optimum transmission performance.

3.1.5 Reference Clock

The internal data clock frequency is 1320 MHz and is generated by internal PLLs. Both, transmitter and receiver require an external clock oscillator or reference clock of 66.0 MHz with a stability of ± 100 ppm. To enable the INDT/R166 supporting VESA Standard XGA24, the clock frequency must be 66.6667 MHz. However, the use of 66.6667 MHz clock frequency disables the transmission of audio data of 44.1 kHz sampling frequency. Transmission of audio data of 48 kHz sampling frequency is still possible as long as there is sufficient bandwidth left.

3.1.6 V_{REF} Reference Circuitry

The V_{REF}-pin at the transmitter device has two modes to set the threshold level at the input pixel interface. For standard 3.3 V LVTTL input level, it must be tied to V_{CC} (3.3 V). For low swing voltage levels (V_{DD} = 1.0 – 2.0 V), V_{REF} must be tied to half the supply voltage (V_{DD}/2 = 0.5 – 1.0 V) of the driver (graphics controller). **Figure 3.3** shows the input thresholds at different V_{REF} levels:

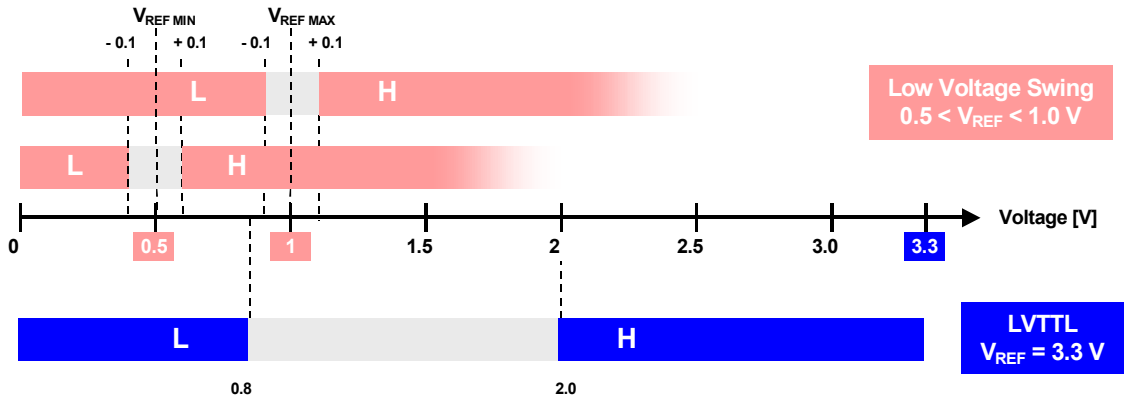


Figure 3.3: V_{REF} Reference Circuitry

3.2 Power Supply

Each GigaSTaR® Digital Display Link chip consists of a separate Bipolar and CMOS die. Therefore, the device provides multiple power planes to minimize EMI. It is suggested to use an own 3.3 V regulator[6] for the whole chip to implement optimal decoupling of the power supply lines. **Table 3.3** shows the current consumption of the devices.

Device	Die	Typical[7] Current Consumption [mA]
INDT/R166B	CMOS	400
	Bipolar	230
INDT/R331B	CMOS	400
	Bipolar	540

Table 3.3: Current Consumption

[5] Refers to the GORE reference cable GGSC1608-X, other cable types may differ.
[6] Do not use two separate regulators to avoid chip damage due to latch-up.
[7] Depending on video operating modes and external circuitry

Table 3.4 shows, which planes can be tied together.

Pin Name	Type	Description	VCC Plane No.	GND Plane No.
VCC_CORE	POWER	CMOS core supply	**1A**	**1B**
GND_CORE	GROUND			
VCC_IO	POWER	CMOS digital I/O supply	**1A**	**1B**
GND_IO	GROUND			
VCC_CML	POWER	CMOS chip-to-chip interface supply	**2A**	**2B**
GND_CML	GROUND			
VCC_SX	POWER	CMOS uplink I/O supply	**4A (1A)**[8]	**4B (1B)**
GND_SX	GROUND			
VCC_IA	POWER	Bipolar Chip-to-chip interface supply	**2A**	**2B**
GND_IA	GROUND			
VCC_A0	POWER	Bipolar downlink I/O supply	**3A**	**3B**
GND_A0	GROUND			
VCC_A1	POWER	Bipolar PLL supply	**3A**	**3B**
GND_A1	GROUND			

Table 3.4: Power Supply Planes

3.3 Absolute Maximum Ratings

The absolute maximum ratings define values beyond which damage may occur to the device. Inova Semiconductors may not be held liable for any product degradation or damage caused by a violation of the absolute maximum ratings. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Functional operation of the device at these or any other conditions above those indicated in the recommended operating conditions is not guaranteed.

Parameter	Symbol	Min.	Max.	Units	Note
DC Supply Voltage	V_{CC}	-0.5	+4.2	V	See keynote (6)
Input Voltage	V_{IN}	-0.5	V_{CC}+0.5	V	
I/O Current (DC or transient any pin)	I_D	-20	+20	mA	See keynote (6)
Junction Temperature (under bias)	T_j	-45	+140	° C	
Storage Temperature	T_{stg}	-55	+150	° C	
Soldering Temp./Time	T_{SLD} / t_{SLD}		220 / 10	° C / sec	
Static Discharge Voltage	V_{ESD1}		± 2000	V	Human Body Model

Table 3.5: Absolute Maximum Ratings

3.4 Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units	Note
DC Supply Voltage	V_{CC}	+3.15	+3.45	V	$V_{cc\ typ.}$ = 3.3 V
Input Voltage	V_{IN}	0	Vcc	V	V_{CC} =3.3V ± 0.15V
CML Output Current	I_{OUTCML}	-10	+10	mA	
CMOS Output Current	$I_{OUTCMOS}$	-10	+10	mA	
Junction Temperature (under bias)	T_j	0	+125	° C	
Ambient Temperature	T_a	-40	+85	° C	

Table 3.6: Recommended Operating Conditions

[8] Plane #4 may be connected to plane #1, if this plane is adequately noise-free.

3.5 AC–Characteristics (under recommended operating conditions, Reference Clock Freq. = 66 MHz)

Parameter	Min.	Typ.	Max.	Units
Input capacitance, any pin (@ 66 MHz)		1.5	3	pF
Serial Transmission Data Rate (Downstream, per Link)		1.32		Gbit/s
Serial Bit Width (Downstream)		757.6		ps
CMOS Output Rise / Fall Time (C_L = 10 pF)		5	10	ns

Table 3.7: AC–Characteristics

3.6 DC–Characteristics (under recommended operating conditions)

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
CMOS Input High Voltage	V_{IH}		2.6			V
CMOS Input Low Voltage	V_{IL}				0.7	V
CMOS Input High Current	I_{IH}	V_{IN} = Vcc	-1		1	µA
CMOS Input Low Current	I_{IL}	V_{IN} = 0 V	-1		1	µA
EQLSEL/OSC Pin High Current	I_{IH}	V_{IN} = Vcc	-10		40	µA
EQLSEL/OSC Pin Low Current	I_{IL}	V_{IN} = 0 V	-10		10	µA
CMOS Output High Voltage	V_{OH}	I_{OH} = -0.5 mA	0,95Vcc			V
CMOS Output Low Voltage	V_{OL}	I_{OL} = 1.5 mA			0,05 Vcc	V
CMOS Output High Current	I_{OH}	V_{OH} = 0.9Vcc	-3	-5		mA
CMOS Output Low Current	I_{OL}	V_{OL} = 0.1Vcc	3.5	6		mA
LOCK Output High Current	I_{LH}	V_{OH} = 0.9Vcc	-1	-2.5		mA
LOCK Output Low Current	I_{LL}	V_{OL} = 0.1Vcc	1.5	3		mA
INDT166B Supply Current	$I_{CCTX166}$	CMOS output load = 10 pF @ $V_{cc\ typ.}$ = 3.3 V	-	635	675	mA
INDR166B Supply Current	$I_{CCRX166}$	CMOS output load = 10 pF @ $V_{cc\ typ.}$ = 3.3 V	-	620	665	mA
INDT331B Supply Current	$I_{CCTX331}$	CMOS output load = 10 pF @ $V_{cc\ typ.}$ = 3.3 V	-	955	985	mA
INDR331B Supply Current	$I_{CCRX331}$	CMOS output load = 10 pF @ $V_{cc\ typ.}$ = 3.3 V	-	935	975	mA

Table 3.8: DC–Characteristics

Note: Floating CMOS inputs can result in excessive supply current. Therefore unused inputs should be tied to Vcc or Gnd.

3.7 Reference Clock Specification (Ta = -40 to 85° C; Vcc = 3.15 to 3.45 V)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Nominal Frequency (INDT/R166)	f_{OSC}		66.0		MHz	66,6667 MHz possible, see 3.1.5
Nominal Frequency (INDT/R331)	f_{OSC}		66.0		MHz	
Frequency Tolerance	F_{TOL}	-100		+100	ppm	
Duty Cycle		40		60	%	

Table 3.9: Reference Clock Specification

3.8 Timing Specification

(a) Transmitter pixel interface

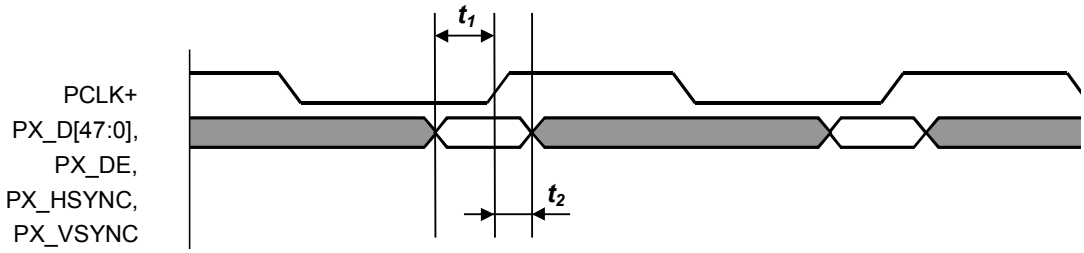


Figure 3.4: Pixel Interface Timing Diagram At Rising Edge At Tx

Parameter	Description	Min.	Typ.	Max.	Unit
t_1	Pixel data and ctrl signal setup time to pixel clock at Tx	0.5	0.9	-	ns
t_2	Pixel data and ctrl signal hold time to pixel clock at Tx	1.0	1.3	-	ns

Table 3.10: Pixel Interface Timing Table At Rising Edge At Tx

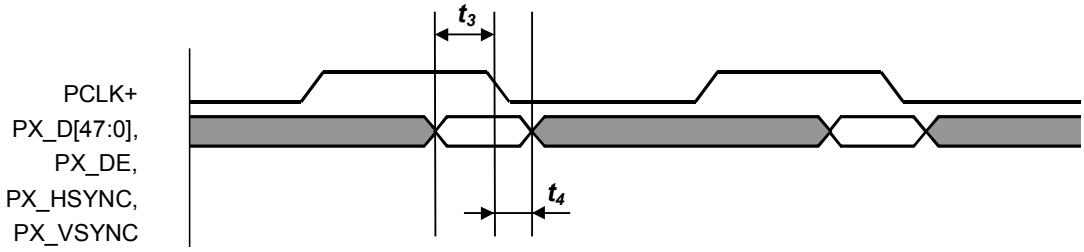


Figure 3.5: Pixel Interface Timing Diagram At One Pixel Per Clock At Falling Edge At Tx

Parameter	Description	Min.	Typ.	Max.	Unit
t_3	Pixel data and ctrl signal setup time to pixel clock at Tx	0.5	0.9	-	ns
t_4	Pixel data and ctrl signal hold time to pixel clock at Tx	0.5	1.3	-	ns

Table 3.11: Pixel Interface Timing Table At One Pixel Per Clock At Falling Edge At Tx

(b) Receiver pixel interface

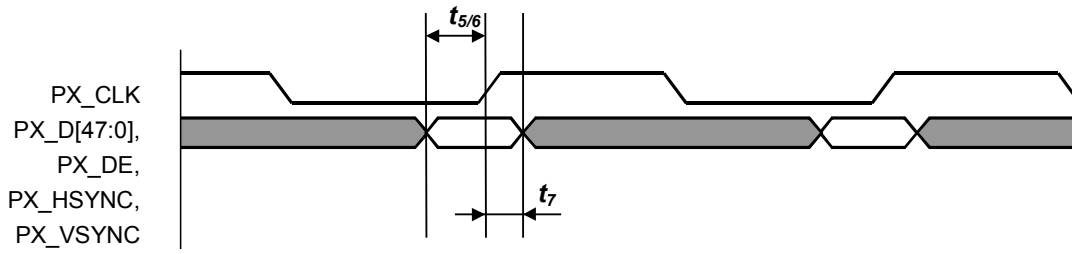


Figure 3.6: Pixel Interface Timing Diagram At Rising Edge At Rx

Parameter	Description	Min.	Typ.	Max.	Unit
t_5	Pixel data and ctrl signal setup time to pixel clock at Rx (SXGA)	1.8	4.0	4.4	ns
t_6	Pixel data and ctrl signal setup time to pixel clock at Rx (UXGA)	1.6	3.0	4.2	ns
t_7	Pixel data and ctrl signal hold time to pixel clock at Rx	0.5	1.2	1.4	ns

Table 3.12: Pixel Interface Timing Table At Rising Edge At Rx

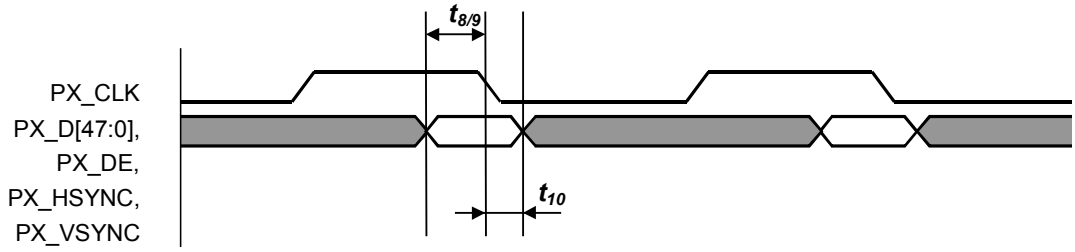


Figure 3.7: Pixel Interface Timing Diagram At Falling Edge At Rx

Parameter	Description	Min.	Typ.	Max.	Unit
t_8	Pixel data and ctrl signal setup time to pixel clock at Rx (SXGA)	2.2	3.8	4.7	ns
t_9	Pixel data and ctrl signal setup time to pixel clock at Rx (UXGA)	1.0	2.9	3.7	ns
t_{10}	Pixel data and ctrl signal hold time to pixel clock at Rx	0.5	1.2	1.3	ns

Table 3.13: Pixel Interface Timing Table At Falling Edge At Rx

(c) Transmitter sideband interface

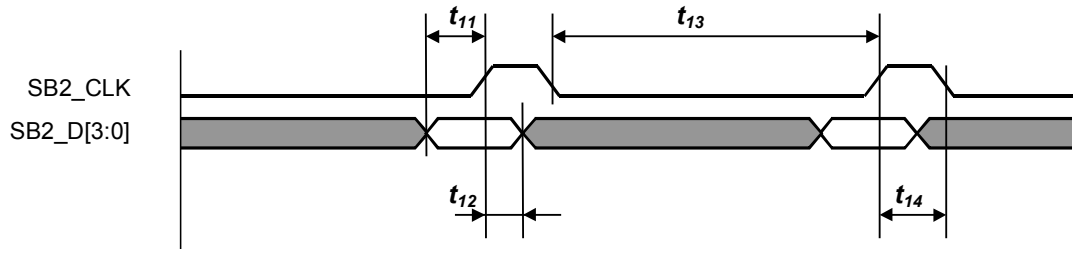


Figure 3.8: Tx Sideband Data Interface; Low Speed Downstream

Parameter	Description	Min.	Typ.	Max.	Unit
t_{11}	Low speed downstream sideband data setup time to clock output at Tx	40	200	-	ns
t_{12}	Low speed downstream sideband data hold time to clock output at Tx	0	100	-	ns
t_{13}	Low speed downstream sideband data clock high time at Tx	29,3	30	31,7	ns
t_{14}	Low speed downstream sideband data clock low time at Tx	900	909	916	ns

Table 3.14: Tx Sideband Data Interface; Low Speed Downstream

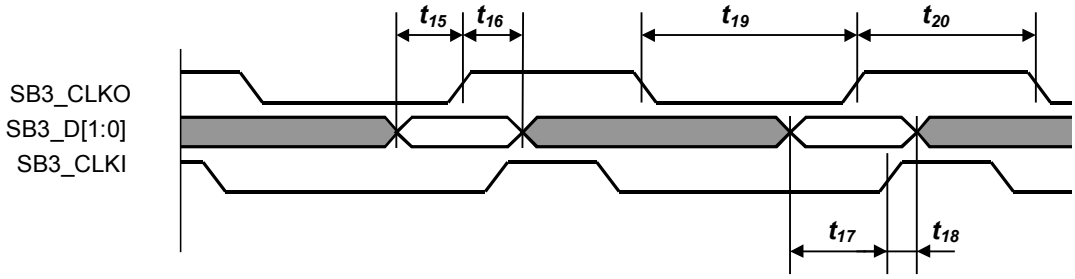


Figure 3.9: Tx Sideband Data Interface; High Speed Downstream

Parameter	Description	Min.	Typ.	Max.	Unit
t_{15}	High speed downstream sideband data setup time to clock output (synchronous mode) at Tx	6	8.6	-	ns
t_{16}	High speed downstream sideband data hold time to clock output (synchronous mode) at Tx	0	2.0	-	ns
t_{17}	High speed downstream sideband data setup time to clock input (asynchronous mode) at Tx	2	6.0	-	ns
t_{18}	High speed downstream sideband data hold time to clock input (asynchronous mode) at Tx	2	1.0	-	ns
t_{19}	High speed downstream sideband data clock output high time at Tx	6,1	6.3	6,5	ns
t_{20}	High speed downstream sideband data clock output low time	8,6	9.5	10,1	ns

Table 3.15: Tx Sideband Data Interface; High Speed Downstream

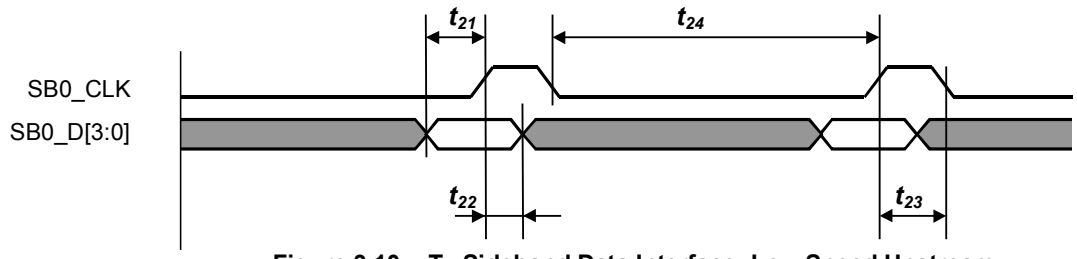


Figure 3.10: Tx Sideband Data Interface; Low Speed Upstream

Parameter	Description	Min.	Typ.	Max.	Unit
t_{21}	Low speed upstream sideband data setup time to clock output at Tx	420	430	440	ns
t_{22}	Low speed upstream sideband data hold time to clock output at Tx	520	530	540	ns
t_{23}	Low speed upstream sideband data clock high time at Tx	532	534	536	ns
t_{24}	Low speed upstream sideband data clock low time at Tx	430	435	442	ns

Table 3.16: Tx Sideband Data Interface; Low Speed Upstream

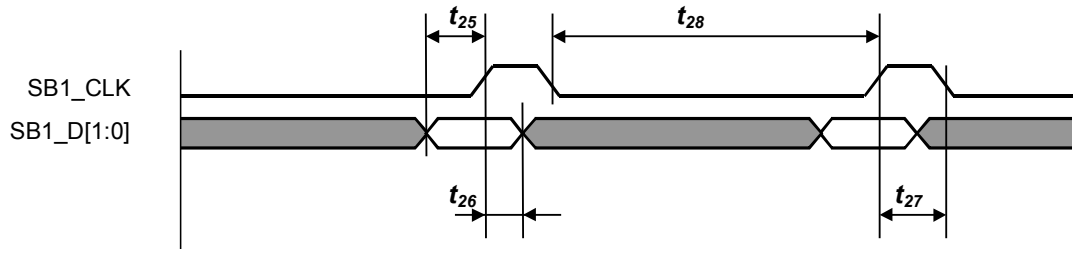


Figure 3.11: Tx Sideband Data Interface; High Speed Upstream

Parameter	Description	Min.	Typ.	Max.	Unit
t_{25}	High speed upstream sideband data setup time to clock output at Tx	9,4	10,2	11,5	ns
t_{26}	High speed upstream sideband data hold time to clock output at Tx	4,4	5.5	6,0	ns
t_{27}	High speed upstream sideband data clock high time at Tx	9,6	10.5	11,5	ns
t_{28}	High speed upstream sideband data clock low time at Tx	3,8	9.7	10,2	ns

Table 3.17: Tx Sideband Data Interface; High Speed Upstream

(d) Receiver sideband interface

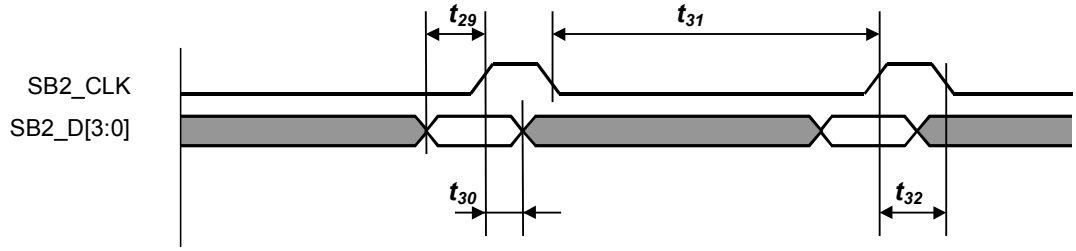


Figure 3.12: Rx Sideband Data Interface; Low Speed Downstream

Parameter	Description	Min.	Typ.	Max.	Unit
t_{29}	Low speed downstream sideband data setup time to clock output at Rx	478	484	490	ns
t_{30}	Low speed downstream sideband data hold time to clock output at Rx	450	455	460	ns
t_{31}	Low speed downstream sideband data clock high time at Rx	450	454	458	ns
t_{32}	Low speed downstream sideband data clock low time at Rx	480	484	490	ns

Table 3.18: Rx Sideband Data Interface; Low Speed Downstream

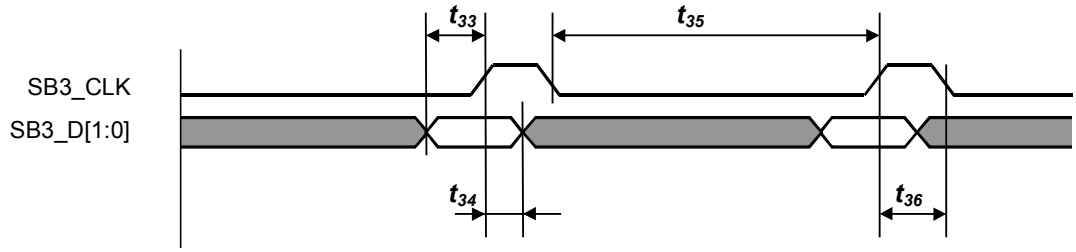


Figure 3.13: Rx Sideband Data Interface; High Speed Downstream

Parameter	Description	Min.	Typ.	Max.	Unit
t_{33}	High speed downstream sideband data setup time to clock output at Rx	5,5	6.0	6,4	ns
t_{34}	High speed downstream sideband data hold time to clock output at Rx	7,2	7,5	8,4	ns
t_{35}	High speed downstream sideband data clock high time at Rx	9,8	10.6	11,1	ns
t_{36}	High speed downstream sideband data clock low time at Rx	5,5	6.4	6,8	ns

Table 3.19: Rx Sideband Data Interface; High Speed Downstream

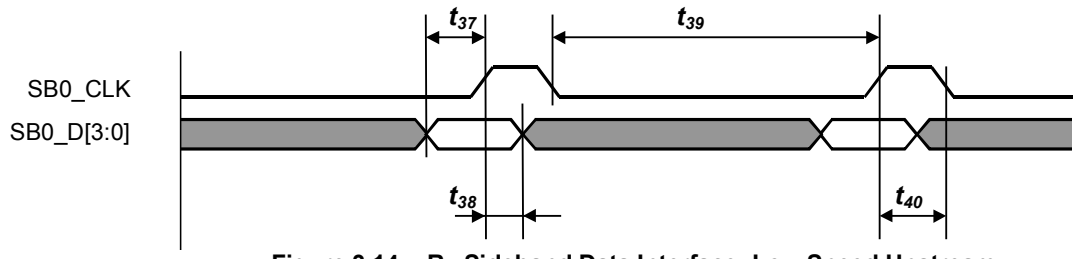


Figure 3.14: Rx Sideband Data Interface; Low Speed Upstream

Parameter	Description	Min.	Typ.	Max.	Unit
t_{37}	Low speed upstream sideband data setup time to clock output at Rx	20	100	-	ns
t_{38}	Low speed upstream sideband data hold time to clock output at Rx	0	10	-	ns
t_{39}	Low speed upstream sideband data clock high time at Rx	47,9	48,8	49,7	ns
t_{40}	Low speed upstream sideband data clock low time at Rx	912	922	932	ns

Table 3.20: Rx Sideband Data Interface; Low Speed Upstream

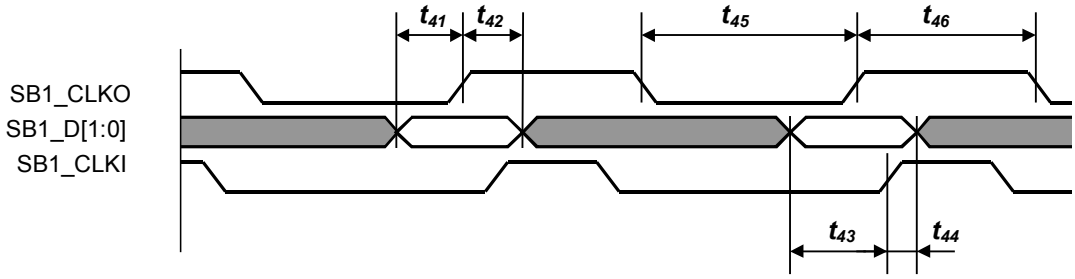


Figure 3.15: Rx Sideband Data Interface; High Speed Upstream

Parameter	Description	Min.	Typ.	Max.	Unit
t_{41}	High speed upstream sideband data setup time to clock output (synchronous mode) at Rx	4,0	6,0	-	ns
t_{42}	High speed upstream sideband data hold time to clock output (synchronous mode) at Rx	0	1,0	-	ns
t_{43}	High speed upstream sideband data setup time to clock output (asynchronous mode) at Rx	0	2,5		ns
t_{44}	High speed upstream sideband data hold time to clock output (asynchronous mode) at Rx	1,0	2,5		ns
t_{45}	High speed upstream sideband data clock high time at Rx	7,2	10,1	11,3	ns
t_{46}	High speed upstream sideband data clock low time at Rx	9,7	10,1	10,6	ns

Table 3.21: Rx Sideband Data Interface; High Speed Upstream

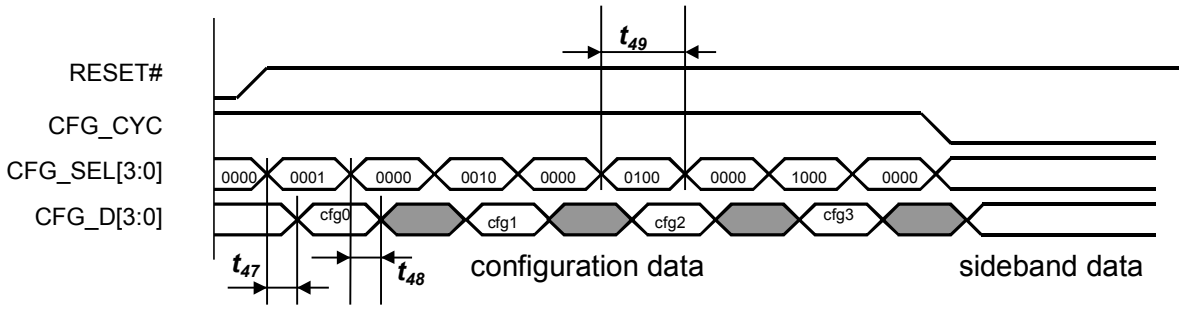


Figure 3.16: Configuration Interface Timing

Parameter	Description	Min.	Typ.	Max.	Unit
t_{47}	Configuration Select High Phase	-	350	-	ns
t_{48}	Configuration Select High to Configuration Data valid	-	100	-	ns
t_{49}	Configuration data valid after Configuration Select high to low transition	-	0	-	ns

Table 3.22: Configuration Interface Timing

4 Signals

4.1 INDT166B Transmitter Signal Description

Pin Name	Pin	Dir	Type	Description
Link Interface				
TX0+	B8	OUT	CML	Serial Data Output (Downlink)
TX0–	B9	OUT	CML	
RX2+	A5	IN	CML	Serial Data Input (Uplink)
RX2–	A4	IN	CML	
LOCK0	B6	OUT	LVTTL	Lock Indicator. HIGH when PLL of Downlink is properly locked
SYNC2	B2	OUT	LVTTL	HIGH when the Uplink is frame synchronous
Pixel Interface				
PX_CLK+	K14	IN	LVTTL*	Pixel clock 24 – 161 MHz, diff + or single-ended
PX_CLK–	J14	IN	LVTTL*	Pixel clock 24 – 161 MHz, diff – pull to GND in single ended mode
PX_D[47:0]	(see Table 4.3)	IN	LVTTL*	Configurable parallel pixel data interface
PX_HSYNC	J13	IN	LVTTL*	Pixel data framing – Horizontal sync pulse (active HIGH)
PX_VSYNC	H13	IN	LVTTL*	Pixel data framing – Vertical sync pulse (active HIGH)
PX_DE	H14	IN	LVTTL*	Pixel data framing – Data enable (active HIGH)
VREF	G13	IN	A	Configures the input level of the pixel interface
Sideband Interface				
SB0_CLK	A13	OUT	LVTTL	Sideband Data Channel 0 Upstream Synchronous Clock Output. Data is provided aligned to rising edge.
SB0_D[3:0] (CFG_SEL[3:0])	A11,B11,A12,B12	OUT	LVTTL	If CFG_CYC=0: Sideband Data Channel 0 Upstream Output If CFG_CYC=1: Configuration vector output
SB1_CLK	E14	OUT	LVTTL	Sideband Data Channel 1 Upstream Synchronous Clock Output. Data is provided aligned to rising edge.
SB1_D[1:0]	D14,D13	OUT	LVTTL	Sideband Data Channel 1 Upstream Output
SB2_CLK	C13	OUT	LVTTL	Sideband Data Channel 2 Downstream Synchronous Clock Output. Data is registered at rising edge.
SB2_D[3:0] (CFG_D[3:0])	A14,B14,B13,C14	IN	LVTTL	If CFG_CYC=0: Sideband Data Channel 2 Downstream Input If CFG_CYC=1: Configuration data input
SB3_CLKI	G14	IN	LVTTL	Sideband Data Channel 3 Downstream Asynchronous Clock Input. Data is registered at rising edge.
SB3_CLKO	F13	OUT	LVTTL	Sideband Data Channel 3 Downstream Synchronous Clock Output. Data is registered at rising edge.
SB3_D[1:0]	E13,F14	IN	LVTTL	Sideband Data Channel 3 Downstream Input
Audio Interface				
AI_C0	C2	IN	LVTTL	S/P-DIF Audio Channel 0
AI_C1	C1	IN	LVTTL	S/P-DIF Audio Channel 1
AI_C2	D2	IN	LVTTL	S/P-DIF Audio Channel 2
AI_C3	D1	IN	LVTTL	S/P-DIF Audio Channel 3
Other Signals				
RESET#	B3	IN	LVTTL	Asynchronous Hardware Reset (active LOW)
ERROR	A2	OUT	LVTTL	Pixel Buffer Overrun
CFG_CYC	A1	OUT	LVTTL	Indicates that the configuration process is active
OSC	A6	IN	LVTTL	Reference Oscillator Input (see chapter 3.7)
CAP1	C11	IN	A	Loop filter pin of Downlink
CAP2	C12	IN	A	Loop filter pin of Downlink
NC	B1	–	–	Not connected

Table 4.1: INDT166B Transmitter Signals

* Configurable to LVTTL or Low Voltage Swing via V_{REF}-pin

Pin Name	Pin	Dir	Type	Description
Power Supply				
VCC_CORE	C3,D3,E4,G7,G8,G10,H3,H8,J3,J4,J8,J11,L5,L6,L10,M3,M8,M11, M12	IN	POWER	CMOS core supply
GND_CORE	D5,E5,E11,F4,F6,F11,G4,G6,H5,H6,H10,H12,J10,K3,K7,K8,K11, L3,L11,M9	IN	GROUND	
VCC_IO	C4,D4,E2,E3,G9,G11,H4,H7,H11,J7,J12,K5,K6,K9,K10,L9,L12,M4, M7	IN	POWER	CMOS digital I/O supply
GND_IO	A3,C5,E12,F3,F5,F12,G3,G5,G12,H9,J5,J6,J9,K4,K12,L4,L7,L8,M5, M6,M10	IN	GROUND	
VCC_CML	F7,F8	IN	POWER	CMOS chip-to-chip interface supply
GND_CML	F9,F10	IN	GROUND	
VCC_SX	B4	IN	POWER	CMOS uplink I/O supply
GND_SX	B5	IN	GROUND	
VCC_IA	E8,E10	IN	POWER	Bipolar Chip-to-chip interface supply
GND_IA	E7,E9	IN	GROUND	
VCC_A0	A7,A10,C6,C7,C10,D6,D12	IN	POWER	Bipolar downlink I/O supply
GND_A0	A8,A9,B7,B10,C8,C9,D11,E6	IN	GROUND	
VCC_A1	D9,D10	IN	POWER	Bipolar PLL supply
GND_A1	D7,D8	IN	GROUND	

Table 4.2: INDT166B Transmitter Power Supply

Pin Name	Pin	Pin Name	Pin	Pin Name	Pin	Pin Name	Pin
PX_D47	K13	PX_D35	N11	PX_D23	N5	PX_D11	L2
PX_D46	L14	PX_D34	P10	PX_D22	P4	PX_D10	K1
PX_D45	L13	PX_D33	N10	PX_D21	N4	PX_D9	K2
PX_D44	M14	PX_D32	P9	PX_D20	P3	PX_D8	J1
PX_D43	M13	PX_D31	N9	PX_D19	N3	PX_D7	J2
PX_D42	N14	PX_D30	P8	PX_D18	P2	PX_D6	H1
PX_D41	N13	PX_D29	N8	PX_D17	P1	PX_D5	H2
PX_D40	P14	PX_D28	P7	PX_D16	N1	PX_D4	G1
PX_D39	P13	PX_D27	N7	PX_D15	N2	PX_D3	G2
PX_D38	P12	PX_D26	P6	PX_D14	M1	PX_D2	F1
PX_D37	N12	PX_D25	N6	PX_D13	M2	PX_D1	F2
PX_D36	P11	PX_D24	P5	PX_D12	L1	PX_D0	E1

Table 4.3: INDT166B Transmitter Pixel Data Pin Numbers

4.2 INDR166B Receiver Signal Description

Pin Name	Pin	Dir	Type	Description
Link Interface				
RX0+	B8	IN	CML	Serial Data Input (Downlink 0)
RX0–	B9	IN	CML	
TX2+	A5	OUT	CML	Serial Data Output (Uplink)
TX2–	A4	OUT	CML	
LOCK0	B6	OUT	LVTTL	Lock Indicator. HIGH when PLL of Downlink is properly locked
SYNC0	B2	OUT	LVTTL	High, when the Downlink is frame synchronous
EQ	C5	IN	LVTTL	Selects the Downlink equalizer (LOW=OFF; HIGH=ON)
Pixel Interface				
PX_CLK	J14	OUT	LVTTL	Pixel clock 24 – 161 MHz,
PX_CLK_IN	A3	IN	LVTTL	Pixel clock 24 – 161 MHz, de-jitter feedback
PX_CLK_OUT	H14	OUT	LVTTL	Pixel clock 24 – 161 MHz, de-jitter feedback
PX_D[47:0]	(see Table 4.6)	OUT	LVTTL	Configurable parallel pixel data interface
PX_HSYNC	G13	OUT	LVTTL	Pixel data framing – Horizontal sync pulse (active HIGH)
PX_VSYNC	H13	OUT	LVTTL	Pixel data framing – Vertical sync pulse (active HIGH)
PX_DE	J13	OUT	LVTTL	Pixel data framing – Data enable (active HIGH)
Sideband Interface				
SB0_CLK	A13	OUT	LVTTL	Sideband Data Channel 0 Upstream Synchronous Clock Output. Data is registered at rising edge.
SB0_D[3:0] (CFG_D[3:0])	A11,B11,A 12,B12	IN	LVTTL	If CFG_CYC=0: Sideband Data Channel 0 Upstream Input If CFG_CYC=1: Configuration data input

Pin Name	Pin	Dir	Type	Description
SB1_CLKI	E13	IN	LVTTL	Sideband Data Channel 1 Upstream Asynchronous Clock Input. Data is registered at rising edge.
SB1_CLKO	E14	OUT	LVTTL	Sideband Data Channel 1 Upstream Synchronous Clock Output. Data is registered at rising edge.
SB1_D[1:0]	D14,D13	IN	LVTTL	Sideband Data Channel 1 Upstream Input
SB2_CLK	C13	OUT	LVTTL	Sideband Data Channel 2 Downstream Synchronous Clock Output. Data is provided aligned to rising edge.
SB2_D[3:0] (CFG_SEL[3:0])	A14,B14,B13,C14	OUT	LVTTL	If CFG_CYC=0: Sideband Data Channel 2 Downstream Output If CFG_CYC=1: Configuration vector output
SB3_CLK	G14	OUT	LVTTL	Sideband Data Channel 3 Downstream Synchronous Clock Output. Data is provided aligned to rising edge.
SB3_D[1:0]	F14,F13	OUT	LVTTL	Sideband Data Channel 3 Downstream Output
Audio Interface				
AI_C0	C2	OUT	LVTTL	S/P-DIF Audio Channel 0
AI_C1	C1	OUT	LVTTL	S/P-DIF Audio Channel 1
AI_C2	D2	OUT	LVTTL	S/P-DIF Audio Channel 2
AI_C3	D1	OUT	LVTTL	S/P-DIF Audio Channel 3
Other Signals				
RESET#	B3	IN	LVTTL	Asynchronous Hardware Reset (active LOW)
ERROR	A2	OUT	LVTTL	Pixel Clock Recovery Error
CFG_CYC	A1	OUT	LVTTL	Indicates that the configuration process is active
OSC	A6	IN	LVTTL	Reference Oscillator Input (see chapter 3.7)
CAP1	C11	IN	A	Loop filter pin of Downlink
CAP2	C12	IN	A	Loop filter pin of Downlink
NC	B1	–	–	Not connected

Table 4.4: INDR166B Receiver Signals

Pin Name	Pin	Dir	Type	Description
Power Supply				
VCC_CORE	C3,E3,G8,G10,J3,J4,J7,J11,L5,L6,L10,M8,M11	IN	POWER	CMOS core supply
GND_CORE	E4,E11,F4,F11,F12,G4,G6,H6,H10,J10,K8,K11,L3,L8,M9	IN	GROUND	
VCC_IO	C4,D3,D4,E2,F2,G7,G9,G11,H3,H4,H7,H8,H11,J8,J12,K5,K6,K9,K10,L9,L12,M3,M4,M7,M12	IN	POWER	CMOS digital I/O supply
GND_IO	D5,E5,E12,F3,F5,F6,G3,G5,G12,H5,H9,H12,J5,J6,J9,K3,K4,K7,K12,L4,L7,L11,M5,M6,M10	IN	GROUND	
VCC_CML	F7,F8	IN	POWER	CMOS chip-to-chip interface supply
GND_CML	F9,F10	IN	GROUND	
VCC_SX	B4	IN	POWER	CMOS uplink I/O supply
GND_SX	B5	IN	GROUND	
VCC_IA	E8,E10	IN	POWER	Bipolar Chip-to-chip interface supply
GND_IA	E7,E9	IN	GROUND	
VCC_A0	A7,A10,C6,C7,C10,D6,D12	IN	POWER	Bipolar downlink I/O supply
GND_A0	A8,A9,B7,B10,C8,C9,D11,E6	IN	GROUND	
VCC_A1	D9,D10	IN	POWER	Bipolar PLL supply
GND_A1	D7,D8	IN	GROUND	

Table 4.5: INDR166B Receiver Power Supply

Pin Name	Pin	Pin Name	Pin	Pin Name	Pin	Pin Name	Pin
PX_D47	K14	PX_D35	P11	PX_D23	P5	PX_D11	L1
PX_D46	K13	PX_D34	N11	PX_D22	N5	PX_D10	L2
PX_D45	L14	PX_D33	P10	PX_D21	P4	PX_D9	K1
PX_D44	L13	PX_D32	N10	PX_D20	N4	PX_D8	K2
PX_D43	M14	PX_D31	P9	PX_D19	P3	PX_D7	J1
PX_D42	M13	PX_D30	N9	PX_D18	N3	PX_D6	J2
PX_D41	N14	PX_D29	P8	PX_D17	P2	PX_D5	H1
PX_D40	N13	PX_D28	N8	PX_D16	P1	PX_D4	H2
PX_D39	P14	PX_D27	P7	PX_D15	N1	PX_D3	G1
PX_D38	P13	PX_D26	N7	PX_D14	N2	PX_D2	G2
PX_D37	P12	PX_D25	P6	PX_D13	M1	PX_D1	F1
PX_D36	N12	PX_D24	N6	PX_D12	M2	PX_D0	E1

Table 4.6: INDR166B Receiver Pixel Data Pin Numbers

4.3 INDT331B Transmitter Signal Description

Pin Name	Pin	Dir	Type	Description
Link Interface				
TX0+	B12	OUT	CML	Serial Data Output (Downlink 0)
TX0–	B13	OUT	CML	
TX1+	B5	OUT	CML	Serial Data Output (Downlink 1)
TX1–	B6	OUT	CML	
RX2+	A10	IN	CML	Serial Data Input (Uplink)
RX2–	A9	IN	CML	
LOCK0	B10	OUT	LVTTL	Lock Indicator 0. HIGH when PLL of Downlink 0 is properly locked
LOCK1	B3	OUT	LVTTL	Lock Indicator 1. HIGH when PLL of Downlink 1 is properly locked
SYNC2	C2	OUT	LVTTL	HIGH when the Uplink is frame synchronous
Pixel Interface				
PX_CLK+	T18	IN	LVTTL*	Pixel clock 24 – 161 MHz, diff + or single-ended
PX_CLK–	R18	IN	LVTTL*	Pixel clock 24 – 161 MHz, diff – pull to GND in single ended mode
PX_D[47:0]	(see Table 4.9)	IN	LVTTL*	Configurable parallel pixel data interface
PX_HSYNC	R17	IN	LVTTL*	Pixel data framing – Horizontal sync pulse (active HIGH)
PX_VSYNC	P18	IN	LVTTL*	Pixel data framing – Vertical sync pulse (active HIGH)
PX_DE	P17	IN	LVTTL*	Pixel data framing – Data enable (active HIGH)
VREF	N18	IN	A	Configures the input level of the pixel interface
Sideband Interface				
SB0_CLK	C18	OUT	LVTTL	Sideband Data Channel 0 Upstream Synchronous Clock Output. Data is provided aligned to rising edge.
SB0_D[3:0] (CFG_SEL[3:0])	A16,A17,A18,B18	OUT	LVTTL	If CFG_CYC=0: Sideband Data Channel 0 Upstream Output If CFG_CYC=1: Configuration vector output
SB1_CLK	G18	OUT	LVTTL	Sideband Data Channel 1 Upstream Synchronous Clock Output. Data is provided aligned to rising edge.
SB1_ D[1:0]	F18,F17	OUT	LVTTL	Sideband Data Channel 1 Upstream Output
SB2_CLK	E17	OUT	LVTTL	Sideband Data Channel 2 Downstream Synchronous Clock Output. Data is registered at rising edge.
SB2_D[3:0] (CFG_D[3:0])	C17,D18, D17,E18	IN	LVTTL	If CFG_CYC=0: Sideband Data Channel 2 Downstream Input If CFG_CYC=1: Configuration data input
SB3_CLKI	J18	IN	LVTTL	Sideband Data Channel 3 Downstream Asynchronous Clock Input. Data is registered at rising edge.
SB3_CLKO	H17	OUT	LVTTL	Sideband Data Channel 3 Downstream Synchronous Clock Output. Data is registered at rising edge.
SB3_D[1:0]	G17,H18	IN	LVTTL	Sideband Data Channel 3 Downstream Input
SB4_CLKI	N17	IN	LVTTL	Sideband Data Channel 4 Downstream Asynchronous Clock Input. Data is registered at rising edge.
SB4_CLKO	M18	OUT	LVTTL	Sideband Data Channel 4 Downstream Synchronous Clock Output. Data is registered at rising edge.
SB4_D[1:0]	K18,L18	IN	LVTTL	Sideband Data Channel 1 Downstream Input
Audio Interface				
AI_C0	D2	IN	LVTTL	S/P-DIF Audio Channel 0
AI_C1	D1	IN	LVTTL	S/P-DIF Audio Channel 1
AI_C2	E1	IN	LVTTL	S/P-DIF Audio Channel 2
AI_C3	F1	IN	LVTTL	S/P-DIF Audio Channel 3
Other Signals				
RESET#	A2	IN	LVTTL	Asynchronous Hardware Reset. Active LOW
ERROR	B2	OUT	LVTTL	Pixel Buffer Overrun
CFG_CYC	B1	OUT	LVTTL	Indicates that the configuration process is active
OSC	A3	IN	LVTTL	Reference Oscillator Input (see chapter 3.7)
CAP1	A15	IN	A	Loop filter pin Downlink 0
CAP2	B15	IN	A	Loop filter pin Downlink 0
CAP3	A8	IN	A	Loop filter pin Downlink 1
CAP4	B8	IN	A	Loop filter pin Downlink 1
NC	C1	–	–	Not connected

Table 4.7: INDT331B Transmitter Signals

* Configurable to LVTTL or Low Voltage Swing via V_{REF}-pin

Pin Name	Pin	Dir	Type	Description
Power Supply				
VCC_CORE	G3,G4,G9,G12,H4,J4,J8,J12,J15,J16,J17,L6,L10,L14,N2,N3,N4,N8, N12,R6,R10,R14,T6,T10,T14	IN	POWER	CMOS core supply
GND_CORE	F2,G7,G13,G14,H6,H10,H14,J2,J3,K2,K4,K8,K12,K15,K16,K17,L2, M6,M10,M14,P4,P8,P12,P15,P16,T3,T4	IN	GROUND	
VCC_IO	G2,G5,G8,G10,G11,G15,G16,H2,H3,H7,H8,H11,H12,H15,H16,J7, J11,K5,K6,K9,K10,K13,K14,L5,L9,L13,M2,M3,M4,M7,M8,M11,M12, M15,M16,M17,N7,N11,N15,N16,P5,P6,P9,P10,P13,P14,R5,R9, R13,T5,T9,T13	IN	POWER	CMOS digital I/O supply
GND_IO	A1,B16,B17,C16,D9,D16,E2,E3,E9,E15,E16,F3,F8,F9,F10,F15,F16, G6,H5,H9,H13,J5,J6,J9,J10,J13,J14,K3,K7,K11,L3,L4,L7,L8,L11, L12,L15,L16,L17,M5,M9,M13,N5,N6,N9,N10,N13,N14,P3,P7,P11, R3,R4,R7,R8,R11,R12,R15,R16,T2,T7,T8,T11,T12,T15,T16,U2	IN	GROUND	
VCC_CML	F4,F5,F11,F12	IN	POWER	CMOS chip-to-chip interface supply
GND_CML	F6,F7,F13,F14	IN	GROUND	
VCC_SX	B9	IN	POWER	CMOS uplink I/O supply
GND_SX	C9	IN	GROUND	
VCC_IA	E6,E8,E12,E14	IN	POWER	Bipolar Chip-to-chip interface supply
GND_IA	E5,E7,E11,E13	IN	GROUND	
VCC_A0	A4,A7,A11,A14,C3,C4,C8,C10,C11,C15,D3,D8,D10,D15	IN	POWER	Bipolar downlink I/O supply
GND_A0	A5,A6,A12,A13,B4,B7,B11,B14,C5,C6,C7,C12,C13,C14,E4,E10	IN	GROUND	
VCC_A1	D6,D7,D13,D14	IN	POWER	Bipolar PLL supply
GND_A1	D4,D5,D11,D12	IN	GROUND	

Table 4.8: INDT331B Transmitter Power Supply

Pin Name	Pin	Pin Name	Pin	Pin Name	Pin	Pin Name	Pin
PX_D47	T17	PX_D35	U13	PX_D23	U7	PX_D11	T1
PX_D46	U18	PX_D34	V12	PX_D22	V6	PX_D10	R1
PX_D45	U17	PX_D33	U12	PX_D21	U6	PX_D9	R2
PX_D44	V18	PX_D32	V11	PX_D20	V5	PX_D8	P1
PX_D43	V17	PX_D31	U11	PX_D19	U5	PX_D7	P2
PX_D42	V16	PX_D30	V10	PX_D18	V4	PX_D6	N1
PX_D41	U16	PX_D29	U10	PX_D17	U4	PX_D5	M1
PX_D40	V15	PX_D28	V9	PX_D16	V3	PX_D4	L1
PX_D39	U15	PX_D27	U9	PX_D15	U3	PX_D3	K1
PX_D38	V14	PX_D26	V8	PX_D14	V2	PX_D2	J1
PX_D37	U14	PX_D25	U8	PX_D13	V1	PX_D1	H1
PX_D36	V13	PX_D24	V7	PX_D12	U1	PX_D0	G1

Table 4.9: INDT331B Transmitter Pixel Data Pin Numbers

4.4 INDR331B Receiver Signal Description

Pin Name	Pin	Dir	Type	Description
Link Interface				
RX0+	B12	IN	CML	Serial Data Input (Downlink 0)
RX0–	B13	IN	CML	
RX1+	B5	IN	CML	Serial Data Input (Downlink 1)
RX1–	B6	IN	CML	
TX2+	A10	OUT	CML	Serial Data Output (Uplink)
TX2–	A9	OUT	CML	
LOCK0	B10	OUT	LVTTL	Lock Indicator 0. HIGH when PLL of Downlink 0 is properly locked
LOCK1	B3	OUT	LVTTL	Lock Indicator 1. HIGH when PLL of Downlink 1 is properly locked
SYNC0	C1	OUT	LVTTL	HIGH when the Downlink 0 is frame synchronous
SYNC1	D1	OUT	LVTTL	HIGH when the Downlink 1 is frame synchronous
EQ	A2	IN	LVTTL	Selects the Downlink equalizer (LOW=OFF; HIGH=ON)
Pixel Interface				
PX_CLK	R18	OUT	LVTTL	Pixel clock 24 – 161 MHz,
PX_CLK_IN	B2	IN	LVTTL	Pixel clock 24 – 161 MHz, de-jitter feedback
PX_CLK_OUT	P18	OUT	LVTTL	Pixel clock 24 – 161 MHz, de-jitter feedback
PX_D[47:0]	(see Table 4.12)	OUT	LVTTL	Configurable parallel pixel data interface
PX_HSYNC	N18	OUT	LVTTL	Pixel data framing – Horizontal sync pulse (active HIGH)
PX_VSYNC	N17	OUT	LVTTL	Pixel data framing – Vertical sync pulse (active HIGH)
PX_DE	P17	OUT	LVTTL	Pixel data framing – Data enable (active HIGH)
Sideband Interface				
SB0_CLK	C18	OUT	LVTTL	Sideband Data Channel 0 Upstream Synchronous Clock Output. Data is registered at rising edge.
SB0_D[3:0] (CFG_D[3:0])	A16,A17,A18,B18	IN	LVTTL	If CFG_CYC=0: Sideband Data Channel 0 Upstream Input If CFG_CYC=1: Configuration data input
SB1_CLKI	G17	IN	LVTTL	Sideband Data Channel 1 Upstream Asynchronous Clock Input. Data is registered at rising edge.
SB1_CLKO	G18	OUT	LVTTL	Sideband Data Channel 1 Upstream Synchronous Clock Output. Data is registered at rising edge.
SB1_ D[1:0]	F18,F17	IN	LVTTL	Sideband Data Channel 1 Upstream Input
SB2_CLK	E17	OUT	LVTTL	Sideband Data Channel 2 Downstream Synchronous Clock Output. Data is provided aligned to rising edge.
SB2_D[3:0] (CFG_SEL[3:0])	C17,D18, D17,E18	OUT	LVTTL	If CFG_CYC=0: Sideband Data Channel 2 Downstream Output If CFG_CYC=1: Configuration vector output
SB3_CLK	M18	OUT	LVTTL	Sideband Data Channel 3 Downstream Synchronous Clock Output. Data is provided aligned to rising edge.
SB3_D[1:0]	K18,L18	OUT	LVTTL	Sideband Data Channel 3 Downstream Output
SB4_CLK	J18	OUT	LVTTL	Sideband Data Channel 4 Downstream Synchronous Clock Output. Data is provided aligned to rising edge.
SB4_D[1:0]	H18,H17	OUT	LVTTL	Sideband Data Channel 4 Downstream Output
Audio Interface				
AI_C0	E1	OUT	LVTTL	S/P-DIF Audio Channel 0
AI_C1	F1	OUT	LVTTL	S/P-DIF Audio Channel 1
AI_C2	G1	OUT	LVTTL	S/P-DIF Audio Channel 2
AI_C3	H1	OUT	LVTTL	S/P-DIF Audio Channel 3
Other Signals				
RESET#	A1	IN	LVTTL	Asynchronous Hardware Reset (active LOW)
ERROR	B1	OUT	LVTTL	Pixel Clock Recovery Error
CFG_CYC	C2	OUT	LVTTL	Indicates that the configuration process is active
OSC	A3	IN	LVTTL	Reference Oscillator Input (see chapter 3.7)
CAP1	A15	IN	A	Loop filter pin Downlink 0
CAP2	B15	IN	A	Loop filter pin Downlink 0
CAP3	A8	IN	A	Loop filter pin Downlink 1
CAP4	B8	IN	A	Loop filter pin Downlink 1

Table 4.10: INDR331B Receiver Signals

Pin Name	Pin	Dir	Type	Description
Power Supply				
VCC_CORE	G4,G9,G12,H3,H4,J3,J4,J8,J12,J15,J16,J17,L6,L10,L14,N3,N4,N8, N12,R6,R10,R14,T6,T10,T14	IN	POWER	CMOS core supply
GND_CORE	E3,F15,G7,G13,H6,H10,H14,K3,K4,K8,K12,K15,K16,K17,L3,L4,M6, M10,M14,P4,P8,P12,P15,P16,R4,R16,T4	IN	GROUND	
VCC_IO	G2,G3,G5,G8,G10,G11,G15,G16,H2,H7,H8,H11,H12,H15,H16,J2, J7,J11,K5,K6,K9,K10,K13,K14,L5,L9,L13,M3,M4,M7,M8,M11,M12,M15,M16 ,M17,N2,N7,N11,N15,N16,P5,P6,P9,P10,P13,P14,R5,R9,R13,T5,T9,T13	IN	POWER	CMOS digital I/O supply
GND_IO	B16,B17,C16,D2,D9,D16,E2,E9,E15,E16,F2,F3,F8,F9,F10,F16, G6,G14,H5,H9,H13,J5,J6,J9,J10,J13,J14,K2,K7,K11,L2,L7,L8,L11, L12,L15,L16,L17,M2,M5,M9,M13,N5,N6,N9,N10,N13,N14,P3,P7, P11,R3,R7,R8,R11,R12,R15,T2,T3,T7,T8,T11,T12,T15,T16,U2	IN	GROUND	
VCC_CML	F4,F5,F11,F12	IN	POWER	CMOS chip-to-chip interface supply
GND_CML	F6,F7,F13,F14	IN	GROUND	
VCC_SX	B9	IN	POWER	CMOS uplink I/O supply
GND_SX	C9	IN	GROUND	
VCC_IA	E6,E8,E12,E14	IN	POWER	Bipolar Chip-to-chip interface supply
GND_IA	E5,E7,E11,E13	IN	GROUND	
VCC_A0	A4,A7,A11,A14,C3,C4,C8,C10,C11,C15,D3,D8,D10,D15	IN	POWER	Bipolar downlink I/O supply
GND_A0	A5,A6,A12,A13,B4,B7,B11,B14,C5,C6,C7,C12,C13,C14,E4,E10	IN	GROUND	
VCC_A1	D6,D7,D13,D14	IN	POWER	Bipolar PLL supply
GND_A1	D4,D5,D11,D12	IN	GROUND	

Table 4.11: INDR331B Receiver Power Supply

Pin Name	Pin	Pin Name	Pin	Pin Name	Pin	Pin Name	Pin
PX_D47	R17	PX_D35	U14	PX_D23	U8	PX_D11	V1
PX_D46	T18	PX_D34	V13	PX_D22	V7	PX_D10	U1
PX_D45	T17	PX_D33	U13	PX_D21	U7	PX_D9	T1
PX_D44	U18	PX_D32	V12	PX_D20	V6	PX_D8	R1
PX_D43	U17	PX_D31	U12	PX_D19	U6	PX_D7	R2
PX_D42	V18	PX_D30	V11	PX_D18	V5	PX_D6	P1
PX_D41	V17	PX_D29	U11	PX_D17	U5	PX_D5	P2
PX_D40	V16	PX_D28	V10	PX_D16	V4	PX_D4	N1
PX_D39	U16	PX_D27	U10	PX_D15	U4	PX_D3	M1
PX_D38	V15	PX_D26	V9	PX_D14	V3	PX_D2	L1
PX_D37	U15	PX_D25	U9	PX_D13	U3	PX_D1	K1
PX_D36	V14	PX_D24	V8	PX_D12	V2	PX_D0	J1

Table 4.12: INDR331B Receiver Pixel Data Pin Numbers

5 Pin Assignment

5.1 INDT166B Transmitter

	1	2	3	4	5	6	7	8	9	10	11	12	13	14
A	●CFG_CYC	ERROR	GND_IO	RX2-	RX2+	OSC	VCC_A0	GND_A0	GND_A0	VCC_A0	SB0_D3	SB0_D1	SB0_CLK	SB2_D3
B	NC	SYNC2	RESET#	VCC_SX	GND_SX	LOCK0	GND_A0	TX0+	TX0-	GND_A0	SB0_D2	SB0_D0	SB2_D1	SB2_D2
C	AI_C1	AI_C0	VCC_CORE	VCC_IO	GND_IO	VCC_A0	VCC_A0	GND_A0	GND_A0	VCC_A0	CAP1	CAP2	SB2_CLK	SB2_D0
D	AI_C3	AI_C2	VCC_CORE	VCC_IO	GND_CORE	VCC_A0	GND_A1	GND_A1	VCC_A1	VCC_A1	GND_A0	VCC_A0	SB1_D0	SB1_D1
E	PX_D0	VCC_IO	VCC_IO	VCC_CORE	GND_CORE	GND_A0	GND_IA	VCC_IA	GND_IA	VCC_IA	GND_CORE	GND_IO	SB3_D1	SB1_CLK
F	PX_D2	PX_D1	GND_IO	GND_CORE	GND_IO	GND_CORE	VCC_CML	VCC_CML	GND_CML	GND_CML	GND_CORE	GND_IO	SB3_CLKO	SB3_D0
G	PX_D4	PX_D3	GND_IO	GND_CORE	GND_IO	GND_CORE	VCC_CORE	VCC_CORE	VCC_IO	VCC_CORE	VCC_IO	GND_IO	VREF	SB3_CLKI
H	PX_D6	PX_D5	VCC_CORE	VCC_IO	GND_CORE	GND_CORE	VCC_IO	VCC_CORE	GND_IO	GND_CORE	VCC_IO	GND_CORE	PX_VSYNC	PX_DE
J	PX_D8	PX_D7	VCC_CORE	VCC_CORE	GND_IO	GND_IO	VCC_IO	VCC_CORE	GND_IO	GND_CORE	VCC_CORE	VCC_IO	PX_HSYNC	PX_CLK-
K	PX_D10	PX_D9	GND_CORE	GND_IO	VCC_IO	VCC_IO	GND_CORE	GND_CORE	VCC_IO	VCC_IO	GND_CORE	GND_IO	PX_D47	PX_CLK+
L	PX_D12	PX_D11	GND_CORE	GND_IO	VCC_CORE	VCC_CORE	GND_IO	GND_IO	VCC_IO	VCC_CORE	GND_CORE	VCC_IO	PX_D45	PX_D46
M	PX_D14	PX_D13	VCC_CORE	VCC_IO	GND_IO	GND_IO	VCC_IO	VCC_CORE	GND_CORE	GND_IO	VCC_CORE	VCC_CORE	PX_D43	PX_D44
N	PX_D16	PX_D15	PX_D19	PX_D21	PX_D23	PX_D25	PX_D27	PX_D29	PX_D31	PX_D33	PX_D35	PX_D37	PX_D41	PX_D42
P	PX_D17	PX_D18	PX_D20	PX_D22	PX_D24	PX_D26	PX_D28	PX_D30	PX_D32	PX_D34	PX_D36	PX_D38	PX_D39	PX_D40

Table 5.1: INDT166B GigaSTaR® Digital Display Link Transmitter Pin Assignment (Top View)

● = Pin A1 Identifier

5.2 INDR166B Receiver

	1	2	3	4	5	6	7	8	9	10	11	12	13	14
A	CFG_CYC	ERROR	PX_CLK_IN	TX2-	TX2+	OSC	VCC_A0	GND_A0	GND_A0	VCC_A0	SB0_D3	SB0_D1	SB0_CLK	SB2_D3
B	NC	SYNC0	RESET#	VCC_SX	GND_SX	LOCK0	GND_A0	RX0+	RX0-	GND_A0	SB0_D2	SB0_D0	SB2_D1	SB2_D2
C	AI_C1	AI_C0	VCC_CORE	VCC_IO	EQ	VCC_A0	VCC_A0	GND_A0	GND_A0	VCC_A0	CAP1	CAP2	SB2_CLK	SB2_D0
D	AI_C3	AI_C2	VCC_IO	VCC_IO	GND_IO	VCC_A0	GND_A1	GND_A1	VCC_A1	VCC_A1	GND_A0	VCC_A0	SB1_D0	SB1_D1
E	PX_D0	VCC_IO	VCC_CORE	GND_CORE	GND_IO	GND_A0	GND_IA	VCC_IA	GND_IA	VCC_IA	GND_CORE	GND_IO	SB1_CLKI	SB1_CLKO
F	PX_D1	VCC_IO	GND_IO	GND_CORE	GND_IO	GND_IO	VCC_CML	VCC_CML	GND_CML	GND_CML	GND_CORE	GND_CORE	SB3_D0	SB3_D1
G	PX_D3	PX_D2	GND_IO	GND_CORE	GND_IO	GND_CORE	VCC_IO	VCC_CORE	VCC_IO	VCC_CORE	VCC_IO	GND_IO	PX_HSYNC	SB3_CLK
H	PX_D5	PX_D4	VCC_IO	VCC_IO	GND_IO	GND_CORE	VCC_IO	VCC_IO	GND_IO	GND_CORE	VCC_IO	GND_IO	PX_VSYNC	PX_CLK_OUT
J	PX_D7	PX_D6	VCC_CORE	VCC_CORE	GND_IO	GND_IO	VCC_CORE	VCC_IO	GND_IO	GND_CORE	VCC_CORE	VCC_IO	PX_DE	PX_CLK
K	PX_D9	PX_D8	GND_IO	GND_IO	VCC_IO	VCC_IO	GND_IO	GND_CORE	VCC_IO	VCC_IO	GND_CORE	GND_IO	PX_D46	PX_D47
L	PX_D11	PX_D10	GND_CORE	GND_IO	VCC_CORE	VCC_CORE	GND_IO	GND_CORE	VCC_IO	VCC_CORE	GND_IO	VCC_IO	PX_D44	PX_D45
M	PX_D13	PX_D12	VCC_IO	VCC_IO	GND_IO	GND_IO	VCC_IO	VCC_CORE	GND_CORE	GND_IO	VCC_CORE	VCC_IO	PX_D42	PX_D43
N	PX_D15	PX_D14	PX_D18	PX_D20	PX_D22	PX_D24	PX_D26	PX_D28	PX_D30	PX_D32	PX_D34	PX_D36	PX_D40	PX_D41
P	PX_D16	PX_D17	PX_D19	PX_D21	PX_D23	PX_D25	PX_D27	PX_D29	PX_D31	PX_D33	PX_D35	PX_D37	PX_D38	PX_D39

Table 5.2: INDR166B GigaSTaR® Digital Display Link Receiver Pin Assignment (Top View)

5.3 INDT331B Transmitter

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
A	GND_IO	RESET#	OSC	VCC_A0	GND_A0	GND_A0	VCC_A0	CAP3	RX2-	RX2+	VCC_A0	GND_A0	GND_A0	VCC_A0	CAP1	SB0_D3	SB0_D2	SB0_D1
B	CFG_CYC	ERROR	LOCK1	GND_A0	TX1+	TX1-	GND_A0	CAP4	VCC_SX	LOCK0	GND_A0	TX0+	TX0-	GND_A0	CAP2	GND_IO	GND_IO	SB0_D0
C	NC	SYNC2	VCC_A0	VCC_A0	GND_A0	GND_A0	GND_A0	VCC_A0	GND_SX	VCC_A0	VCC_A0	GND_A0	GND_A0	GND_A0	VCC_A0	GND_IO	SB2_D3	SB0_CLK
D	AI_C1	AI_C0	VCC_A0	GND_A1	GND_A1	VCC_A1	VCC_A1	VCC_A0	GND_IO	VCC_A0	GND_A1	GND_A1	VCC_A1	VCC_A1	VCC_A0	GND_IO	SB2_D1	SB2_D2
E	AI_C2	GND_IO	GND_IO	GND_A0	GND_IA	VCC_IA	GND_IA	VCC_IA	GND_IO	GND_A0	GND_IA	VCC_IA	GND_IA	VCC_IA	GND_IO	GND_IO	SB2_CLK	SB2_D0
F	AI_C3	GND_CORE	GND_IO	VCC_CML	VCC_CML	GND_CML	GND_CML	GND_IO	GND_IO	GND_IO	VCC_CML	VCC_CML	GND_CML	GND_CML	GND_IO	GND_IO	SB1_D0	SB1_D1
G	PX_D0	VCC_IO	VCC_CORE	VCC_CORE	VCC_IO	GND_IO	GND_CORE	VCC_IO	VCC_CORE	VCC_IO	VCC_IO	VCC_CORE	GND_CORE	GND_CORE	VCC_IO	VCC_IO	SB3_D1	SB1_CLK
H	PX_D1	VCC_IO	VCC_IO	VCC_CORE	GND_IO	GND_CORE	VCC_IO	VCC_IO	GND_IO	GND_CORE	VCC_IO	VCC_IO	GND_IO	GND_CORE	VCC_IO	VCC_IO	SB3_CLKO	SB3_D0
J	PX_D2	GND_CORE	GND_CORE	VCC_CORE	GND_IO	GND_IO	VCC_IO	VCC_CORE	GND_IO	GND_IO	VCC_IO	VCC_CORE	GND_IO	GND_IO	VCC_CORE	VCC_CORE	VCC_CORE	SB3_CLKI
K	PX_D3	GND_CORE	GND_IO	GND_CORE	VCC_IO	VCC_IO	GND_IO	GND_CORE	VCC_IO	VCC_IO	GND_IO	GND_CORE	VCC_IO	VCC_IO	GND_CORE	GND_CORE	GND_CORE	SB4_D1
L	PX_D4	GND_CORE	GND_IO	GND_IO	VCC_IO	VCC_CORE	GND_IO	GND_IO	VCC_IO	VCC_CORE	GND_IO	GND_IO	VCC_IO	VCC_CORE	GND_IO	GND_IO	GND_IO	SB4_D0
M	PX_D5	VCC_IO	VCC_IO	VCC_IO	GND_IO	GND_CORE	VCC_IO	VCC_IO	GND_IO	GND_CORE	VCC_IO	VCC_IO	GND_IO	GND_CORE	VCC_IO	VCC_IO	VCC_IO	SB4_CLKO
N	PX_D6	VCC_CORE	VCC_CORE	VCC_CORE	GND_IO	GND_IO	VCC_IO	VCC_CORE	GND_IO	GND_IO	VCC_IO	VCC_CORE	GND_IO	GND_IO	VCC_IO	VCC_IO	SB4_CLKI	VREF
P	PX_D8	PX_D7	GND_IO	GND_CORE	VCC_IO	VCC_IO	GND_IO	GND_CORE	VCC_IO	VCC_IO	GND_IO	GND_CORE	VCC_IO	VCC_IO	GND_CORE	GND_CORE	PX_DE	PX_VSYNC
R	PX_D10	PX_D9	GND_IO	GND_IO	VCC_IO	VCC_CORE	GND_IO	GND_IO	VCC_IO	VCC_CORE	GND_IO	GND_IO	VCC_IO	VCC_CORE	GND_IO	GND_IO	PX_HSYNC	PX_CLK-
T	PX_D11	GND_IO	GND_CORE	GND_CORE	VCC_IO	VCC_CORE	GND_IO	GND_IO	VCC_IO	VCC_CORE	GND_IO	GND_IO	VCC_IO	VCC_CORE	GND_IO	GND_IO	PX_D47	PX_CLK+
U	PX_D12	GND_IO	PX_D15	PX_D17	PX_D19	PX_D21	PX_D23	PX_D25	PX_D27	PX_D29	PX_D31	PX_D33	PX_D35	PX_D37	PX_D39	PX_D41	PX_D45	PX_D46
V	PX_D13	PX_D14	PX_D16	PX_D18	PX_D20	PX_D22	PX_D24	PX_D26	PX_D28	PX_D30	PX_D32	PX_D34	PX_D36	PX_D38	PX_D40	PX_D42	PX_D43	PX_D44

Table 5.3: INDT331B GigaSTaR® Digital Display Link Transmitter Pin Assignment (Top View)

5.4 INDR331B Receiver

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
A	RESET#	EQ	OSC	VCC_A0	GND_A0	GND_A0	VCC_A0	CAP3	TX2-	TX2+	VCC_A0	GND_A0	GND_A0	VCC_A0	CAP1	SB0_D3	SB0_D2	SB0_D1
B	ERROR	PX_CLK_IN	LOCK1	GND_A0	RX1+	RX1-	GND_A0	CAP4	VCC_SX	LOCK0	GND_A0	RX0+	RX0-	GND_A0	CAP2	GND_IO	GND_IO	SB0_D0
C	SNYC0	CFG_CYC	VCC_A0	VCC_A0	GND_A0	GND_A0	GND_A0	VCC_A0	GND_SX	VCC_A0	VCC_A0	GND_A0	GND_A0	GND_A0	VCC_A0	GND_IO	SB2_D3	SB0_CLK
D	SYNC1	GND_IO	VCC_A0	GND_A1	GND_A1	VCC_A1	VCC_A1	VCC_A0	GND_IO	VCC_A0	GND_A1	GND_A1	VCC_A1	VCC_A1	VCC_A0	GND_IO	SB2_D1	SB2_D2
E	AI_C0	GND_IO	GND_CORE	GND_A0	GND_IA	VCC_IA	GND_IA	VCC_IA	GND_IO	GND_A0	GND_IA	VCC_IA	GND_IA	VCC_IA	GND_IO	GND_IO	SB2_CLK	SB2_D0
F	AI_C1	GND_IO	GND_IO	VCC_CML	VCC_CML	GND_CML	GND_CML	GND_IO	GND_IO	GND_IO	VCC_CML	VCC_CML	GND_CML	GND_CML	GND_CORE	GND_IO	SB1_D0	SB1_D1
G	AI_C2	VCC_IO	VCC_IO	VCC_CORE	VCC_IO	GND_IO	GND_CORE	VCC_IO	VCC_CORE	VCC_IO	VCC_IO	VCC_CORE	GND_CORE	GND_IO	VCC_IO	VCC_IO	SB1_CLKI	SB1_CLKO
H	AI_C3	VCC_IO	VCC_CORE	VCC_CORE	GND_IO	GND_CORE	VCC_IO	VCC_IO	GND_IO	GND_CORE	VCC_IO	VCC_IO	GND_IO	GND_CORE	VCC_IO	VCC_IO	SB4_D0	SB4_D1
J	PX_D0	VCC_IO	VCC_CORE	VCC_CORE	GND_IO	GND_IO	VCC_IO	VCC_CORE	GND_IO	GND_IO	VCC_IO	VCC_CORE	GND_IO	GND_IO	VCC_CORE	VCC_CORE	VCC_CORE	SB4_CLK
K	PX_D1	GND_IO	GND_CORE	GND_CORE	VCC_IO	VCC_IO	GND_IO	GND_CORE	VCC_IO	VCC_IO	GND_IO	GND_CORE	VCC_IO	VCC_IO	GND_CORE	GND_CORE	GND_CORE	SB3_D1
L	PX_D2	GND_IO	GND_CORE	GND_CORE	VCC_IO	VCC_CORE	GND_IO	GND_IO	VCC_IO	VCC_CORE	GND_IO	GND_IO	VCC_IO	VCC_CORE	GND_IO	GND_IO	GND_IO	SB3_D0
M	PX_D3	GND_IO	VCC_IO	VCC_IO	GND_IO	GND_CORE	VCC_IO	VCC_IO	GND_IO	GND_CORE	VCC_IO	VCC_IO	GND_IO	GND_CORE	VCC_IO	VCC_IO	VCC_IO	SB3_CLK
N	PX_D4	VCC_IO	VCC_CORE	VCC_CORE	GND_IO	GND_IO	VCC_IO	VCC_CORE	GND_IO	GND_IO	VCC_IO	VCC_CORE	GND_IO	GND_IO	VCC_IO	VCC_IO	PX_VSYNC	PX_HSYNC
P	PX_D6	PX_D5	GND_IO	GND_CORE	VCC_IO	VCC_IO	GND_IO	GND_CORE	VCC_IO	VCC_IO	GND_IO	GND_CORE	VCC_IO	VCC_IO	GND_CORE	GND_CORE	PX_DE	PX_CLK_OUT
R	PX_D8	PX_D7	GND_IO	GND_CORE	VCC_IO	VCC_CORE	GND_IO	GND_IO	VCC_IO	VCC_CORE	GND_IO	GND_IO	VCC_IO	VCC_CORE	GND_IO	GND_CORE	PX_D47	PX_CLK
T	PX_D9	GND_IO	GND_IO	GND_CORE	VCC_IO	VCC_CORE	GND_IO	GND_IO	VCC_IO	VCC_CORE	GND_IO	GND_IO	VCC_IO	VCC_CORE	GND_IO	GND_IO	PX_D45	PX_D46
U	PX_D10	GND_IO	PX_D13	PX_D15	PX_D17	PX_D19	PX_D21	PX_D23	PX_D25	PX_D27	PX_D29	PX_D31	PX_D33	PX_D35	PX_D37	PX_D39	PX_D43	PX_D44
V	PX_D11	PX_D12	PX_D14	PX_D16	PX_D18	PX_D20	PX_D22	PX_D24	PX_D26	PX_D28	PX_D30	PX_D32	PX_D34	PX_D36	PX_D38	PX_D40	PX_D41	PX_D42

Table 5.4: INDR331B GigaSTaR® Digital Display Link Receiver Pin Assignment (Top View)

6 Package Information

6.1 INDT/R166B

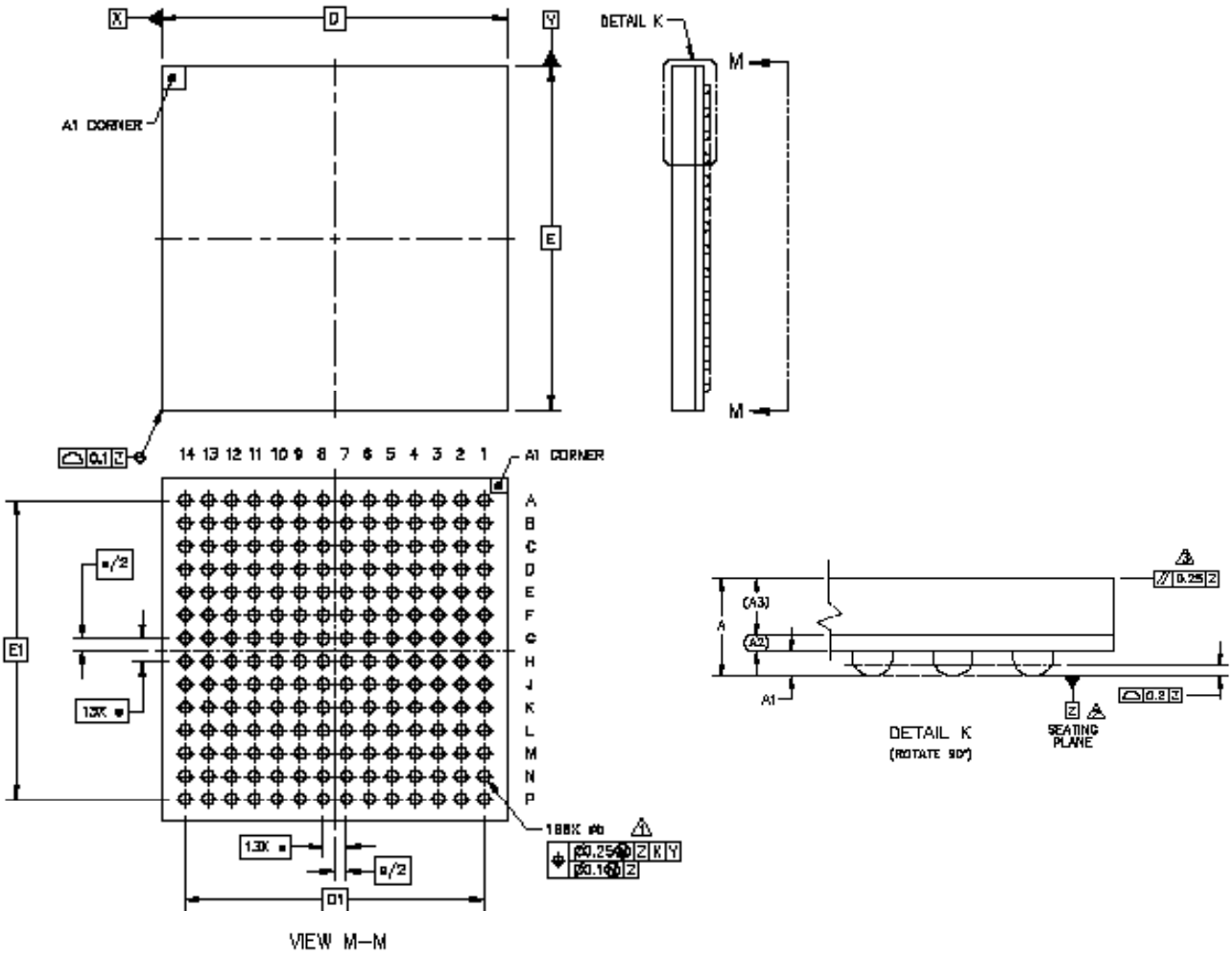


Figure 6.1: Package: BGA 196, 15 x 15 mm, 196 balls, 1 mm ball pitch

Dim	Min	Nom	Max
A	–		1.9
A1	0.36		0.46
A2		0.38 REF	
A3		1.0 REF	
b	0.44		0.64
D		15 BSC	
E		15 BSC	
e		1.0 BSC	
D1		13 BSC	
E1		13 BSC	
All dimensions and tolerances in mm!			

Figure 6.2: BGA 196 – Dimensions and Tolerances

6.2 INDT/R331B

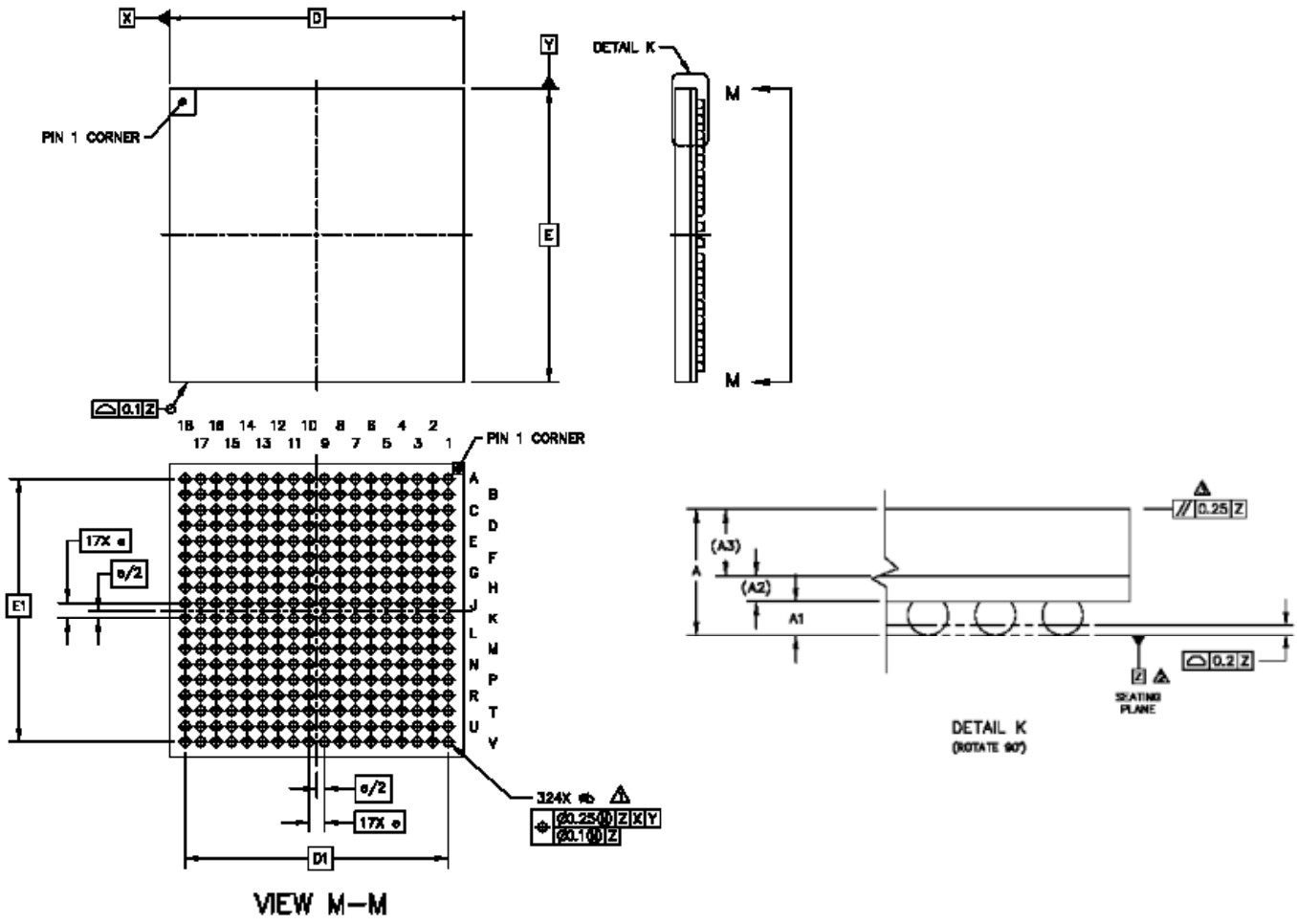


Figure 6.3: Package: BGA 324, 19 x 19 mm, 324 balls, 1 mm ball pitch

Dim	Min	Nom	Max
A	–		2.0
A1	0.4		0.6
A2		0.38 Ref	
A3		1.0 Ref	
b	0.55		0.7
D		19 BSC	
E		19 BSC	
e		1.0 BSC	
D1		17 BSC	
E1		17 BSC	
All dimensions and tolerances in mm!			

Figure 6.4: BGA 324 – Dimensions and Tolerances

7 Ordering and Product Availability

Ordering Code	Delivery Package	Minimum Packing Quantity	Status
INDT166B	Tray (in sealed dry pack)	126 units	Engineering Samples available by June '05
INDR166B	Tray (in sealed dry pack)	126 units	Engineering Samples available by June '05
IND166SK	Sample Kit (5 x Tx, 5 x Rx)	10 units	Engineering Samples available by June '05
INDT331B	Tray (in sealed dry pack)	84 units	Engineering Samples available by June '05
INDR331B	Tray (in sealed dry pack)	84 units	Engineering Samples available by June '05
IND331SK	Sample Kit (2 x Tx, 2 x Rx)	4 units	Engineering Samples available by June '05

Table 7.1: Product Availability

8 Revision History

The information contained in this data sheet supersedes information published in previous versions.
The following changes were made:

- v 0.1 Preliminary Data Sheet

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