Active Receive Mixer DC to 500 MHz

Preliminary Datasheet

AD8342

FEATURES

Broadband RF port: LF to 500 MHz
Conversion gain: 3 dB
Noise figure: 12 dB
Input IP3: 24 dBm
Input P_{1dB}: 8.5 dBm
LO drive: 0 dBm
External control of mixer bias for low power operation
Single-ended, 50 Ω LO input ports
High Input Impedance RF port
Single-supply operation: 5 V @ 97 mA
Power-down mode
Exposed paddle LFCSP: 3 mm × 3 mm

APPLICATIONS

Cellular base station receivers and transmitters
ISM receivers and transmitters
Radio links
RF Instrumentation

FUNCTIONAL BLOCK DIAGRAM

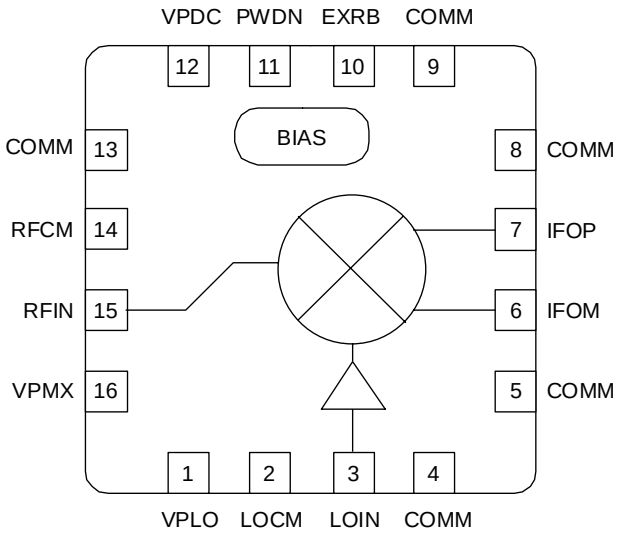

Figure 1.

GENERAL DESCRIPTION

The AD8342 is a high performance, broadband active mixer. It is well suited for demanding receive applications that require wide bandwidth on all ports and very low intermodulation distortion and noise figure.

The AD8342 provides a typical conversion gain of 3dB at 500 MHz. The integrated LO driver supports a 50 Ω input impedance with a low LO drive level, helping to minimize external component count.

The high input impedance RF port can be terminated and driven single ended or a matching network can be used for best noise or power match. The RF input accepts input signals as large as 1.7 V p-p or 8 dBm (re: 50 Ω) at P_{1dB}.

The open-collector differential outputs provide excellent balance and can be used with a differential filter or IF amplifier, such as the AD8369 or AD8351. These outputs may also be converted to a single-ended signal through the use of a matching network or a transformer (balun). When centered on the VPOS supply voltage, each of the differential outputs may swing 2.5 V p-p.

The AD8342 is fabricated on an Analog Devices proprietary, high performance SiGe IC process. The AD8342 is available in a 16-lead LFCSP package. It operates over a −40°C to +85°C temperature range. An evaluation board is also available.

Rev. PrB

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 **www.analog.com**
Fax: 781.326.8703

SPECIFICATIONS

V_S = 5 V, T_A = 25°C, f_{RF} = 500 MHz, f_{LO} = 600 MHz, LO power = 0 dBm, Z_O = 50 Ω, R_{BIAS} = 1.82 kΩ, unless otherwise noted.

Table 1.

Parameter	Conditions	Min	Typ	Max	Unit
RF INPUT INTERFACE	(Pin 15, RFIN and Pin 14, RFCM)				
Return Loss	Hi-Z input terminated off-chip		10		dB
DC Bias Level	Internally generated; port must be ac-coupled		2.5		V
OUTPUT INTERFACE					
Output Impedance	Differential impedance, f = 200 MHz		9||1		kΩ||pF
DC Bias Voltage	Externally generated	4.75	V_S	5.25	V
Power Range	Via a 4:1 balun			+13	dBm
LO INTERFACE					
LO Power		−10	0	+4	dBm
Return Loss			10		dB
DC Bias Voltage	Internally generated; port must be ac-coupled		V_S – 1.6		V
POWER-DOWN INTERFACE					
PWDN Threshold			V_S – 1.4		V
PWDN Response Time	Device enabled, IF output to 90% of its final level		0.4		µs
	Device disabled, supply current < 5 mA		0.01		µs
PWDN Input Bias Current	Device enabled		−80		µA
	Device disabled		+100		µA
POWER SUPPLY					
Positive Supply Voltage		4.75	5	5.25	V
Quiescent Current					
VPDC	Supply current for bias cells		5		mA
VPMX, IFOP, IFOM	Supply current for mixer, R_{BIAS} = 1.82 kΩ		57		mA
VPLO	Supply current for LO limiting amplifier		35		mA
Total Quiescent Current	V_S = 5 V	TBD	97	TBD	mA
Power-Down Current	Device disabled		500		µA

AC PERFORMANCE

V_S = 5 V, T_A = 25°C, LO power = 0 dBm, Z_O = 50 Ω, R_{BIAS} = 1.82 kΩ, unless otherwise noted.

Table 2.

Parameter	Conditions	Min	Typ	Max	Unit
RF Frequency Range		LF		500	MHz
LO Frequency Range	High Side LO	LF		850	MHz
IF Frequency Range	Note: the upper "IF" is when used as an upconverter	DC		350	MHz
Conversion Gain	f_{RF} = 460 MHz, f_{LO} = 550 MHz, f_{IF} = 90 MHz		3.2		dB
	f_{RF} = 238 MHz, f_{LO} = 286 MHz, f_{IF} = 48 MHz		3.4		dB
SSB Noise Figure	f_{RF} = 460 MHz, f_{LO} = 550 MHz, f_{IF} = 90 MHz		12.5		dB
	f_{RF} = 238 MHz, f_{LO} = 286 MHz, f_{IF} = 48 MHz		12.2		dB
Input Third-Order Intercept	f_{RF1} = 460 MHz, f_{RF2} = 461 MHz, f_{LO} = 550 MHz, f_{IF} = 90 MHz, each RF tone -10 dBm		22.5		dBm
	f_{RF1} = 238 MHz, f_{RF2} = 239 MHz, f_{LO} = 286MHz, f_{IF} = 45MHz, each RF tone -10 dBm		23.5		dBm
Input Second-Order Intercept	f_{RF1} = 460 MHz, f_{RF2} = 480 MHz, f_{LO} = 550 MHz, f_{IF} = 90 MHz		48		dBm
	f_{RF1} = 238 MHz, f_{RF2} = 248 MHz, f_{LO} = 286 MHz, f_{IF} = 48 MHz		48		dBm
Input 1 dB Compression Point	f_{RF} = 460 MHz, f_{LO} = 550 MHz, f_{IF} = 90 MHz		8.5		dBm
	f_{RF} = 238 MHz, f_{LO} = 286 MHz, f_{IF} = 48 MHz		8.5		dBm
LO to IF Output Leakage	LO Power = 0 dBm, f_{RF} = 500 MHz, f_{LO} = 600 MHz		TBD		dBm
LO to RF Input Leakage	LO Power = 0 dBm, f_{RF} = 500 MHz, f_{LO} = 600 MHz		TBD		dBm
2xLO to IF Output Leakage	LO Power = 0 dBm, f_{RF} = 500 MHz, f_{LO} = 600 MHz		TBD		dBm
RF to IF Output Leakage	RF Power = -10 dBm, f_{RF} = 500 MHz, f_{LO} = 600 MHz		TBD		dBm
IF/2 Spurious	RF Power = -10 dBm, f_{RF} = 500 MHz, f_{LO} = 600 MHz		TBD		dBm

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Supply Voltage, V_S	5.5 V
RF Input Level	12 dBm
LO Input Level	12 dBm
PWDN Pin	V_S + 0.5 V
IFOP, IFOM Bias Voltage	5.5 V
Minimum Resistor from EXRB to COMM	1.82 kΩ
Internal Power Dissipation	580 mW
θ_{JA}	77°C/W
Maximum Junction Temperature	125°C
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature Range (Soldering 60 sec)	300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

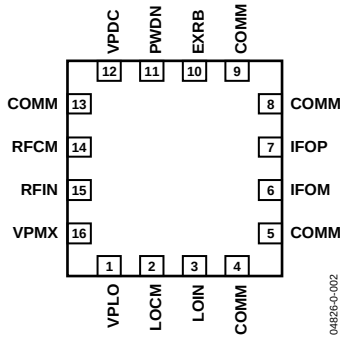

Figure 2. 16-Lead LFCSP

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Function
1	VPLO	Positive Supply Voltage for the LO Buffer: 4.75 V to 5.25 V.
2	LOCM	AC Ground for Limiting LO Amplifier, AC-Coupled to Ground.
3	LOIN	LO Input. Nominal input level 0 dBm, input level range −10 dBm to +4 dBm, re: 50 Ω, ac-coupled.
4, 5, 8, 9, 13	COMM	Device Common (DC Ground).
6, 7	IFOM, IFOP	Differential IF Outputs; Open Collectors, Each Requires DC Bias of 5.00 V (Nominal).
10	EXRB	Mixer Bias Voltage, Connect Resistor from EXRB to Ground, Typical Value of 1.82 kΩ Sets Mixer Current to Nominal Value. Minimum resistor value from EXRB to ground = 1.82 kΩ.
11	PWDN	Connect to Ground for Normal Operation. Connect pin to V_S for disable mode.
12	VPDC	Positive Supply Voltage for the DC Bias Cell: 4.75 V to 5.25 V.
14	RFCM	AC Ground for RF Input, AC-Coupled to Ground.
15	RFIN	RF Input. Must be ac-coupled.
16	VPMX	Positive Supply Voltage for the Mixer: 4.75 V to 5.25 V.

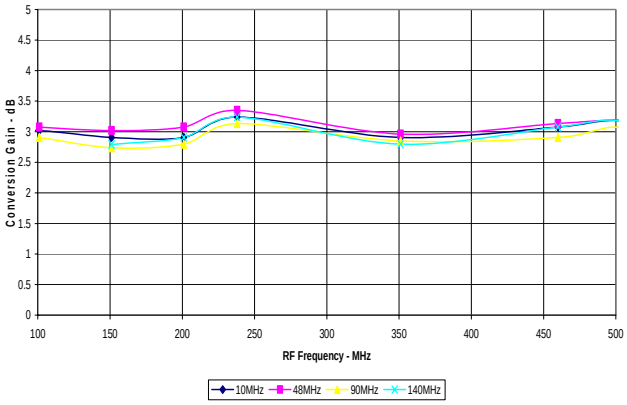

Figure 3. Conversion Gain vs. RF Frequency for Multiple IF Frequencies

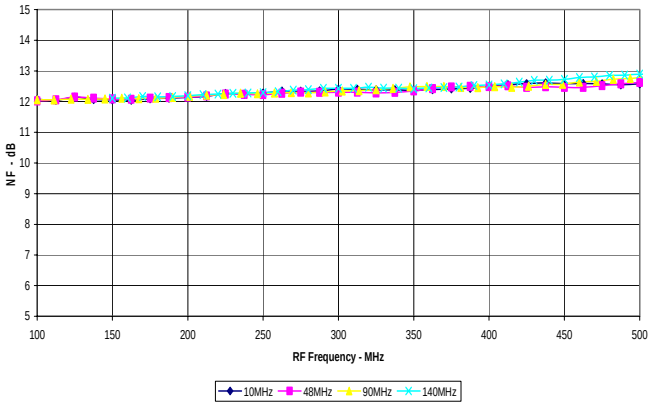

Figure 4. Single Sideband Noise Figure vs RF Frequency for Multiple IF Frequencies

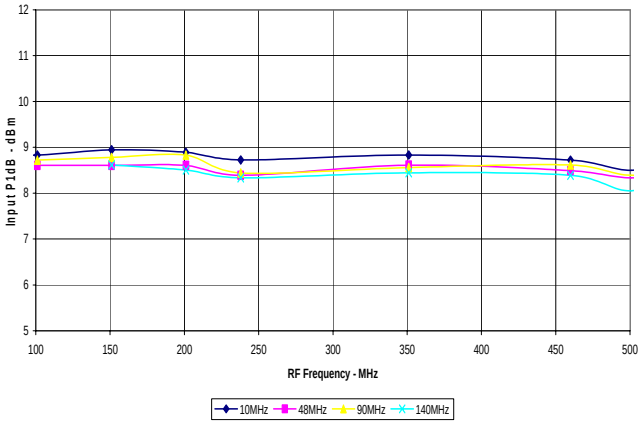

Figure 5. Input Compression Point vs RF Frequency for Multiple IF Frequencies

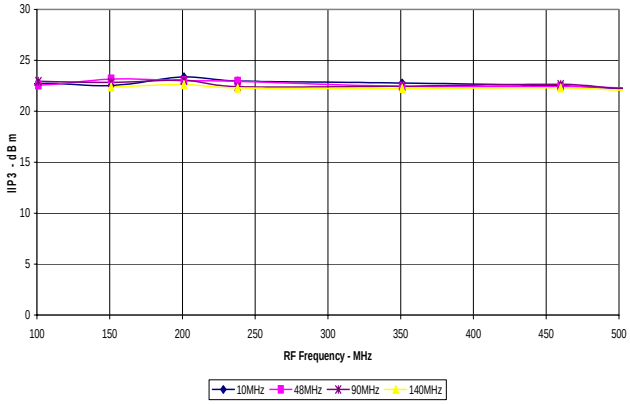

Figure 6.. Input IP3 vs. RF Frequency for Multiple IF Frequencies

EVALUATION BOARD

An evaluation board is available for the AD8342. The evaluation board is configured for single-ended signaling at the IF output port via a balun transformer. The schematic for the evaluation board is presented in Figure 7.

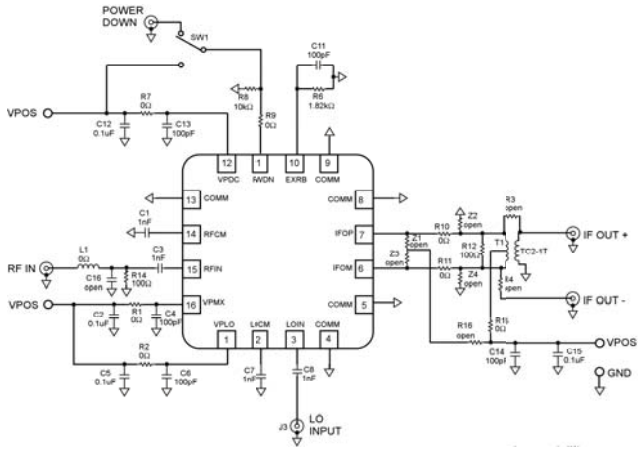

Figure 7. Customer Evaluation Board

Table 5. Evaluation Boards Configuration Options

Component	Function	Default Conditions
R1, R2, R7, C2, C4, C5, C6, C12, C13, C14, C15	**Supply Decoupling**. Power supply decoupling resistors and filter capacitors.	R1, R2, R7 = 0 Ω (Size 0603) C4, C6, C13, C14 = 100 pF (Size 0603) C2, C5, C12, C15 = 0.1 µF (Size 0603)
R3, R4, R15, R16	Jumpers for IF output interface. The eval board can be configured to provide a balanced differential output by removing R15 and T1 and adding 0-Ω resistors for R3, R4, and R16 and adding suitable choke inductors for Z1 and Z3.	R3=R4=R16=open R15=0 Ω (Size 0402)
R6, C11	R_{BIAS} resistor that sets the bias current for the mixer core. The capacitor provides ac bypass for R6.	R6 = 1.82 kΩ (Size 0603) C11 = 100 pF (Size 0603)
C3, R14, C16, L1	**RF Input**. **C3** Provides dc block for RF input. R14 provides a resistive input termination. C16 and L1 are provided for reactive matching the input.	C3 = 1000 pF (Size 0402) R14 = 100 Ω (Size 0603) C16 = open (Size 0603) L1 = 0 Ω (Size 0603)
C1	**RF Common AC Coupling**. Provides dc block for RF input common connection.	C1 = 1000 pF (Size 0402)
C8	**LO Input AC Coupling**. Provides dc block for the LO input.	C8 = 100 pF (Size 0402)
C7	**LO Common AC Coupling**. Provides dc block for LO input common connection.	C7 = 100 pF (Size 0402)
SW1 R8, R9	**Power Down**. The part is on when the PWDN is connected to a low potential. The part is disabled when PWDN is connected to the positive supply via SW1. R8 provides a pull-down when SW1 is open and can be used as a termination when excercising the PWDN feature with an external generator.	R8 = 10 kΩ (Size 0603) R9 = 0 Ω (Size 0603)
T1, R10, R11, R12, Z1, Z2, Z3, Z4	**IF Output Interface**. R12 Provides a real 100 -Ω termination to the open collector outputs. T1 converts differential, high impedance IF output to single-ended. The center tap of the primary is used to supply the bias voltage (V_S) to the IF output pins.	T1 = TC2-1T, 2:1 (Mini-Circuits) R10=R11 = 0 Ω (Size 0603) R12 = 100 Ω (Size 0603) Z1 = Z2 = Open Z3 = Z4 = Open

OUTLINE DIMENSIONS

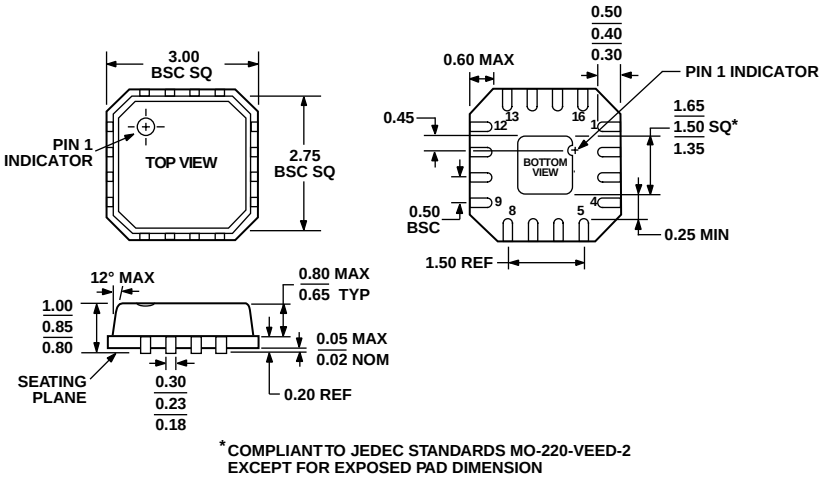

Figure 7. 16-Lead Lead Frame Chip Scale Package [LFCSP]
3 mm × 3 mm Body (CP-16-3)
Dimensions in millimeters