Hot Swap Controller and I²C Power Monitor with Convert Pin

Preliminary Technical Data

ADM1176

FEATURES

Allows Safe Board Insertion and Removal from a Live Backplane
Controls Supply Voltages from 3.15 V to 14V
Precision Current Sense Amplifier
Precision Voltage Input
12-bit ADC for Current and Voltage Readback
Charge Pumped Gate Drive for External N-FET Switch
Adjustable Analog Current Limit with Circuit Breaker
Fast Response Limits Peak Fault Current
Automatic Retry or Latch-Off On Current Fault
Programmable hot swap timing via TIMER pin
Active-high ON pin
I²C Fast Mode compliant interface (400 KHz max)
Two address pins allow 16 devices on the same bus
10-lead MSOP package

APPLICATIONS

Power Monitoring/Power Budgeting
Central office Equipment
Telecommunication and Datacommunication Equipment
PC/Servers

GENERAL DESCRIPTION

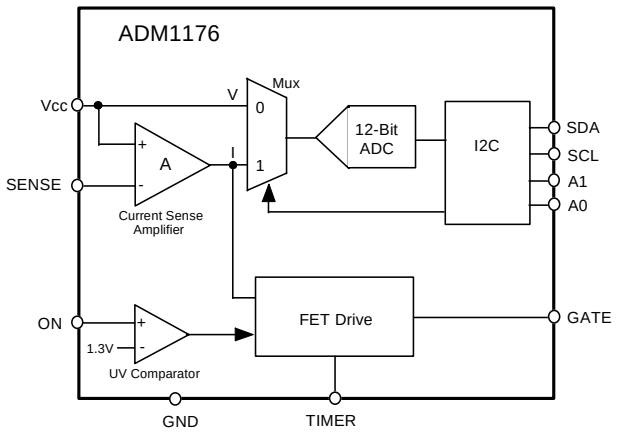
The ADM1176 is an integrated hot-swap controller which offers digital current and voltage monitoring via an on-chip 12-bit ADC, communicated through an I²C interface.

An internal current sense amplifier senses voltage across the sense resistor in the power path via the VCC and SENSE pins.

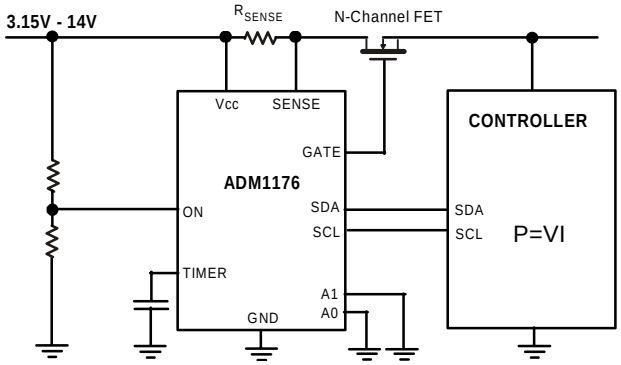
The ADM1176 limits the current through this resistor by controlling the gate voltage of an external N-channel FET in the power path, via the GATE pin. The sense voltage (and hence the inrush current) is kept below a preset maximum.

The ADM1176 protects the external FET by limiting the time that it spends with the maximum current running in it. This current limit period is set by the choice of capacitor attached to the TIMER pin. Additionally, the device provides protection from overcurrent events at times after the hot-swap event is complete. In the case of a short-circuit event the current in the sense resistor will exceed an overcurrent trip threshold, and the FET will be switched off immediately by pulling down the GATE pin.

FUNCTIONAL BLOCK DIAGRAM



APPLICATIONS DIAGRAM



A 12-bit ADC can measure the current seen in the sense resistor, and also the supply voltage on the VCC pin.

An industry standard I²C interface allows a controller to read current and voltage data from the ADC. Measurements can be initiated by an I²C command. Alternatively the ADC can run continuously and the user can read the latest conversion data whenever it is required. Up to 4 unique I²C addresses can be created by the way the ADR pin is connected.

The ADM1176 is packaged in a 10-lead MSOP package.

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REVISION HISTORY

May 06—Revision PrD: Preliminary Version

ADM1176—Specifications

Table 1. V_{CC} = 3.15V to 14V, T_A = -40°C to +85°C, Typical Values at T_A = +25°C unless otherwise noted.

Parameter	Min	Typ	Max	Units	Conditions
VCC Pin					
Operating Voltage Range, V_{VCC}	3.15		14	V	
Supply Current, I_{CC}		1.6	3	mA	
Undervoltage Lockout, V_{UVLO}		2.8		V	V_{VCC} Rising
Undervoltage Lockout Hysteresis, $V_{UVLOHYST}$		25		mV	
ON Pin					
Input Current, I_{INON}	−100	0	+100	nA	
Trip Threshold, V_{ONTH}		1.3		V	ON rising
Trip Threshold Hysteresis, V_{ONHYST}		80		mV	
Glitch Filter Time		3		µs	
SENSE Pin					
Input Leakage, I_{SENSE}	−1		+1	µA	$V_{SENSE} = V_{VCC}$
Overcurrent Fault Timing Threshold, V_{OCTIM}	85			mV	$V_{OCTRIM} = (V_{VCC} - V_{SENSE})$, Fault timing starts on the TIMER pin
Overcurrent Limit Threshold, $V_{LIM\ M}$	90	100	110	mV	$V_{LIM} = (V_{VCC} - V_{SENSE})$, Closed loop regulation to a current limit
Fast Overcurrent Trip Threshold, V_{OCFAST}			115	mV	$V_{OCFAST} = (V_{VCC} - V_{SENSE})$, Gate pulldown current turned on
GATE Pin					
Drive Voltage, V_{GATE}	5	7	10	V	$V_{GATE} - V_{VCC}$, V_{VCC} = 3.15 V
Drive Voltage, V_{GATE}	6	8	12	V	$V_{GATE} - V_{VCC}$, V_{VCC} = 5 V
Drive Voltage, V_{GATE}	5	7	10	V	$V_{GATE} - V_{VCC}$, V_{VCC} = 13.2 V
Pullup Current	10	12	14	µA	V_{GATE} = 0 V
Pulldown Current		2		mA	V_{GATE} = 3 V, V_{VCC} > UVLO
Pulldown Current		25		mA	V_{GATE} = 3 V, V_{VCC} < UVLO
TIMER Pin					
Pull-Up Current (Power On Reset), $I_{TIMERUPPOR}$	−4	−5	−6	µA	Initial Cycle, V_{TIMER} = 1 V
Pull-Up Current (Fault Mode), $I_{TIMERUPFAULT}$	−48	−60	−72	µA	During Current Fault, V_{TIMER} = 1 V
Pull-Down Current (Retry Mode), $I_{TIMERDNRETRY}$		2	2.5	µA	After current fault and during a cool-down period on a retry device, V_{TIMER} = 1 V
Pull-Down Current, $I_{TIMERDN}$		100		µA	Normal Operation, V_{TIMER} = 1 V
Trip Threshold High, V_{TIMERH}	1.235	1.3	1.365	V	TIMER rising
Trip Threshold Low, V_{TIMERL}	0.18	0.2	0.22	V	TIMER falling
A0, A1 Pins					
Set address to 00, $V_{ADRLOWV}$	0		0.8	V	Low state
Set address to 01, $R_{ADRLOWZ}$	135	150	165	kΩ	Resistor to ground state, load pin with specified resistance for 01 decode
Set address to 10, $I_{ADRHIGHZ}$	−1		+1	µA	Open state, maximum load allowed on A0 or A1 pin for 10 decode
Set address to 11, $V_{ADRHIGHV}$	2		5.5	V	High state
Input current for 00 decode, I_{ADRLOW}		3	10	µA	V_{ADR} = 2.0 V to 5.5 V
Input current for 11 decode, $I_{ADRHIGH}$	−40	−22		µA	V_{ADR} = 0 V to 0.8 V

Parameter	Min	Typ	Max	Units	Conditions
MONITORING ACCURACY[1]					
Current Sense Absolute Accuracy	TBD		TBD	%	V_{SENSE} = 75 mV
	-2.3		+2.3	%	V_{SENSE} = 75 mV, @ 0°C to +70°C
	TBD		TBD	%	V_{SENSE} = 50 mV
	-2.5		+2.5	%	V_{SENSE} = 50 mV, @ 0°C to +70°C
	TBD		TBD	%	V_{SENSE} = 25 mV
	-2.8		+2.8	%	V_{SENSE} = 25mV, @ 0°C to +70°C
	-3.5		+3.5	%	V_{SENSE} = 12.5 mV, @ 25°C
Current Sense Accuracy, T_C		±0.01		%/°C	
V_{SENSE} for ADC full-scale		105		mV	
Voltage Sense Accuracy	−1.5		+1.5	%	V_{VCC} = 3.15 V to 5.5V (VRANGE = 1)
	−1.5		+1.5	%	V_{VCC} = 10.8 V to 26V (VRANGE = 1)
V_{CC} for ADC full-scale, low range		6.656		V	VRANGE = 1
V_{CC} for ADC full-scale, high range		26.628[2]		V	VRANGE = 0
I^2C TIMING[3]					
Low level input voltage, V_{IL}			0.99	V	
High level input voltage, V_{IH}	2.31			V	
Low level output voltage on SDA, V_{OL}			0.4	V	I_{OL} = 3mA
Output fall time on SDA from V_{IHMIN} to V_{ILMAX}	20+0.1C_B		250	ns	C_B = bus capacitance from SDA to GND
Maximum width of spikes suppressed by input filtering on SDA and SCL pins	50		250	ns	
Input current, I_I, on SDA/SCL when not driving out a logic low	−10		+10	µA	
Input capacitance on SDA/SCL		5		pF	
SCL clock frequency, f_{SCL}			400	kHz	
LOW period of the SCL clock	600			ns	
HIGH period of the SCL clock	1300			ns	
Setup time for a repeated START condition, $t_{SU;STA}$	600			ns	
SDA output data hold time, $t_{HD;DAT}$	100			ns	
Set-up time for a stop condition, $t_{SU;STO}$	600			ns	
Bus free time between a STOP and a START condition, t_{BUF}	1300			ns	
Capacitive load for each bus line			400	pF	

[1] Monitoring accuracy is a measure of the error in a code that is read back for a particular voltage/current. This is a combination of amplifier error, reference error and ADC error.
[2] The maximum operating voltage is limited to VVCC =14 V which corresponds to an ADC code of 871.
[3] The following conditions apply to all timing specifications: VBUS =3.3V, TA =25°C. All timings refer to VIHMIN and VILMAX.

Absolute Maximum Ratings

Table 2. ADM1176 Absolute Maximum Ratings

Parameter	**Rating**
V_{CC} Pin	20V
SENSE Pins	20V
TIMER Pin	-0.3V to +6V
ON Pin	-0.3V to +20V
GATE Pin	30V
SDA, SCL Pins	-0.3V to +6V
A0, A1 Pins	-0.3V to +6V
Power Dissipation	TBD
Storage Temperature	–65°C to +125°C
Operating Temperature Range	–40°C to +85°C
Lead Temperature Range (Soldering 10 sec)	300°C
Junction Temperature	150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only. Functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions may affect device reliability. Ambient temperature = 25°C, unless otherwise noted.

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS

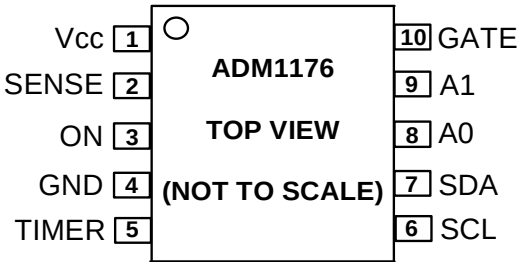

Figure 1. Pin Configurations

PIN FUNCTIONAL DESCRIPTIONS

Table 3.

Pin No.	Name	Description
1	VCC	Positive supply input pin. The operating supply voltage range is between 3.15 V to 14 V. An undervoltage lockout (UVLO) circuit resets the ADM1176 when a low supply voltage is detected.
2	SENSE	Current sense input pin. A sense resistor between the VCC and SENSE pins sets the analog current limit. The hotswap operation of the ADM1176 controls the external FET gate to maintain the (V_{VCC}-V_{SENSE}) voltage at 100 mV or below.
3	ON	Undervoltage input pin. Active high pin. An internal ON comparator has a trip threshold of 1.3 V and the output of this comparator is used as an enable for the hotswap operation. With an external resistor divider from VCC to GND, this pin can be used to enable the hotswap operation one a specific voltage on VCC, giving an undervoltage function.
4	GND	Chip Ground Pin
5	TIMER	Timer pin. An external capacitor CTIMER sets a 270 ms/µF initial timing cycle delay and a 21.7 ms/µF fault delay. The GATE pin turns off whenever the TIMER pin is pulled beyond the upper threshold. An overvoltage detection with an external zener can be used to force this pin high.
6	SCL	I^2C Clock Pin. Open-drain output requires an external resistive pull-up.
7	SDA	I^2C Data I/O Pin. Open-drain output requires an external resistive pull-up.
8	A0	I^2C Address Pin. This pin can be tied low, tied high, left floating or tied low through a resistor. Sixteen different I^2C address options are available depending on the external configuration of the A0 and A1 pins.
9	A1	I^2C Address Pin. This pin can be tied low, tied high, left floating or tied low through a resistor. Sixteen different I^2C address options are available depending on the external configuration of the A0 and A1 pins.
10	GATE	GATE Output Pin. This pin is the high side gate drive of an external N-channel FET. This pin is driven by the FET drive controller which utilises a charge pump to provide a 12 µA pull-up current to charge the FET gate pin. The FET drive controller regulates to a maximum load current (100 mV through the sense resistor) by modulating the GATE pin.

OVERVIEW OF THE HOTSWAP FUNCTION

When circuit boards are inserted into a live backplane, discharged supply bypass capacitors would draw large transient currents from the backplane power bus as they charge. Such transient currents can cause permanent damage to connector pins, and dips on the backplane supply which could reset other boards in the system. The ADM1176 is designed to turn a circuit board's supply voltage on and off in a controlled manner, allowing the circuit board to be safely inserted into or removed from a live backplane. The ADM1176 can reside either on the backplane or on the circuit board itself.

The ADM1176 controls the "inrush" current to a fixed maximum level by modulating the gate of an external N-channel FET placed between the live supply rail and the load. This "hotswap" function protects the card connectors and the FET itself from damage and also limits any problems which could be caused by the high current loads on the live supply rail.

The ADM1176 holds the GATE pin down (and thus the FET is held off) until a number of conditions are met. An undervoltage lockout circuit ensures that the device is being provided with an adequate input supply voltage. Once this has been successfully detected, the device goes through an initial timing cycle to provide a delay before it will attempt to hotswap. This delay ensures that the board is fully seated in the backplane before the board is powered up.

Once the initial timing cycle is complete, the hotswap function is switched on under control of the ON pin. When asserted high the hotswap operation starts.

The ADM1176 charges up the gate of the FET to turn on the load. It will continue to charge up the GATE pin until the linear current limit (set to 100 mV/R_{SENSE}) is reached. For some combinations of low load capacitance and high current limit, this limit may not be reached before the load is fully charged up. If current limit is reached, the ADM1176 will regulate the GATE pin to keep the current at this limit. For currents above the overcurrent fault timing threshold, nominally 100 mV/R_{SENSE}, the current fault is timed by sourcing a current out to the TIMER pin. If the load becomes fully charged before the fault current limit time is reached (when the TIMER pin reaches 1.3 V), the current will drop below the overcurrent fault timing threshold, the ADM1176 will then charge the GATE pin higher to fully enhance the FET for lowest R_{ON}, and the TIMER pin will be pulled down again.

If the fault current limit time is reached before the load drops below the current limit, a fault has been detected, and the hotswap operation is aborted by pulling down on the GATE pin to turn off the FET. The ADM1176-2 latches off at this point and will only attempt to hotswap again when the ON pin is de-asserted then asserted again. The ADM1176-1 will retry the hotswap operation indefinitely, keeping the FET in SOA by using the TIMER pin to time a cool-down period in between hotswap attempts. The current and voltage threshold combinations on the TIMER pin set the retry duty cycle to 3.8%.

The ADM1176 is designed to operate over a range of supplies from 3.15 V to 14 V.

UNDERVOLTAGE LOCKOUT

An internal undervoltage lockout (UVLO) circuit resets the ADM1176 if the VCC supply is too low for normal operation. The UVLO has a low-to-high threshold of 2.8 V, with 25 mV hysteresis. Above 2.8 V supply voltage, the ADM1176 will start the initial timing cycle.

ON FUNCTION

The ADM1176-1 has an active-high ON pin. The ON pin is the input to a comparator which has a low-to-high threshold of 1.3 V, an 80 mV hysteresis and a glitch filter of 3 µs. A low input on the ON pin turns off the hotswap operation by pulling the GATE pin to ground, turning off the external FET. The TIMER pin is also reset by turning on a pull-down current on this pin. A low-to-high transition on the ON pin starts the hotswap operation. A 10 kΩ pull-up resistor connecting the ON pin to the supply is recommended.

Alternatively, an external resistor divider at the ON pin can be used to program an undervoltage lockout value higher than the internal UVLO circuit, thereby setting a voltage level at the VCC supply where the hotswap operation is to start. An RC filter can be added at the ON pin to increase the delay time at card insertion if the initial timing cycle delay is insufficient.

TIMER FUNCTION

The TIMER pin handles several timing functions with an external capacitor, C_{TIMER}. There are two comparator thresholds: V_{TIMERH} (0.2 V) and V_{TIMERL} (1.3 V). The four timing current sources are a 5 µA and a 60 µA pull-up, and a 2 µA and a 100 µA pull-down. The 100 µA is a non-ideal current source approximating a 7 kΩ resistor below 0.4 V.

These current and voltage levels, together with the value of C_{TIMER} that the user chooses, determine the initial timing cycle time, the fault current limit time, and the hotswap retry duty cycle.

GATE AND TIMER FUNCTION DURING A HOTSWAP

During hot insertion of a board onto a live supply rail at VCC, the abrupt application of supply voltage charges the external FET drain/gate capacitance, which could cause an unwanted gate voltage spike. An internal circuit holds GATE low before the internal circuitry wakes up. This reduces the FET current surges substantially at insertion. The GATE pin is also held low during the initial timing cycle, and until the ON pin has been taken high to start the hotswap operation.

During hotswap operation the GATE pin is first pulled up by a 12 μA current source. If the current through the sense resistor reaches the overcurrent fault timing threshold, Voctim, then a pull-up current of 60 μA on the TIMER pin is turned on, and this pin starts charging up. At a slightly higher voltage in the sense resistor, the error amplifier servos the GATE pin to maintain a constant current to the load by controlling the voltage across the sense resistor to the linear current limit, V_{LIM}.

A normal hotswap will complete when the board supply capacitors near full charge and the current through the sense resistor drops, to eventually reach the level of the board load current. As soon as the current drops below the overcurrent fault timing threshold, the current into the TIMER pin will switch from being a 60 μA pull-up to a 100 μA pull-down. The ADM1176 will then drive the GATE voltage as high as it can to fully enhance the FET and reduce R_{ON} losses to a minimum.

A hotswap will fail if the load current fails to drop below the overcurrent fault timing threshold, V_{OCTIM}, before the TIMER pin has charged up to 1.3 V. In this case the GATE pin is then pulled down with a 2 mA current sink. The GATE pull-down will stay on until a hotswap retry starts, which can be forced by de-asserting then re-asserting the ON pin, or the device will retry automatically after a cool-down period, on the ADM1176-1.

The ADM1176 also features a method of protection from sudden load current surges, such as a low impedance fault, when the current seen across the sense resistor may go well beyond the linear current limit. If the fast overcurrent trip threshold, V_{OCFAST}, is exceeded, the 2 mA GATE pull-down is turned on immediately. This pulls the GATE voltage down quickly to enable the ADM1176 to limit the length of the current spike that gets through, and also to bring the current through the sense resistor back into linear regulation as quickly as possible. This protects the backplane supply from sustained overcurrent conditions, which may otherwise have caused problems with the backplane supply level dropping too low.

CALCULATING CURRENT LIMITS AND FAULT CURRENT LIMIT TIME

The nominal linear current limit is determined by a sense resistor connected between the VCC and SENSE pins as given by the equation below:

$$I_{LIMIT(NOM)} = V_{LIM(NOM)}/R_{SENSE} = 100\ \text{mV}/R_{SENSE} \quad (1)$$

The minimum linear fault current is given by Equation 2:

$$I_{LIMIT(MIN)} = V_{LIM(MIN)}/R_{SENSE(MAX)} = 90\ \text{mV}/R_{SENSE(MAX)} \quad (2)$$

The maximum linear fault current is given by Equation 3:

$$I_{LIMIT(MAX)} = V_{LIM(MAX)}/R_{SENSE(MIN)} = 110\ \text{mV}/R_{SENSE(MIN)} \quad (3)$$

The power rating of the sense resistor should be rated at the maximum linear fault current level.

The minimum overcurrent fault timing threshold current is given by

$$I_{OCTIM(MIN)} = V_{OCTIM(MIN)}/R_{SENSE(MAX)} = 85\ \text{mV}/R_{SENSE(MAX)} \quad (4)$$

The maximum fast overcurrent trip threshold current is given by

$$I_{OCFAST(MAX)} = V_{OCFAST(MAX)}/R_{SENSE(MIN)} = 115\ \text{mV}/R_{SENSE(MIN)} \quad (5)$$

The fault current limit time is the time that a device will spend timing an overcurrent fault, and is given by

$$t_{FAULT} \sim= 21.7 \times C_{TIMER}\ \text{ms}/\mu\text{F} \quad (6)$$

INITIAL TIMING CYCLE

When VCC is first connected to the backplane supply, there is an internal supply (time-point (1) in Figure 2) in the ADM1176 which needs to charge up. A very short time later (significantly less than 1 ms) the internal supply will be fully up and, since the undervoltage lockout voltage has been exceeded at VCC, the device will come out of reset. During this first short reset period the GATE pin is held down with a 25 mA pulldown current, and the TIMER pin is pulled down with a 100 μA current sink.

The ADM1176 then goes through an initial timing cycle. At point (2) the TIMER pin is pulled high with 5 μA. At time point (3), the TIMER reaches the V_{TIMERL} threshold and the first portion of the initial cycle ends. The 100 μA current source then pulls down the TIMER pin until it reaches 0.2 V at time point (4). The initial cycle delay (time point 2 to time point 4) is related to C_{TIMER} by equation:

$$t_{INITIAL} \sim= 270 \times C_{TIMER}\ \text{ms}/\mu\text{F} \quad (7)$$

When the initial timing cycle terminates, the device is ready to start a hotswap operation (assuming ON pin is asserted). In the example shown in Figure 2, the ON pin was asserted at the same time as VCC was applied, so the hotswap operation starts immediately after time-point (4). At this point the FET gate is charged up with a 12 µA current source. At timepoint (5) the threshold voltage of the FET is reached and the load current begins to flow. The FET is controlled to keep the sense voltage at 100 mV (this corresponds to a maximum load current level defined by the value of R_{SENSE}). At timepoint (6) V_{GATE} and V_{OUT} have reached their full potential and the load current has settled to its nominal level. Figure 3 illustrates the situation where the ON pin is asserted after V_{VCC} is applied.

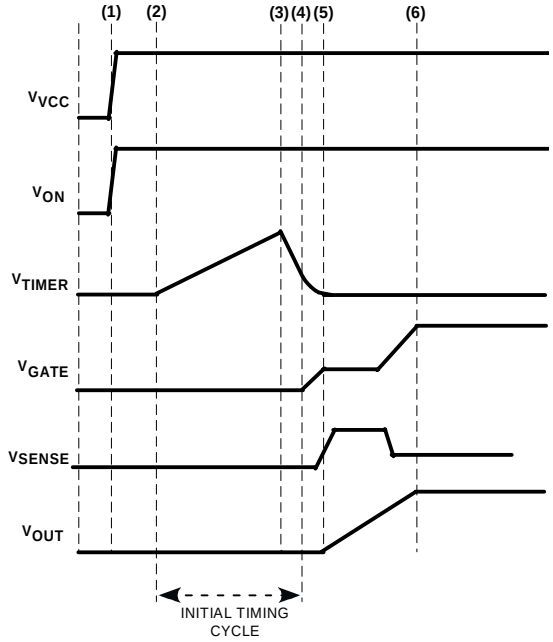

Figure 2. Start-up (ON asserts as power is applied)

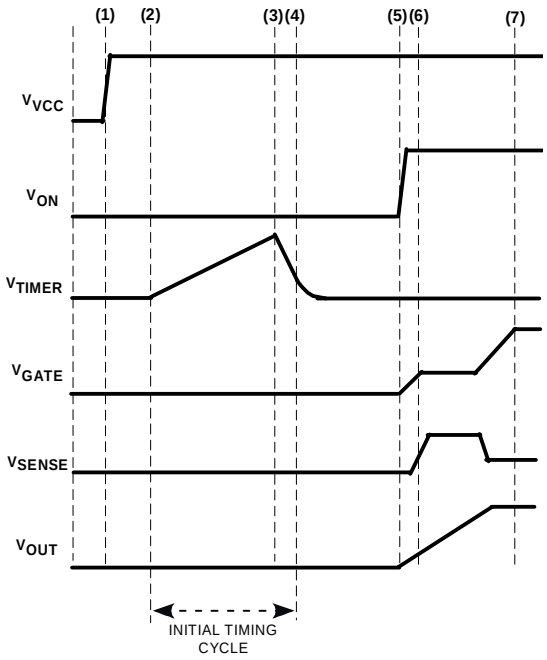

Figure 3. Start-up (ON asserts after power is applied)

HOTSWAP RETY ON ADM1176-1

With the ADM1176-1 the device will turn off the FET after an overcurrent fault, and will then use the TIMER pin to time a delay before automatically retrying to hotswap.

As with all ADM1176 devices, on overcurrent fault is timed by charging the TIMER cap with a 60 µA pull-up current, and when the TIMER pin reaches 1.3 V the fault current limit time has been reached and the GATE pin is pulled down. On the ADM1176-1, the TIMER pin is then pulled down with a 2 µA current sink. When the TIMER pin reaches 0.2 V, it will automatically restart the hotswap operation.

The cool down period is related to C_{TIMER} by equation:

$$t_{COOL} \sim = 550 \times C_{TIMER} \text{ ms/µF} \quad (8)$$

The retry duty cycle is thus given by

$$t_{FAULT}/(t_{COOL} + t_{FAULT}) \times 100\% = 3.8\% \quad (9)$$

VOLTAGE AND CURRENT READBACK

In addition to providing hot swap functionality, the ADM1176 also contains the components to allow voltage and current readback over an I²C bus. The voltage output of the current sense amplifier and the voltage on the VCC pin are fed into a 12-bit ADC via a multiplexer. The device can be instructed to convert voltage and/or current at any time during operation via an I²C command. When all conversions are complete the voltage and/or current values can be read out to 12-bit accuracy in two or three bytes.

SERIAL BUS INTERFACE

Control of the ADM1176 is carried out via the Inter-IC Bus (I²C). This interface is compatible with fastmode I²C (400 kHz max). The ADM1176 is connected to this bus as a slave device, under the control of a master device.

IDENTIFYING THE ADM1176 ON THE I²C BUS

The ADM1176 has a 7-bit serial bus slave address. When the device is powered up, it will do so with a default serial bus address. The three MSBs of the address are set to 100, the four LSBs are determined by the state of the A0 and A1 pins. There are sixteen different configurations available on the A0 and A1 pins which correspond to sixteen different I²C addresses for the four LSBs. These are explained in Table 4 below. This scheme allows sixteen ADM1176 devices to operation on a single I²C bus.

Table 4. Setting I²C Addresses via the A0 and A1 Pins

A0 Configuration	A1 Configuration	Address
Low state	Low state	0x80
Low state	Resistor to GND	0x88
Low state	Floating	0x90
Low state	High state	0x98
Resistor to GND	Low state	0x82
Resistor to GND	Resistor to GND	0x8A
Resistor to GND	Floating	0x92
Resistor to GND	High state	0x9A
Floating	Low state	0x84
Floating	Resistor to GND	0x8C
Floating	Floating	0x94
Floating	High state	0x9C
High state	Low state	0x86
High state	Resistor to GND	0x8E
High state	Floating	0x96
High state	High state	0x9E

GENERAL I²C TIMING

and Figure 5 show timing diagrams for general read and write operations using the I²C. The I²C specification defines specific conditions for different types of read and write operation, which are discussed later. The general I²C protocol operates as follows:

1. The master initiates data transfer by establishing a START condition, defined as a high to low transition on the serial data line SDA while the serial clock line SCL remains high. This indicates that a data stream will follow. All slave peripherals connected to the serial bus respond to the START condition, and shift in the next 8 bits, consisting of a 7-bit slave address (MSB first) plus a R/W bit, which determines the direction of the data transfer, i.e. whether data will be written to or read from the slave device (0 = write, 1 = read).

   The peripheral whose address corresponds to the transmitted address responds by pulling the data line low during the low period before the ninth clock pulse, known as the acknowledge bit, and holding it low during the high period of this clock pulse. All other devices on the bus now remain idle while the selected device waits for data to be read from or written to it. If the R/W bit is a 0, the master will write to the slave device. If the R/W bit is a 1, the master will read from the slave device.

2. Data is sent over the serial bus in sequences of nine clock pulses, eight bits of data followed by an acknowledge bit from the slave device. Data transitions on the data line must occur during the low period of the clock signal and remain stable during the high period, as a low to high transition when the clock is high may be interpreted as a STOP signal.

   If the operation is a write operation, the first data byte after the slave address is a command byte. This tells the slave device what to expect next. It may be an instruction such as telling the slave device to expect a block write, or it may simply be a register address that tells the slave where subsequent data is to be written.

   Since data can flow in only one direction as defined by the R/W bit, it is not possible to send a command to a slave device during a read operation. Before doing a read operation, it may first be necessary to do a write operation to tell the slave what sort of read operation to expect and/or the address from which data is to be read.

3. When all data bytes have been read or written, stop conditions are established. In WRITE mode, the master will pull the data line high during the 10th clock pulse to assert a STOP condition. In READ mode, the master device will release the SDA line during the low period before the ninth clock pulse, but the slave device will not pull it low. This is known as No Acknowledge. The master will then take the data line low during the low period before the 10th clock pulse, then high during the 10th clock pulse to assert a STOP condition.

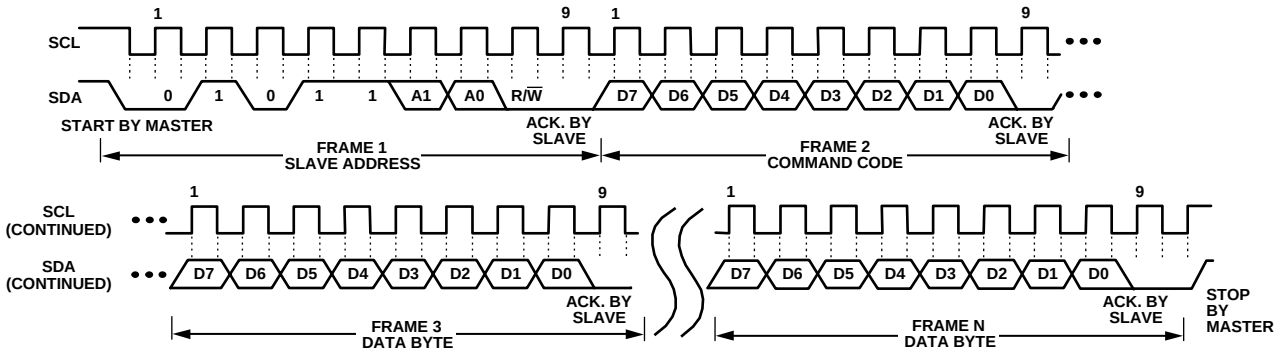

Figure 4. General I²C Write Timing Diagram

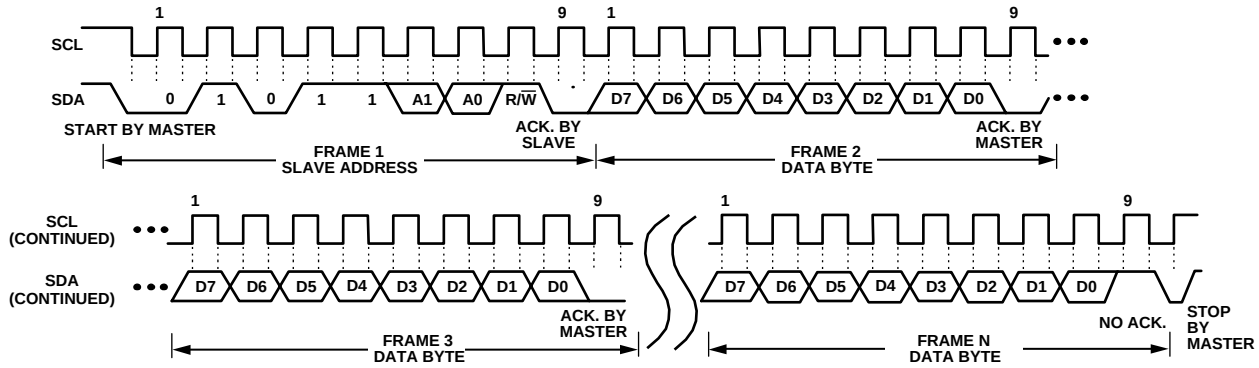

Figure 5. General I²C Read Timing Diagram

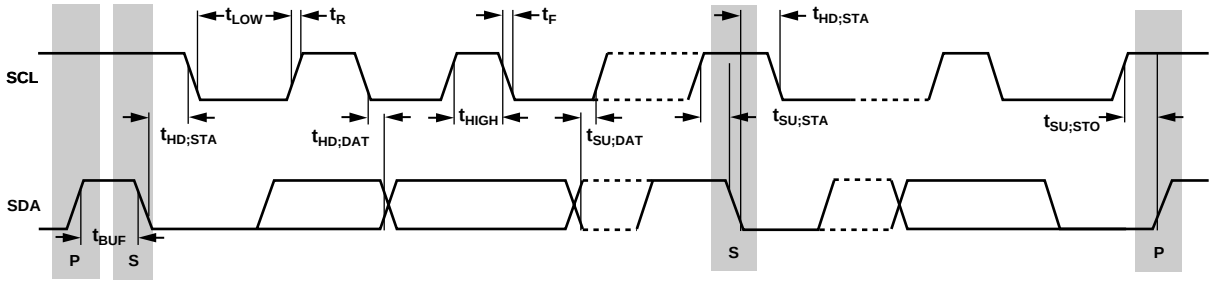

Figure 6. Serial Bus Timing Diagram

WRITE AND READ OPERATIONS

The I²C specification defines several protocols for different types of read and write operations. The ones used in the ADM1176 are discussed below. The following abbreviations are used in the diagrams:

Table 5. I²C abbreviations

S	START
P	STOP
R	READ
W	WRITE
A	ACKNOWLEDGE
N	NO ACKNOWLEDGE

QUICK COMMAND

This operation allows the master check if the slave is present on the bus. This entails the following:

1. The master device asserts a start condition on SDA.
2. The master sends the 7-bit slave address followed by the write bit (low).
3. The addressed slave device asserts ACK on SDA.

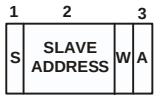

Figure 7. Quick Command

WRITE COMMAND BYTE

In this operation the master device sends a command byte to the slave device, as follows:

1. The master device asserts a start condition on SDA.
2. The master sends the 7-bit slave address followed by the write bit (low).
3. The addressed slave device asserts ACK on SDA.
4. The master sends the command byte. The command byte is identified by an MSB =0. (An MSB =1 indicates an Extended Register Write. See next section.)
5. The slave asserts ACK on SDA.
6. The master asserts a STOP condition on SDA to end the transaction.

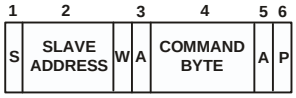

Figure 8. Command Byte Write

The seven LSBs of the command byte are used to configure and control the ADM1176. Details of the function of each bit are provided in Table 6.

Table 6. Command Byte Operations

Bit	Default	Name	Function
C0	0	V_CONT	Set to convert voltage continuously. If readback is attempted before the first conversion is complete, the ADM1176 will ACK and return all zeros in the returned data.
C1	0	V_ONCE	Set to convert voltage once. Self-clears. I²C will NACK an attempted read until ADC conversion is complete.
C2	0	I_CONT	Set to convert voltage continuously. If readback is attempted before the first conversion is complete, the ADM1176 will ACK and return all zeros in the returned data.
C3	0	I_ONCE	Set to convert current once. Self-clears. I²C will NACK an attempted read until ADC conversion is complete.
C4	0	VRANGE	Selects different internal attenuation resistor networks for voltage readback. A "0" in C4 selects a 14:1 voltage divider. A "1" in C4 selects a 7:2 voltage divider. With an ADC full-scale of 1.902 V, the voltage at the VCC pin for an ADC full-scale result is 26.63 V for VRANGE = 0 and 6.66 V for VRANGE = 1.
C5	0	N/A	Unused
C6	0	STATUS_RD	Status Read. When this bit is set the data byte read back from the ADM1176 will be the STATUS byte. This contains the status of the device alerts. See Table14 for full details of the status byte.

WRITE EXTENDED BYTE

In this operation the master device writes to one of the three extended registers of the slave device, as follows:

1. The master device asserts a start condition on SDA.
2. The master sends the 7-bit slave address followed by the write bit (low).
3. The addressed slave device asserts ACK on SDA.
4. The master sends the register address byte. The MSB of this byte is set to 1 to indicate an extended register write. The two LSBs indicate which of the three extended registers will be written to (see Table 7). All other bits should be set to 0.
5. The slave asserts ACK on SDA.
6. The master sends the command byte. The command byte is identified by an MSB = 0. (An MSB = 1 indicates an Extended Register Write. See next section.)
7. The slave asserts ACK on SDA.
8. The master asserts a STOP condition on SDA to end the transaction.

Figure 9. Command Byte Write

Table 8, Table 9, and give details of each extended register.

Table 7. Extended Register Addresses

A6	A5	A4	A3	A2	A1	A0	Extended Register
0	0	0	0	0	0	1	ALERT_EN
0	0	0	0	0	1	0	ALERT_TH
0	0	0	0	0	1	1	CONTROL

Table 8. ALERT_EN Register Operations

Bit	Default	Name	Function
0	0	EN_ADC_OC1	Enabled if a single ADC conversion on the I channel has exceeded the threshold set in the ALERT_TH register
1	0	EN_ADC_OC4	Enabled if four consecutive ADC conversions on the I channel have exceeded the threshold set in the ALERT_TH register
2	1	EN_HS_ALERT	Enabled if the hotswap has either latched off, or entered a cool down cycle, because of an overcurrent event
3	0	EN_OFF_ALERT	Enable an ALERT if the HS operation is turned off by a transition which de-asserts the ON pin, or by an operation which writes the SWOFF bit high.
4	0	CLEAR	Clears the ON_ALERT, HS_ALERT and ADC_ALERT status bits in the STATUS register. These may immediately reset if the source of the alert has not been cleared, or disabled with the other bits in this register. This bit self-clears to 0 after the STATUS register bits have been cleared.

Table 9. ALERT_TH Register Operations

Bit	Default	Function
7:0	FF	The ALERT_TH register sets the current level at which an alert will occur. Defaults to ADC full-scale. ALERT_TH 8-bit number corresponds to the top 8-bits of the current channel data.

Table 10. CONTROL Register Operations

Bit	Default	Name	Function
0	0	SWOFF	Force hotswap off. Equivalent to de-asserting the ON pin.

READ VOLTAGE AND/OR CURRENT DATA BYTES

The ADM1176 can be set up to provide information in three different ways (see Write Command Byte section above). Depending on how the device is configured the following data can be read out of the device after a conversion (or conversions):

1. Voltage and Current Readback.

The ADM1176 will digitize both voltage and current. Three bytes will be read out of the device in the following format:

Table 11.

Byte	Contents	B7	B6	B5	B4	B3	B2	B1	B0
1	Voltage MSBs	V11	V10	V9	V8	V7	V6	V5	V4
2	Current MSBs	I11	I10	I9	I8	I7	I6	I5	I4
3	LSBs	V3	V2	V1	V0	I3	I2	I1	I0

2. Voltage Readback.

The ADM1176 will digitize voltage only. Two bytes will be read out of the device in the following format:

Table 12.

Byte	Contents	B7	B6	B5	B4	B3	B2	B1	B0
1	Voltage MSBs	V11	V10	V9	V8	V7	V6	V5	V4
2	Voltage LSBs	V3	V2	V1	V0	0	0	0	0

3. Current Readback.

The ADM1176 will digitize current only. Two bytes will be read out of the device in the following format:

Table 13.

Byte	Contents	B7	B6	B5	B4	B3	B2	B1	B0
1	Current MSBs	I11	I10	I9	I8	I7	I6	I5	I4
2	Current LSBs	I3	I2	I1	I0	0	0	0	0

The following series of events occur when the master receives three bytes (voltage and current data) from the slave device:

1. The master device asserts a START condition on SDA.
2. The master sends the 7-bit slave address followed by the read bit (high).
3. The addressed slave device asserts ACK on SDA.
4. The master receives the first data byte.
5. The master asserts ACK on SDA.
6. The master receives the second data byte.
7. The master asserts ACK on SDA.
8. The master receives the third data byte.
9. The master asserts NO ACK on SDA.
10. The master asserts a STOP condition on SDA and the transaction ends.

For the cases where the master is reading voltage only or current only, only two data bytes will be read and events 7 and 8 above will not be required.

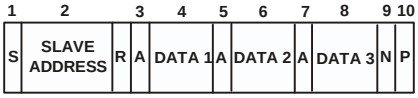

Figure 10. Three Byte Read fromADM1176

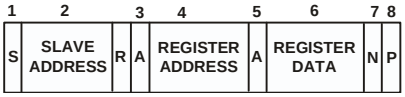

Figure 11. Two Byte Read fromADM1176

READ STATUS REGISTER

A single register of status data can also be read from the ADM1176.

1. The master device asserts a START condition on SDA.
2. The master sends the 7-bit slave address followed by the read bit (high).
3. The addressed slave device asserts ACK on SDA.
4. The master receives the status byte.
5. The master asserts ACK on SDA.

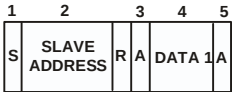

Figure 12. Status Read fromADM1176

Table 14 shows the ADM1176 status registers in detail. Note that bits 1, 3 and 5 are cleared by writing to bit 4 of the ALERT_EN register (CLEAR).

Table 14. Status Byte Operations

Bit	Name	Function
0	ADC_OC	An ADC based overcurrent comparison has been detected on the last 3 conversions
1	ADC_ALERT	An ADC based overcurrent trip has happened, which has caused the ALERT. Cleared by writing to bit 4 of the ALERT_EN register.
2	HS_OC	The hotswap is off due to an analog overcurrent event. On parts which latch off, this will be the same as the HS_ALERT status bit (if EN_HS_ALERT=1). On the retry parts this will indicate the current state—a 0 could indicate that the data was read during a period when the device is retrying, or that it has successfully hotswapped by retrying after at least one overcurrent timeout.
3	HS_ALERT	The hotswapper has failed since the last time this was reset. Cleared by writing to bit 4 of the ALERT_EN register.
4	OFF_STATUS	The state of the ON pin. Set to 1 if the input pin is de-asserted. Can also be set to 1 by writing to the SWOFF bit of the CONTROL register.
5	OFF_ALERT	An alert has been caused either by the ON pin or the SWOFF bit. Cleared by writing to bit 4 of the ALERT_EN register.

KELVIN SENSE RESISTOR CONNECTION

When using a low-value sense resistor for high current measurement the problem of parasitic series resistance can arise. The lead resistance can be a substantial fraction of the rated resistance making the total resistance a function of lead length. This problem can be avoided by using a Kelvin sense connection. This type of connection separates the current path through the resistor and the voltage drop across the resistor. Figure 13 below shows the correct way to connect the sense resistor between the VCC and SENSE pins of the ADM1176.

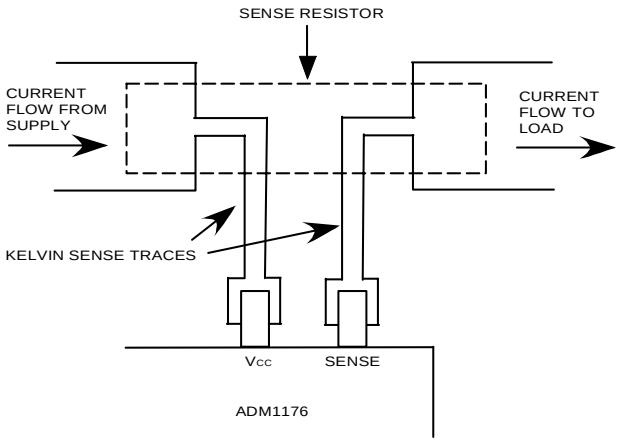

Figure 13. Kelvin Sense Connections

OUTLINE DIMENSIONS

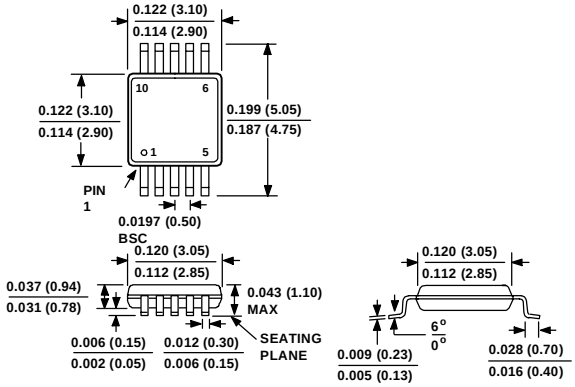

Figure 14. 10-Lead MSOP Package
(RM-10)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Hotswap Retry Option	Brand	Temperature Range	Package Description	Package Outline
ADM1176-1ARMZ-R7	Automatic Retry Version	M5U	–40°C to +85°C	MSOP-10	RM-10
ADM1176-2ARMZ-R7	Latched Off Version	M5V	–40°C to +85°C	MSOP-10	RM-10

[1] Z = Pb-free part.