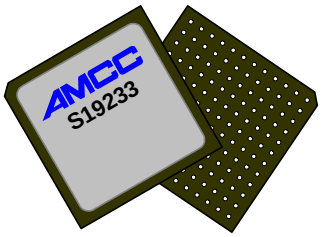


S19233

10 G Ethernet/Fibre Channel/SONET/SDH Dual CDR

Features

- Complies with ITU-T specifications, 50 mUI_{pp} max. jitter generation (50 KHz - 80 MHz)
- Complies with XFP MSA Specifications
- 25 mUI_{pp} Jitter Generation
- CML serial input sensitivity at 5 mV_{pp} Diff.
- Dual CDR - 9.95 to 11.32 Gbps operation
- Superior Crosstalk Isolation
- Electronic Dispersion Compensation (EDC) Optimized for 0 to 100 Km SMF with 2 dB dispersion penalty
- Low power EDC ideal for Power Level 2 XFP modules
- Suitable for low Optical Signal to Noise Ratio (OSNR) environments
- Automatic Threshold Adjust
- External threshold & Phase Adjust
- AGC embedded equalizer
- LOS Function - Compliant to GR-253
- Integrated equalizer that support over 24" FR-4 on Transmitter Electrical Side
- Transmitter (Optical Side) - CDR
- Lock detect indication
- 650 mW Typical Power
- -40 to 85°C operation
- CMOS 0.13 Micron Technology
- 1.8 and 3,3 Volt Power Supply
- 6 x 6 mm^2 PBGA package with RoHS compliant lead free option
- ESD - 1500 V, 500 V High Speed Inputs

Applications

- 10 G Fibre Channel and Ethernet Designs
- 10 GbE with FEC
- 10 G SONET/SDH/FEC Designs
- SONET/SDH Test Equipment
- SONET/SDH/FEC DWDM Equipment
- XFP MSA Modules

Description

The S19233 is a fully integrated low power dual CDR device with Electronic Dispersion Compensation (EDC). It is suitable for use in 10 GbE/10G FC/SONET/SDH PMD modules, such as the XFP MSA modules. This device can be used to compensate channel impairments caused by either single mode fiber up to 120 km or FR-4 copper medium over 24". Integrated in this device on the receive optical side, an AGC amplifier with offset cancellation circuitry, EDC/Equalization with control circuitry, and CDR. On the transmit electrical side the S19233 also has an equalization circuit, and CDR that reshapes the data after up to 24" of transmission over copper on FR-4 PWB material. The low-jitter CML interfaces guarantees compliance with the bit error rate requirements of the Telcordia and ITU-T standards. The S19233 is packaged in a 6 x 6 mm^2 PBGA, offering designers a small package outline.

Value Proposition - Design multiple XFP modules ranging from 2 km to 120 km link with one footprint. The S19233 is pin compatible to the lower cost 10G Dual CDR S19256 (no EDC).

S19256: 2 km-30 km;

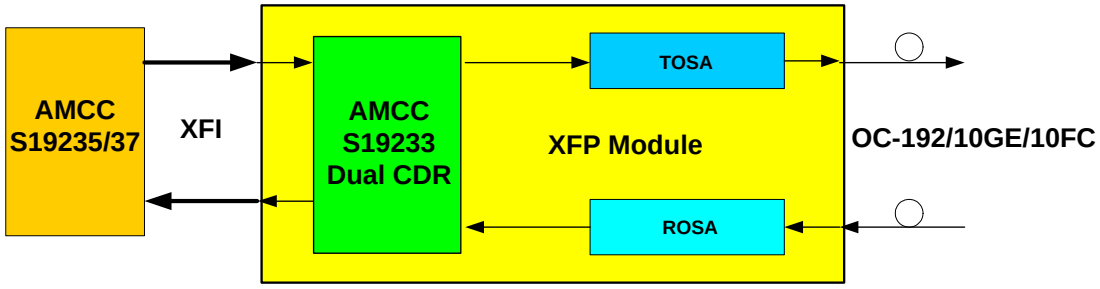
S19233: 2 km-120 km

Overview

The S19233 can be used to implement the front end of SONET/SDH/FEC/10GbE/FC/G.709 equipment which consists primarily of the serial transmit interface and the serial receive interface. The system timing circuitry consists of a high-speed phase detector, clock and data recovery unit and equalization circuitry. The device utilizes on-chip clock recovery PLL components that allow the use of a slower external clock reference, 155.52 MHz (or equivalent FEC/10GbE/10 Gbps FC rate), in support of existing system clocking schemes.

The EDC function is embedded in the optical receive side. It provides control to compensate chromatic dispersion in different fiber links. On the transmitter side, an equalizer is integrated in the receive front end to reshape the data after transmission over FR-4. This enables low bit error rate and transmission over longer trace length.

The low-jitter, 1-bit, CML interfaces guarantee compliance with the bit-error rate requirements of the Telcordia and ITU-T standards. The 10 Gbps serial electrical interface specifications are compliant with the XFI as specified in the XFP MSA module specification. The high speed serial input and output can be connected to the AMCC SerDes (S19235 or S19237) across 60 cm (24") of improved FR-4 material or across 40 cm of standard FR-4 with one connector.



System Block Diagram with the S19233

S19233

AMCC Suggested Interface Devices

S19235	SFI4 Phase 1 SONET/SDH STS-192/10 Gig Ethernet CMOS Transceiver with ISI Compensation
S19237	SFI4 Phase 1 SONET/SDH STS-192/10 Gig Ethernet CMOS Transceiver with ISI Compensation

Transmitter Side Operations

- 1-bit serial data input
- Equalization to compensate for FR-4
- Threshold and Offset cancellation adjust
- Clock and Data recovery
- Data retime

Serial data output

- Receiver Side Operations
- Serial input with AGC (Equalization)
- 10 mV_{pp} Differential Sensitivity with threshold adjust
- Loss of signal detection
- Clock and Data recovery
- Serial data output

Common Operations

- Optical and Electrical Loopbacks
- Power Down CDR
- Squelch
- Polarity Invert

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