



FEATURES

Very low offset voltage: 1 mV max

Bias current: 10 pA max

Small packaging, TSOT-23 lead-free

±5 V to ±15 V operation

High slew rate: 20 V/μs

Low voltage noise: 15 nV/√Hz

Unity gain stable

Wide bandwidth: 6 MHz

APPLICATIONS

Reference gain/buffers

Level shift/driving

Active filters

Power line monitoring/control

Current/voltage sense or monitoring

Data acquisition

Sample-and-hold circuits

Integrators

GENERAL DESCRIPTION

The AD4004 is a JFET input operational amplifier featuring precision, very low bias current, and low power in a tiny package at a very attractive price. Combining high input impedance, low input bias current, wide bandwidth, and fast slew rate, the AD4000 is an ideal amplifier for driving A/D inputs and buffering D/A converter outputs.

PIN CONFIGURATIONS

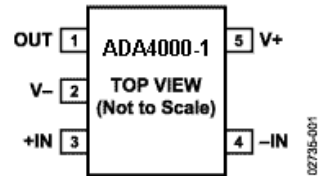


Figure 1. 5-Lead TSOT (UJ-5)

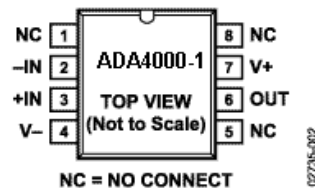


Figure 2. 8-Lead SOIC (R-8)

Additional applications for the AD4004 include electronic instruments; ATE amplification, buffering, and integrator circuits;

Instrumentation quality photodiode amplification; fast precision filters (including PLL filters), utility functions like reference buffering, level shifting, control I/O interface, power supply control and monitoring functions.

Rev. PrA

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REVISION HISTORY

10/05—Revision PrA: Preliminary Version

SPECIFICATIONS

ELECTRICAL SPECIFICATIONS

$V_S = \pm 5.0\text{ V}$, $V_{CM} = 0\text{ V}$, $T_A = +25^\circ\text{C}$, unless otherwise specified.

Table 1.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}			0.1	1.0	mV
Input Bias Current	I_B			5	10	pA
		$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$				pA
Input Offset Current	I_{OS}			5		pA
		$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$				pA
Input Voltage Range			-2.5		3.5	V
Common-Mode Rejection Ratio	CMRR	$-1.5\text{ V} \leq V_{CM} \leq +3.5\text{ V}$ $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		76		dB
Open Loop Gain (Note 1)	A_{VO}	$R_L = 2\text{ k}\Omega$, $V_O = \pm 2.5\text{ V}$ $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		114		dB
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		10		$\mu\text{V}/^\circ\text{C}$
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	$R_L = 2\text{ k}\Omega$ to ground $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		4.0		V
				3.7		V
Output Voltage Low	V_{OL}	$R_L = 2\text{ k}\Omega$ to ground $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		-3.35		V
				-3.7		V
Short Circuit Limit	I_{SC}			28		mA
		$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$				mA
Output Current	I_O			± 10		mA
		$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$				mA
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	$V_S = \pm 5.0\text{ V}$ to $\pm 15.0\text{ V}$ $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		80		dB
						dB
Supply Current/Amplifier	I_{SY}	$V_O = 0\text{ V}$ $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		1.1		mA
						mA
DYNAMIC PERFORMANCE						
Slew Rate	SR	$V_i = 10\text{ V}$, $R_L = 2\text{ k}\Omega$, $C_L = 100\text{ pF}$		20		$\text{V}/\mu\text{s}$
Gain Bandwidth Product	GBP			6		MHz
NOISE PERFORMANCE						
Voltage Noise	$e_{n\text{ p-p}}$	0.1 Hz to 10 Hz		1.2		$\mu\text{Vp-p}$
Voltage Noise Density	e_n	$f = 1\text{ kHz}$		15		$\text{nV}/\sqrt{\text{Hz}}$
Current Noise Density	i_n	$f = 1\text{ kHz}$		0.01		$\text{pA}/\sqrt{\text{Hz}}$

$V_S = \pm 15\text{ V}$, $V_{CM} = 0\text{ V}$, $T_A = +25^\circ\text{C}$, unless otherwise specified.

Table 2.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}			0.1	1.0	mV
Input Bias Current	I_B			5	10	pA
Input Offset Current	I_{OS}	$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		5		pA
Input Voltage Range		$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$				pA
Common-Mode Rejection Ratio	CMRR	$-11\text{ V} \leq V_{CM} \leq +15\text{ V}$ $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	-11	80	+15	V dB
Open Loop Gain	A_{VO}	$R_L = 2\text{ k}\Omega$, $V_O = \pm 10\text{ V}$ $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		114		dB
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		10		dB $\mu\text{V}/^\circ\text{C}$
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	$R_L = 2\text{ k}\Omega$ to ground $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		13.7		V
Output Voltage Low	V_{OL}	$R_L = 2\text{ k}\Omega$ to ground $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		13.5		V
Short Circuit Limit	I_{SC}	$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		-13.3		V
Output Current	I_O	$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		28		mA
		$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$				mA
		$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$				mA
		$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$				mA
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	$V_S = \pm 4.0\text{ V}$ to $\pm 18.0\text{ V}$ $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		80		dB
Supply Current/Amplifier	I_{SY}	$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		1.2		dB mA mA
DYNAMIC PERFORMANCE						
Slew Rate	SR	$V_i = 10\text{ V}$, $R_L = 2\text{ k}\Omega$, $C_L = 100\text{ pF}$		20		V/ μs
Gain Bandwidth Product	GBP			6		MHz
NOISE PERFORMANCE						
Voltage Noise	$e_{n\text{ p-p}}$	0.1 to 10 Hz		1.2		$\mu\text{V p-p}$
Voltage Noise Density	e_n	$f = 1\text{ kHz}$		15		nV/ $\sqrt{\text{Hz}}$
Current Noise Density	i_n	$f = 1\text{ kHz}$		0.01		pA/ $\sqrt{\text{Hz}}$

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Supply Voltage	$\pm 18\text{ V}/+36\text{ V}$
Input Voltage	$\pm V$ supply
Differential Input Voltage ¹	$\pm V$ supply
Output Short-Circuit Duration to Gnd	Indefinite
Storage Temperature Range UJZ, RZ Packages	-65°C to $+150^{\circ}\text{C}$
Operating Temperature Range ADA4000-1	-40°C to $+125^{\circ}\text{C}$
Junction Temperature Range UJZ, RZ Packages	-65°C to $+150^{\circ}\text{C}$
Lead Temperature (Soldering, 10 sec)	$+300^{\circ}\text{C}$

¹ Differential input voltage is limited to ± 5.0 volts or the supply voltage, whichever is less.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, for a device in socket for PDIP packages; a device soldered in a circuit board for SOIC and TSSOP packages.

Table 4. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
5-Pin TSOT (UJZ)			$^{\circ}\text{C}/\text{W}$
8-Pin SOIC (RZ)	158	43	$^{\circ}\text{C}/\text{W}$

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
ADA4000-1AUJZ ¹	-40°C to +125°C	5-Pin TSOT	UJZ-5
ADA4000-1ARZ ¹	-40°C to +125°C	8-Pin SOIC	RZ-8

¹ Z = Pb-free part.

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