GENERAL SEMICONDUCTOR®

GF6968AD

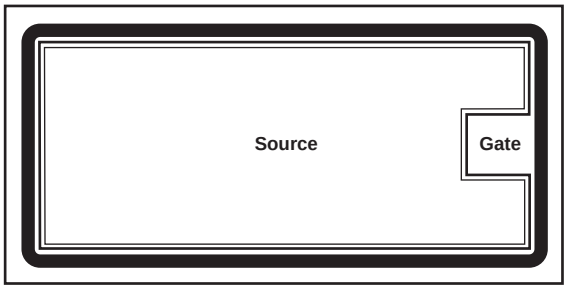
N-Channel Enhancement-Mode MOSFET Die

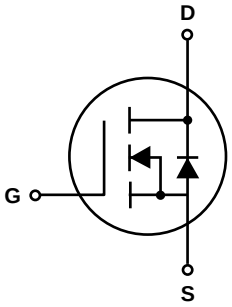
V_{DS} 20V $R_{DS(ON)}$ 30mΩ I_D 6.0A

TRENCH GENFET™

New Product

Chip Geometry





Physical Characteristics

- Die size : 1800 x 1120µm (70.9 x 44.1 mils)
- Metalization:
  Top: Al/Si/Cu
  Back: Ti/Ni/Ag
- Metal Thickness:
  Top: 3.0µm
  Back: 1.4µm
- Die thickness: 9 - 13 mils
- Bonding Area:
  Source: Full metalized surface of source region
  Gate: 181 x 181µm
- Recommended Wire Bonding:
  Source: 2 mil ∅ Au wire (3 or more wires preferred)
  Gate: 2 mil ∅ Au wire

Note: More source wires can further improve performance

Features

- Advanced Trench Process Technology
- High Density Cell Design for Ultra Low On-Resistance
- Fast Switching
- High temperature soldering in accordance with CECC802/Reflow guaranteed
- Logic Level
- Ideal for Li ion battery pack applications

Maximum Ratings and Thermal Characteristics (T_A = 25°C unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	20	V
Gate-Source Voltage		V_{GS}	±10	
Continuous Drain Current T_J = 150°C(1)	T_A = 25°C T_A = 70°C	I_D	6.0 4.8	A
Pulsed Drain Current		I_{DM}	20	
Continuous Source Current (Diode Conduction)(1)		I_S	1.7	
Maximum Power Dissipation(1)	T_A = 25°C T_A = 70°C	P_D	2.0 1.3	W
Operating Junction and Storage Temperature Range		T_J, T_{stg}	–55 to 150	°C
Maximum Junction-to-Ambient(1) Thermal Resistance		$R_{\theta JA}$	62.5	°C/W

Note: Maximum ratings are based on die packaged in a SO-8 Dual package. Actual rating can increase (or decrease), depending on actual assembly method used

5/23/01

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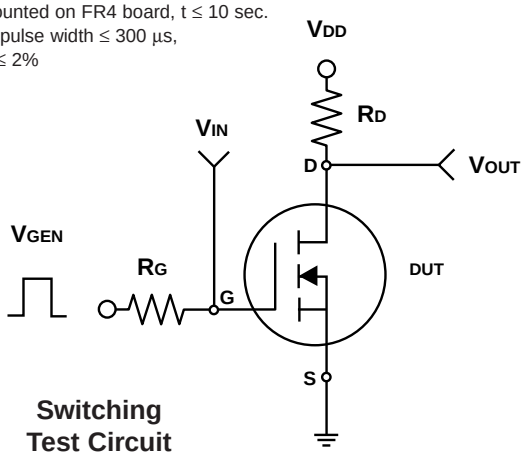
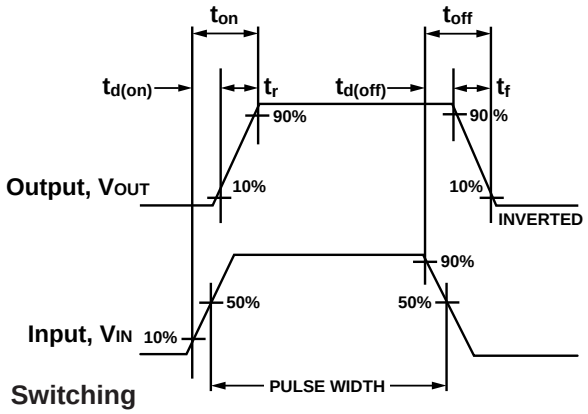
Electrical Characteristics (T_J = 25°C unless otherwise noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS} = 0V, I_D = 250µA	20	–	–	V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250µA	0.5	–	–	V
Gate-Body Leakage	I_{GSS}	V_{DS} = 0V, V_{GS} = ±8V	–	–	±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 20V, V_{GS} = 0V	–	–	1	µA
		V_{DS}=20V, V_{GS}=0V, T_J=55°C	–	–	5	
On-State Drain Current(2)	$I_{D(on)}$	V_{DS} ≥ 5V, V_{GS} = 4.5V	20	–	–	A
Drain-Source On-State Resistance(2)	$R_{DS(on)}$	V_{GS} = 4.5V, I_D = 6A	–	22	30	mΩ
		V_{GS} = 2.5V, I_D = 5.2A	–	28	40	
Forward Transconductance(2)	g_{fs}	V_{DS} = 10V, I_D = 6A	–	24	–	S
Dynamic						
Total Gate Charge	Q_g	V_{DS} = 10V, V_{GS} = 4.5V I_D = 6A	–	13	40	nC
Gate-Source Charge	Q_{gs}		–	2.2	–	
Gate-Drain Charge	Q_{gd}		–	3	–	
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 10V, R_L = 10Ω I_D ≈ 1A, V_{GEN} = 4.5V R_G = 6Ω	–	11	60	ns
Rise Time	t_r		–	15	140	
Turn-Off Delay Time	$t_{d(off)}$		–	43	140	
Fall Time	t_f		–	22	60	
Input Capacitance	C_{iss}	V_{GS} = 0V V_{DS} = 10V f = 1.0MHz	–	1240	–	pF
Output Capacitance	C_{oss}		–	200	–	
Reverse Transfer Capacitance	C_{rss}		–	120	–	
Source-Drain Diode						
Diode Forward Voltage(2)	V_{SD}	I_S = 1.7A, V_{GS} = 0V	–	0.7	1.3	V
Source-Drain Reverse Recovery Time	t_{rr}	I_F = 1.7A, di/dt = 100A/µs	–	–	100	ns

Notes:
(1) Surface mounted on FR4 board, t ≤ 10 sec.
(2) Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2%



Switching Test Circuit



Switching Waveforms

N-Channel Enhancement-Mode MOSFET Die

Ratings and Characteristic Curves (TA = 25°C unless otherwise noted)

Fig. 1 – Output Characteristics

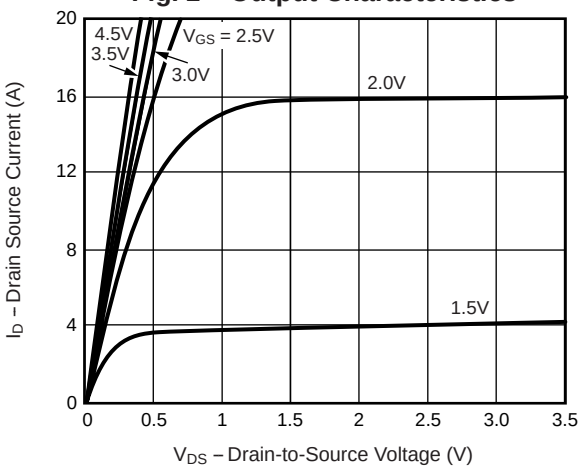


Fig. 2 – Transfer Characteristics

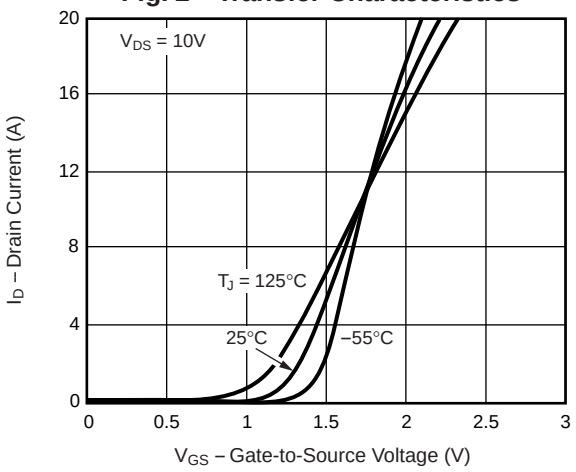


Fig. 3 – Threshold Voltage vs. Temperature

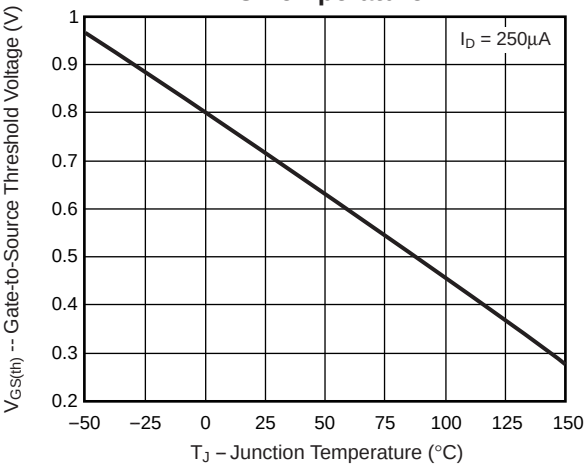


Fig. 4 – On-Resistance vs. Drain Current

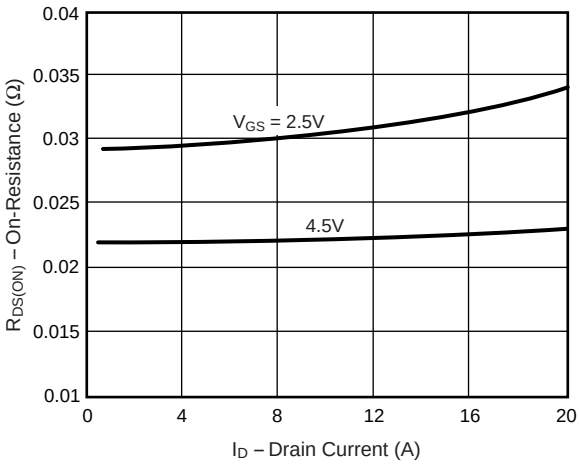
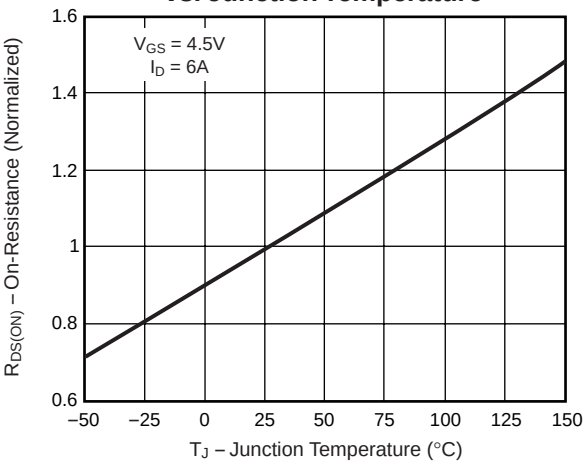


Fig. 5 – On-Resistance vs. Junction Temperature



N-Channel Enhancement-Mode MOSFET Die

Ratings and Characteristic Curves (TA = 25°C unless otherwise noted)

Fig. 6 – On-Resistance vs. Gate-to-Source Voltage

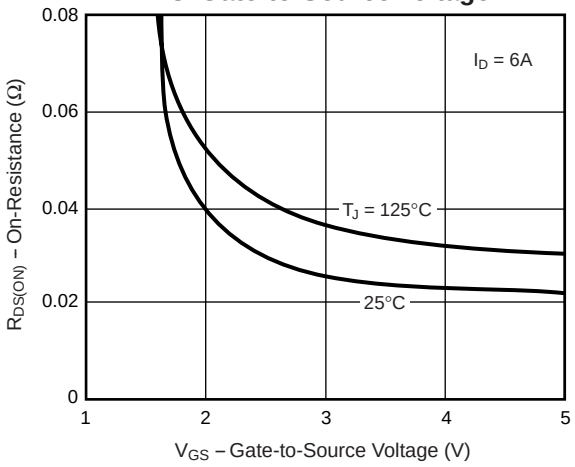


Fig. 7 – Gate Charge

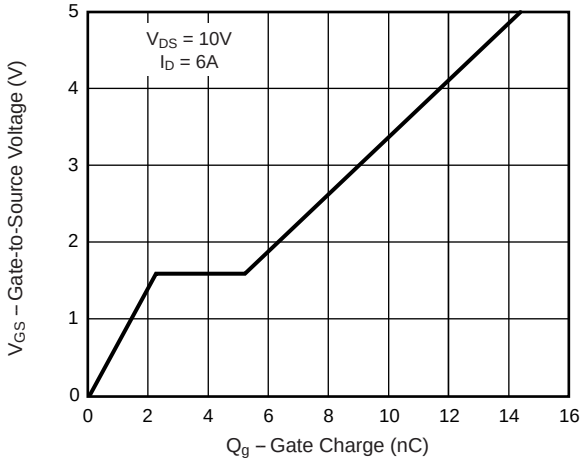


Fig. 8 – Capacitance

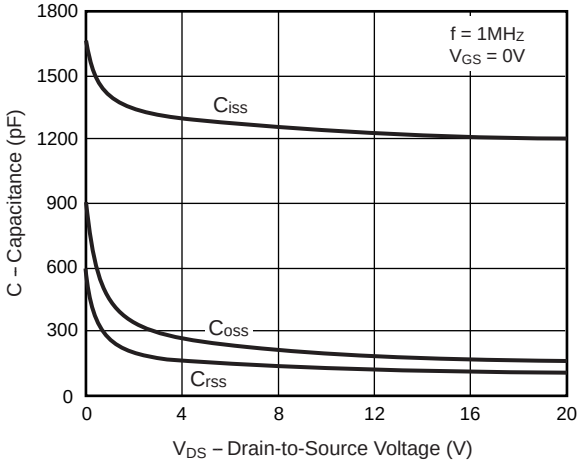
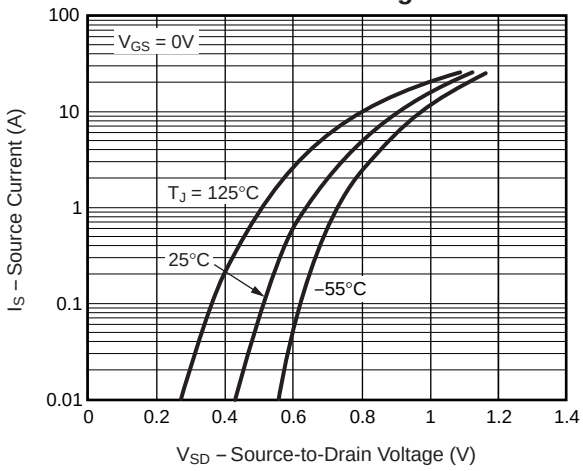


Fig. 9 – Source-Drain Diode Forward Voltage



N-Channel Enhancement-Mode MOSFET Die

Ratings and Characteristic Curves (TA = 25°C unless otherwise noted)

Fig. 10 – Breakdown Voltage vs. Junction Temperature

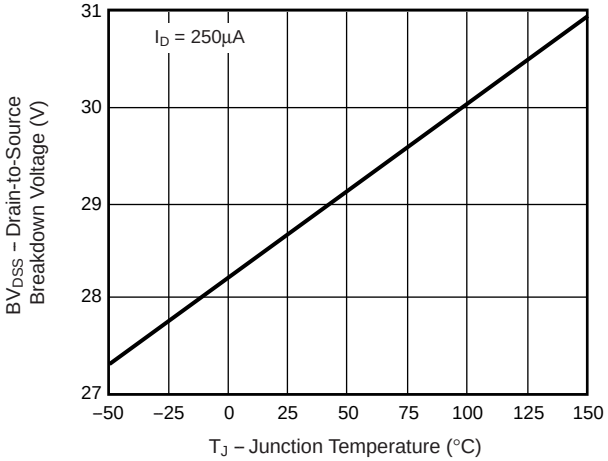


Fig. 11 – Thermal Impedance

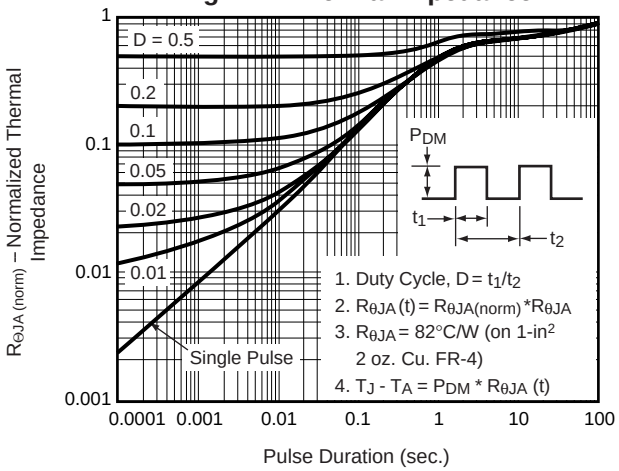


Fig. 12 – Power vs. Pulse Duration

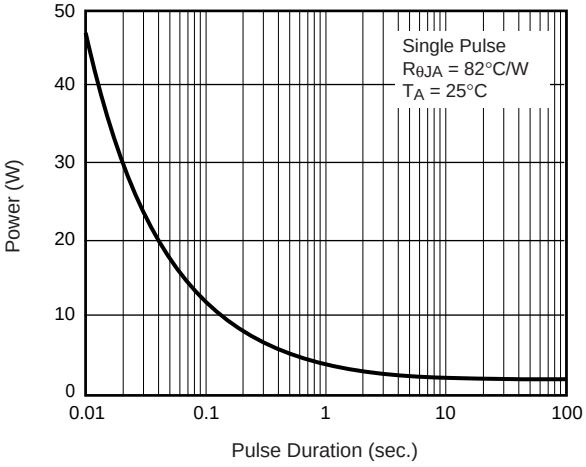


Fig. 13 – Maximum Safe Operating Area