Ultra Low ON-Resistance, Low Voltage, Single Supply, SPDT Analog Switch

The Intersil ISL54053 device is a low ON-resistance, low voltage, bidirectional, single pole/double throw (SPDT) analog switch designed to operate from a single +1.8V to +5.5V supply. Targeted applications include battery powered equipment which benefit from low r_{ON} (0.8Ω) and fast switching speeds (t_{ON} = 24ns, t_{OFF} = 10ns). The digital logic input is 1.8V logic compatible when using a single +3.0V supply.

Cell phones, for example, often face ASIC functionality limitations. The number of analog input or GPIO pins may be limited and digital geometries are not well suited to analog switch performance. This part may be used to "mux-in" additional functionality while reducing ASIC design risk. The ISL54053 is offered in the 6 Ld 1.2mmx1.0mmx0.5mm µTDFN package, alleviating board space limitations.

The ISL54053 is a committed SPDT that consists of one normally open (NO) and one normally closed(NC) switch. This configuration can also be used as a 2-to-1 multiplexer.

TABLE 1. FEATURES AT A GLANCE

	ISL54053
Number of Switches	1
SW	SPDT or 2-1 MUX
1.8V r_{ON}	2.3Ω
1.8V t_{ON}/t_{OFF}	68ns/45ns
3V r_{ON}	1.1Ω
3V t_{ON}/t_{OFF}	29ns/12ns
5V r_{ON}	0.8Ω
5V t_{ON}/t_{OFF}	24ns/10ns
Packages	6 Ld µTDFN

Related Literature

- Technical Brief TB363 "Guidelines for Handling and Processing Moisture Sensitive Surface Mount Devices (SMDs)"

Features

- Drop In replacement for the NLAS5123
- ON-resistance (r_{ON})
  - V_{CC} = +5.0V 0.8Ω
  - V_{CC} = +3.0V 1.1Ω
  - V_{CC} = +1.8V 2.3Ω
- r_{ON} matching between channels 0.004Ω
- r_{ON} flatness (+4.5V Supply) 0.04Ω
- Single supply operation . . . . +1.8V to +5.5V
- Fast switching action (+4.5V Supply)
  - t_{ON} 24ns
  - t_{OFF} 10ns
- Guaranteed break-before-make
- ESD HBM rating . . . . >6kV
- 1.8V CMOS logic compatible (+3V supply)
- Available in 6 lead µTDFN package
- Pb-free plus anneal available (RoHS compliant)

Applications

- Battery powered, handheld, and portable equipment
  - Cellular/mobile phones
  - Pagers
  - Laptops, notebooks, palmtops
- Portable test and measurement
- Medical equipment
- Audio and video switching

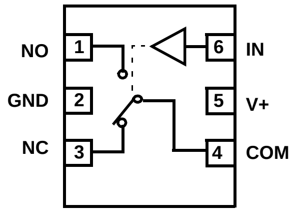
Ordering Information

PART NUMBER (Note)	PART MARKING	TEMP. RANGE (°C)	PACKAGE (Pb-Free)	PKG. DWG. #
ISL54053IRUZ-T	C	-40 to +85	6 Ld µTDFN Tape and Reel	L6.1.2x1.0A

NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Pinout (Note 1)

ISL54053
(6 LD µTDFN)
TOP VIEW



NOTE:

1. Switches Shown for Logic “0” Input.

Truth Table

LOGIC	PIN NC	PIN NO
0	On	Off
1	Off	On

NOTE: Logic “0” ≤ 0.5V. Logic “1” ≥ 1.4V with a 3.0V supply.

Pin Descriptions

PIN	FUNCTION
V+	System Power Supply Input (+1.8V to +5.5V)
GND	Ground Connection
IN	Digital Control Input
COM	Analog Switch Common Pin
NO	Analog Switch Normally Open Pin
NC	Analog Switch Normally Closed Pin

Absolute Maximum Ratings

V+ to GND . . . . -0.5 to 6.0V
Input Voltages
NO, NC, IN (Note 2) . . . . -0.5 to ((V+) + 0.5V)
Output Voltages
COM (Note 2) . . . . -0.5 to ((V+) + 0.5V)
Continuous Current NO, NC, or COM . . . . ±300mA
Peak Current NO, NC, or COM
(Pulsed 1ms, 10% Duty Cycle, Max) . . . . ±500mA
ESD Rating
Human Body Model (Per MIL-STD-883 Method 3015.7) . . . .>6kV
Machine Model (Per EIAJ ED-4701 Method C-111) . . . .>200V
Charged Device Model (Per EOS/ESD DS5.3, 4/14/93) . .>1000V

Operating Conditions

V+ (Positive DC Supply Voltage) . . . . 1.8V to 5.5V
Analog Signal Range . . . . 0V to V+
V_{IN} (Digital Logic Input Voltage (IN) . . . . 0V to V+
Temperature Range . . . . -40°C to +85°C

Thermal Information

Thermal Resistance (Typical, Note 3) θ_{JA} (°C/W)
6 Ld µTDFN Package 175
Maximum Junction Temperature (Plastic Package) . . . . +150°C
Maximum Storage Temperature Range . . . . -65°C to +150°C
Maximum Lead Temperature (Soldering 10s) . . . . +300°C
(Lead Tips Only)
Pb-free reflow profile . . . . see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

2. Signals on NC, NO, IN, or COM exceeding V+ or GND are clamped by internal diodes. Limit forward diode current to maximum current ratings.
3. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.

Electrical Specifications - 5V Supply

Test Conditions: V+ = +4.5V to +5.5V, GND = 0V, V_{INH} = 2.4V, V_{INL} = 0.8V (Notes 4, 6), Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	TEMP (°C)	(NOTE 5) MIN	TYP	(NOTE 5) MAX	UNITS
ANALOG SWITCH CHARACTERISTICS						
Analog Signal Range, V_{ANALOG}		Full	0	-	V+	V
ON-Resistance, r_{ON}	V+ = 4.5V, I_{COM} = 100mA, V_{NO} or V_{NC} = 0V to V+, (See Figure 5)	25	-	0.86	-	Ω
		Full	-	1	-	Ω
r_{ON} Matching Between Channels, Δr_{ON}	V+ = 4.5V, I_{COM} = 100mA, V_{NO} or V_{NC} = 2.5V	25	-	0.004	-	Ω
		Full	-	0.004	-	Ω
r_{ON} Flatness, $r_{FLAT(ON)}$	V+ = 4.5V, I_{COM} = 100mA, V_{NO} or V_{NC} = 0V to V+, (Note 7)	25	-	0.04	-	Ω
		Full	-	0.06	-	Ω
NO or NC OFF Leakage Current, $I_{NO(OFF)}$ or $I_{NC(OFF)}$	V+ = 5.5V, V_{COM} = 0.3V, 5V, V_{NO} or V_{NC} = 5V, 0.3V	25	-10	5	10	nA
		Full	-150	-	150	nA
COM ON Leakage Current, $I_{COM(ON)}$	V+ = 5.5V, V_{COM} = 0.3V, 5V, or V_{NO} or V_{NC} = 0.3V, 5V, or floating	25	-20	9	20	nA
		Full	-300	-	300	nA
DYNAMIC CHARACTERISTICS						
Turn-ON Time, t_{ON}	V+ = 4.5V, V_{NO} or V_{NC} = 3.0V, R_L = 50Ω, C_L = 35pF (See Figure 1, Note 8)	25	-	24	-	ns
		Full	-	30	-	ns
Turn-OFF Time, t_{OFF}	V+ = 4.5V, V_{NO} or V_{NC} = 3.0V, R_L = 50Ω, C_L = 35pF (See Figure 1, Note 8)	25	-	10	-	ns
		Full	-	15	-	ns
Break-Before-Make Time Delay, t_D	V+ = 5.5V, V_{NO} or V_{NC} = 3.0V, R_L = 50Ω, C_L = 35pF (See Figure 3, Note 8)	Full	-	10	-	ns
Charge Injection, Q	V_G = 0V, R_G = 0Ω, C_L = 1.0nF (See Figure 2)	25	-	26	-	pC
OFF Isolation	R_L = 50Ω, C_L = 5pF, f = 100kHz, V_{COM} = $1V_{RMS}$ (See Figure 4)	25	-	80	-	dB
Crosstalk (Channel-to-Channel)	R_L = 50Ω, C_L = 5pF, f = 100kHz, V_{COM} = $1V_{RMS}$ (See Figure 6)	25	-	-83	-	dB
Total Harmonic Distortion	f = 20Hz to 20kHz, V_{COM} = $0.5V_{P-P}$, R_L = 600Ω	25	-	0.03	-	%

Electrical Specifications - 5V Supply

Test Conditions: V+ = +4.5V to +5.5V, GND = 0V, V_{INH} = 2.4V, V_{INL} = 0.8V (Notes 4, 6), Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	TEMP (°C)	(NOTE 5) MIN	TYP	(NOTE 5) MAX	UNITS
-3dB Bandwidth	R_L = 50Ω	25	-	190	-	MHz
NO or NC OFF Capacitance, C_{OFF}	V+ = 4.5V, f = 1MHz, V_{NO} or V_{NC} = V_{COM} = 0V (See Figure 7)	25	-	16	-	pF
COM ON Capacitance, $C_{COM(ON)}$	V+ = 4.5V, f = 1MHz, V_{NO} or V_{NC} = V_{COM} = 0V (See Figure 7)	25	-	48	-	pF
POWER SUPPLY CHARACTERISTICS						
Power Supply Range		Full	1.8	-	5.5	V
Positive Supply Current, I+	V+ = 5.5V, V_{IN} = 0V or V+	25	-	0.075	0.1	µA
		Full	-	-	2.5	µA
DIGITAL INPUT CHARACTERISTICS						
Input Voltage Low, V_{INL}		Full	-	-	0.8	V
Input Voltage High, V_{INH}		Full	2.4	-	-	V
Input Current, I_{INH}, I_{INL}	V+ = 5.5V, V_{IN} = 0V or V+	Full	-0.1	-	0.1	µA

Electrical Specifications - 3V Supply

Test Conditions: V+ = +2.7V to +3.6V, GND = 0V, V_{INH} = 1.4V, V_{INL} = 0.5V (Notes 4, 6), Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	TEMP (°C)	(NOTE 5) MIN	TYP	(NOTE 5) MAX	UNITS
ANALOG SWITCH CHARACTERISTICS						
Analog Signal Range, V_{ANALOG}		Full	0	-	V+	V
ON-Resistance, r_{ON}	V+ = 3.0V, I_{COM} = 100mA, V_{NO} or V_{NC} = 0V to V+, (See Figure 5)	25	-	1.1	1.2	Ω
		Full	-	-	1.5	Ω
r_{ON} Matching Between Channels, Δr_{ON}	V+ = 3.0V, I_{COM} = 100mA, V_{NO} or V_{NC} = 1.5V	25	-	0.004	0.14	Ω
		Full	-	-	0.14	Ω
r_{ON} Flatness, $r_{FLAT(ON)}$	V+ = 3.0V, I_{COM} = 100mA, V_{NO} or V_{NC} = 0V to V+, (Note 7)	25	-	0.04	0.35	Ω
		Full	-	-	0.4	Ω
DYNAMIC CHARACTERISTICS						
Turn-ON Time, t_{ON}	V+ = 2.7V, V_{NO} or V_{NC} = 1.5V, R_L = 50Ω, C_L = 35pF (See Figure 1, Note 8)	25	-	29	-	ns
		Full	-	35	-	ns
Turn-OFF Time, t_{OFF}	V+ = 2.7V, V_{NO} or V_{NC} = 1.5V, R_L = 50Ω, C_L = 35pF (See Figure 1, Note 8)	25	-	12	-	ns
		Full	-	17	-	ns
Break-Before-Make Time Delay, t_D	V+ = 3.6V, V_{NO} or V_{NC} = 1.5V, R_L = 50Ω, C_L = 35pF (See Figure 3, Note 8)	Full	-	10	-	ns
Charge Injection, Q	V_G = 0V, R_G = 0Ω, C_L = 1.0nF (See Figure 2)	25	-	32	-	pC
OFF Isolation	R_L = 50Ω, C_L = 5pF, f = 100kHz, V_{COM} = $1V_{RMS}$ (See Figure 4)	25	-	80	-	dB
Crosstalk (Channel-to-Channel)	R_L = 50Ω, C_L = 5pF, f = 100kHz, V_{COM} = $1V_{RMS}$ (See Figure 6)	25	-	-83	-	dB
Total Harmonic Distortion	f = 20Hz to 20kHz, V_{COM} = $0.5V_{P-P}$, R_L = 600Ω	25	-	0.03	-	%
-3dB Bandwidth	R_L = 50Ω	25	-	190	-	MHz
NO or NC OFF Capacitance, C_{OFF}	f = 1MHz, V_{NO} or V_{NC} = V_{COM} = 0V (See Figure 7)	25	-	16	-	pF
COM ON Capacitance, $C_{COM(ON)}$	f = 1MHz, V_{NO} or V_{NC} = V_{COM} = 0V (See Figure 7)	25	-	48	-	pF
DIGITAL INPUT CHARACTERISTICS						
Input Voltage Low, V_{INL}		Full	-	-	0.5	V
Input Voltage High, V_{INH}		Full	1.4	-	-	V
Input Current, I_{INH}, I_{INL}	V+ = 3.6V, V_{IN} = 0V or V+	Full	-0.1	-	0.1	µA

Electrical Specifications - 1.8V Supply

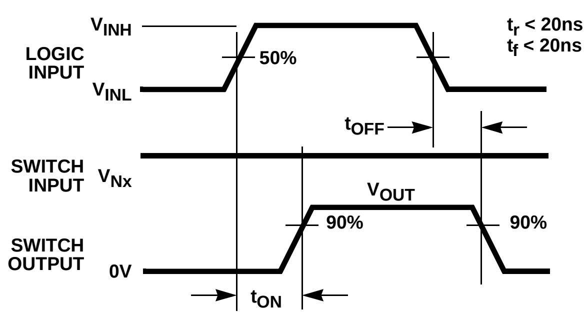
Test Conditions: V+ = +1.8V, GND = 0V, V_{INH} = 1V, V_{INL} = 0.4V (Notes 4, 6), Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	TEMP (°C)	(NOTE 5) MIN	TYP	(NOTE 5) MAX	UNITS
ANALOG SWITCH CHARACTERISTICS						
Analog Signal Range, V_{ANALOG}		Full	0	-	V+	V
ON-Resistance, r_{ON}	V+ = 1.8V, I_{COM} = 10mA, V_{NO} or V_{NC} = 0V to V+, (See Figure 5)	25	-	2.33	-	Ω
		Full	-	2.54	-	Ω
DYNAMIC CHARACTERISTICS						
Turn-ON Time, t_{ON}	V+ = 1.8V, V_{NO} or V_{NC} = 1.5V, R_L = 50Ω, C_L = 35pF (See Figure 1, Note 8)	25	-	68	-	ns
		Full	-	93	-	ns
Turn-OFF Time, t_{OFF}	V+ = 1.8V, V_{NO} or V_{NC} = 1.5V, R_L = 50Ω, C_L = 35pF (See Figure 1, Note 8)	25	-	45	-	ns
		Full	-	71	-	ns
Break-Before-Make Time Delay, t_D	V+ = 1.8V, V_{NO} or V_{NC} = 1.5V, R_L = 50Ω, C_L = 35pF (See Figure 3, Note 8)	Full	-	15	-	ns
Charge Injection, Q	V_G = 0, R_G = 0Ω, C_L = 1.0nF (See Figure 2)	25	-	18	-	pC
DIGITAL INPUT CHARACTERISTICS						
Input Voltage Low, V_{INL}		Full	-	-	0.4	V
Input Voltage High, V_{INH}		Full	1	-	-	V

NOTES:

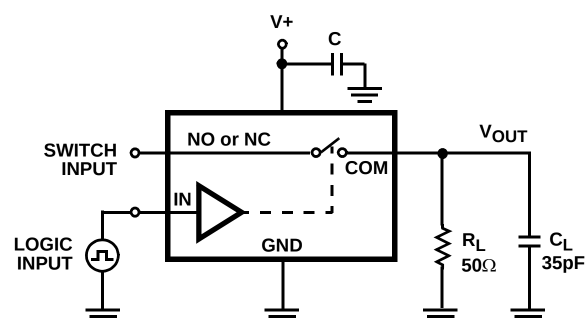
4. V_{IN} = input voltage to perform proper function.
5. The algebraic convention, whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
6. Parts are 100% tested at +25°C. Limits across the full temperature range are guaranteed by design and correlation.
7. Flatness is defined as the difference between maximum and minimum value of on-resistance over the specified analog signal range.
8. Guaranteed by design.

Test Circuits and Waveforms



Logic input waveform is inverted for switches that have the opposite logic sense.

FIGURE 1A. MEASUREMENT POINTS



Repeat test for all switches. C_L includes fixture and stray capacitance.

$$V_{OUT} = V_{(NO\ or\ NC)} \frac{R_L}{R_L + r_{(ON)}}$$

FIGURE 1B. TEST CIRCUIT

FIGURE 1. SWITCHING TIMES

Test Circuits and Waveforms (Continued)

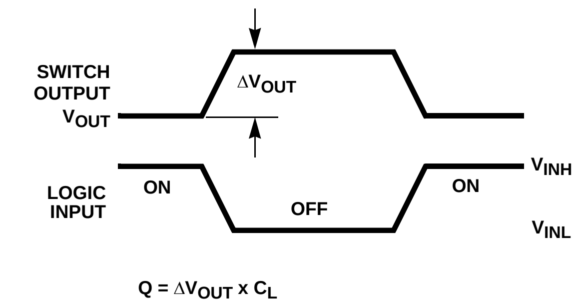


FIGURE 2A. MEASUREMENT POINTS

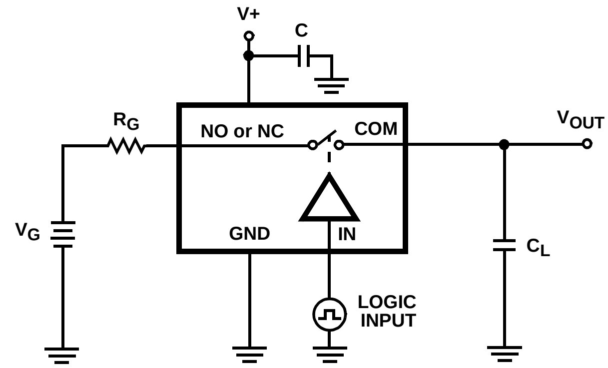


FIGURE 2B. TEST CIRCUIT

FIGURE 2. CHARGE INJECTION

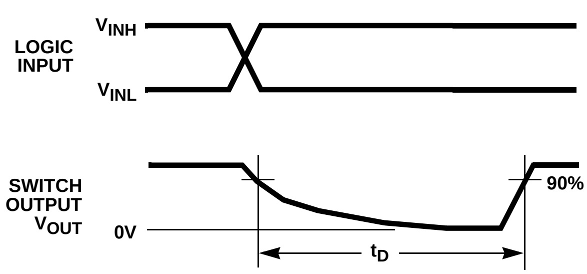
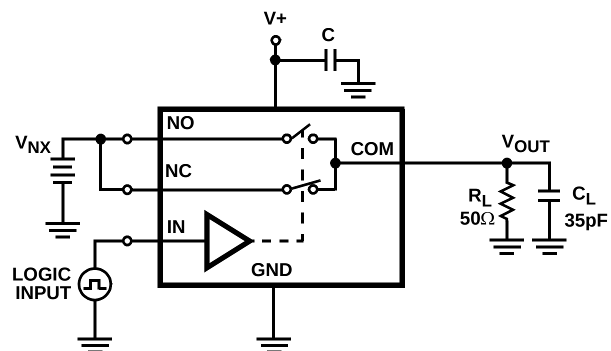


FIGURE 3A. MEASUREMENT POINTS



C_L includes fixture and stray capacitance.

FIGURE 3B. TEST CIRCUIT

FIGURE 3. BREAK-BEFORE-MAKE TIME

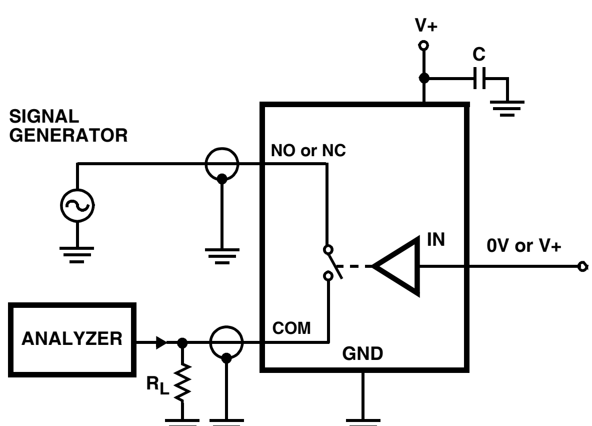


FIGURE 4. OFF ISOLATION TEST CIRCUIT

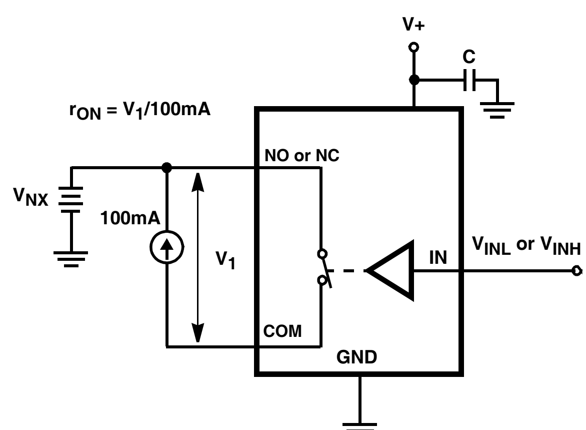


FIGURE 5. r_{ON} TEST CIRCUIT

Test Circuits and Waveforms (Continued)

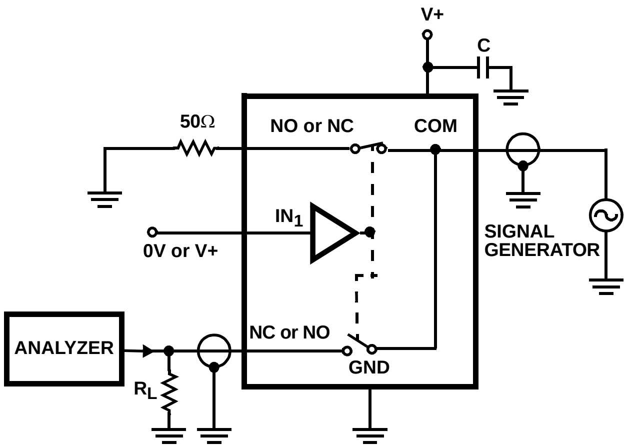


FIGURE 6. CROSSTALK TEST CIRCUIT

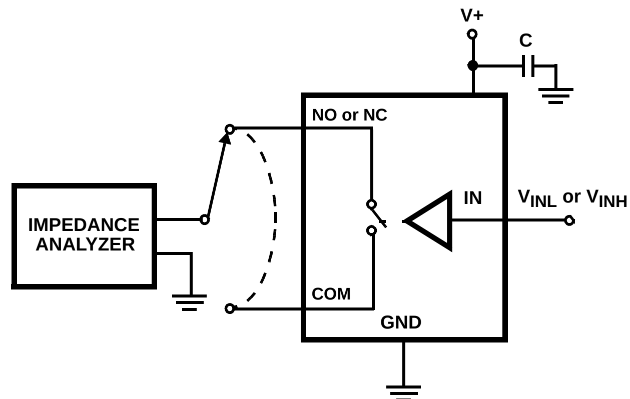


FIGURE 7. CAPACITANCE TEST CIRCUIT

Detailed Description

The ISL54053 is a bidirectional, single pole/double throw (SPDT) analog switch which offers precise switching capability from a single 1.8V to 5.5V supply with low on-resistance (0.8Ω) and high speed operation (t_{ON} = 24ns, t_{OFF} = 10ns). The device is especially well suited for portable battery powered equipment due to its low operating supply voltage (1.8V), low power consumption (5.5µW), low leakage currents (300nA max) and the small µTDFN package. The low on-resistance and r_{ON} flatness provide very low insertion loss and distortion to application that require signal reproduction.

Supply Sequencing and Overvoltage Protection

With any CMOS device, proper power supply sequencing is required to protect the device from excessive input currents which might permanently damage the IC. All I/O pins contain ESD protection diodes from the pin to V+ and to GND (see Figure 8). To prevent forward biasing these diodes, V+ must be applied before any input signals, and the input signal voltages must remain between V+ and GND.

If these conditions cannot be guaranteed, then precautions must be implemented to prohibit the current and voltage at the logic pin and signal pins from exceeding the maximum ratings of the switch. The following two methods can be used to provided additional protection to limit the current in the event that the voltage at a signal pin or logic pin goes below ground or above the V+ rail.

Logic inputs can be protected by adding a 1kΩ resistor in series with the logic input (see Figure 8). The resistor limits the input current below the threshold that produces permanent damage, and the sub-microamp input current produces an insignificant voltage drop during normal operation.

This method is not acceptable for the signal path inputs. Adding a series resistor to the switch input defeats the purpose of using a low r_{ON} switch. Connecting schottky diodes to the signal pins (as shown in Figure 8) will shunt the fault current to the supply or to ground thereby protecting the switch. These schottky diodes must be sized to handle the expected fault current.

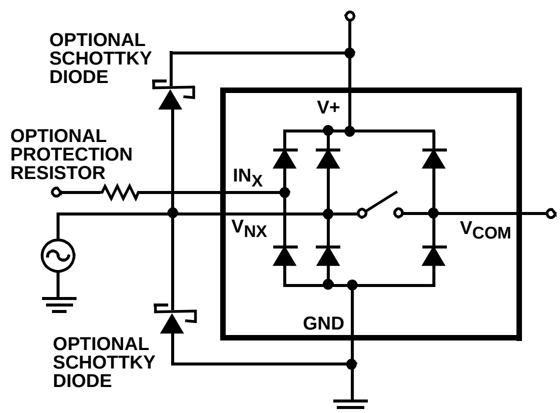


FIGURE 8. OVERVOLTAGE PROTECTION

Power-Supply Considerations

The ISL54053 construction is typical of most single supply CMOS analog switches, in that they have two supply pins: V+ and GND. V+ and GND drive the internal CMOS switches and set their analog voltage limits. Unlike switches with a 4.5V maximum supply voltage, the ISL54053 5.5V maximum supply voltage provides plenty of room for the 10% tolerance of 4.3V supplies, as well as room for overshoot and noise spikes.

The minimum recommended supply voltage is 1.8V but the part will operate with a supply below 1.8V. It is important to note that the input signal range, switching times, and on-resistance degrade at lower supply voltages. Refer to the electrical specification tables and *Typical Performance Curves* on page 8 for details.

V+ and GND also power the internal logic and level shifters. The level shifters convert the input logic levels to switched V+ and GND signals to drive the analog switch gate terminals.

This family of switches cannot be operated with bipolar supplies because the input switching point becomes negative in this configuration.

Logic-Level Thresholds

This switch family is 1.8V CMOS compatible (0.5V and 1.4V) over a supply range of 2V to 5V (see Figure 15). At 5V the V_{IH} level is about 1.2V. This is still below the 1.8V CMOS guaranteed high output minimum level of 1.4V, but noise margin is reduced.

The digital input stages draw supply current whenever the digital input voltage is not at one of the supply rails. Driving the digital input signals from GND to V+ with a fast transition time minimizes power dissipation.

High-Frequency Performance

In 50Ω systems, the ISL54053 has a -3dB bandwidth of 190MHz (see Figure 16). The frequency response is very consistent over a wide V+ range, and for varying analog signal levels.

An OFF switch acts like a capacitor and passes higher frequencies with less attenuation, resulting in signal feedthrough from a switch's input to its output. Off isolation is the resistance to this feedthrough, while crosstalk indicates the amount of feedthrough from one switch to another. Figure 17 details the high off isolation and crosstalk rejection provided by this family. At 100kHz, off isolation is about 80dB in 50Ω systems, decreasing approximately 20dB per decade as frequency increases. Higher load impedances decrease off isolation and crosstalk rejection due to the voltage divider action of the switch OFF impedance and the load impedance.

Leakage Considerations

ESD protection diodes are internally connected between each analog-signal pin and both V+ and GND. One of these diodes conducts if any analog signal exceeds V+ or GND.

Virtually all the analog leakage current comes from the ESD diodes to V+ or GND. Although the ESD diodes on a given signal pin are identical and therefore fairly well balanced, they are reverse biased differently. Each is biased by either V+ or GND and the analog signal. This means their leakages will vary as the signal varies. The difference in the two diode leakages to the V+ and GND pins constitutes the analog-signal-path leakage current. All analog leakage current flows between each pin and one of the supply terminals, not to the other switch terminal. This is why both sides of a given switch can show leakage currents of the same or opposite polarity. There is no connection between the analog signal paths and V+ or GND.

Typical Performance Curves T_A = +25°C, Unless Otherwise Specified

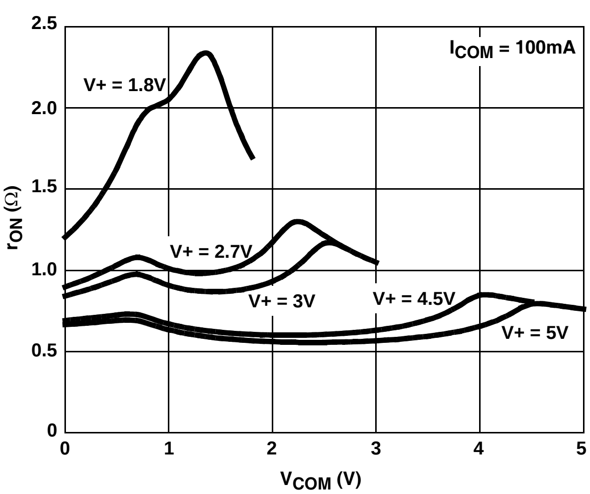


FIGURE 9. ON-RESISTANCE vs SUPPLY VOLTAGE vs SWITCH VOLTAGE

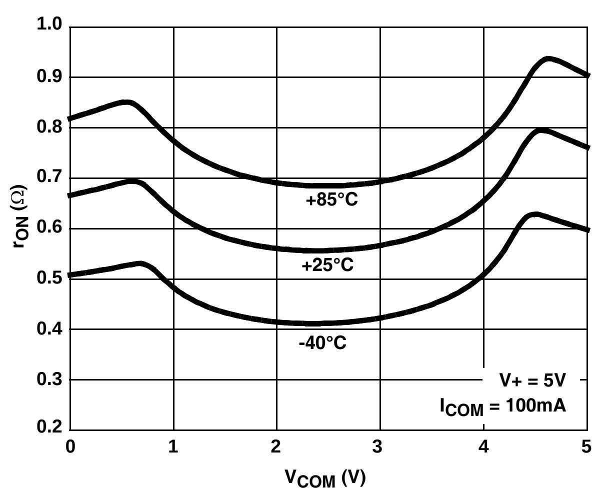


FIGURE 10. ON-RESISTANCE vs SWITCH VOLTAGE

Typical Performance Curves T_A = +25°C, Unless Otherwise Specified **(Continued)**

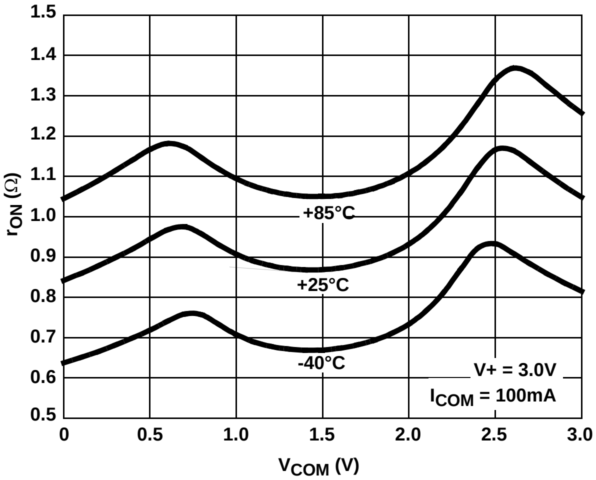


FIGURE 11. ON-RESISTANCE vs SWITCH VOLTAGE

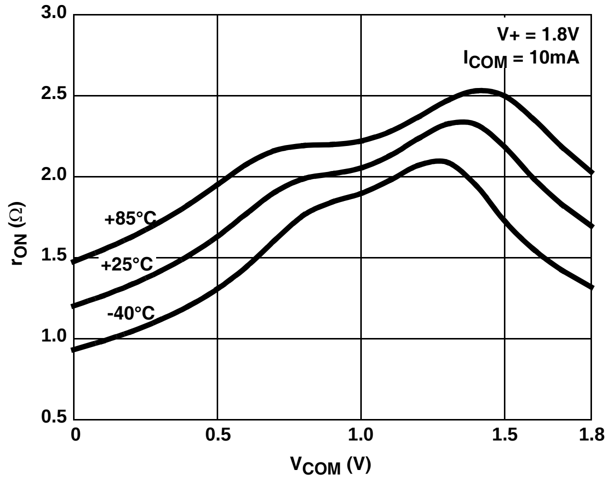


FIGURE 12. ON-RESISTANCE vs SWITCH VOLTAGE

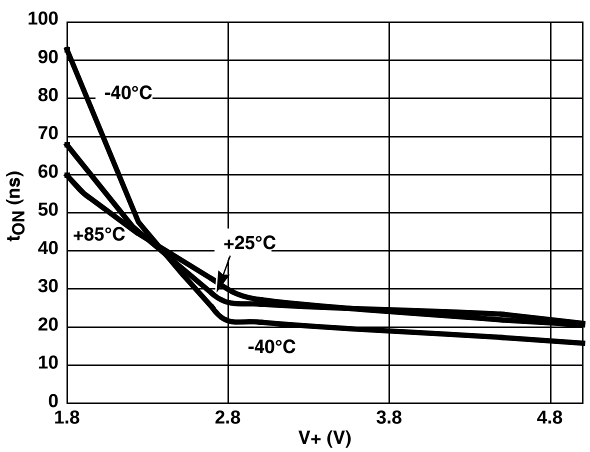


FIGURE 13. TURN-ON TIME vs SUPPLY VOLTAGE

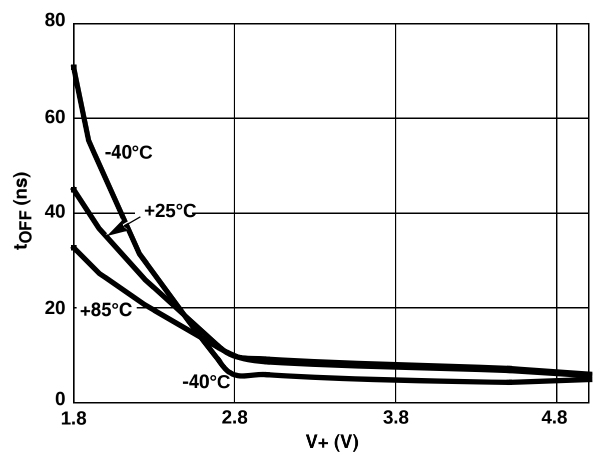


FIGURE 14. TURN-OFF TIME vs SUPPLY VOLTAGE

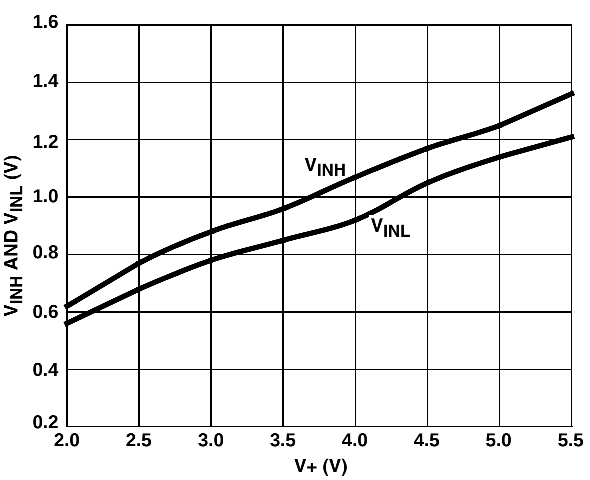


FIGURE 15. DIGITAL SWITCHING POINT vs SUPPLY VOLTAGE

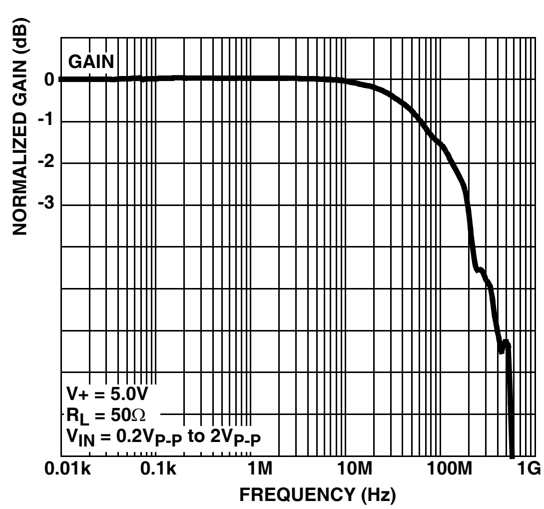


FIGURE 16. FREQUENCY RESPONSE

Typical Performance Curves T_A = +25°C, Unless Otherwise Specified **(Continued)**

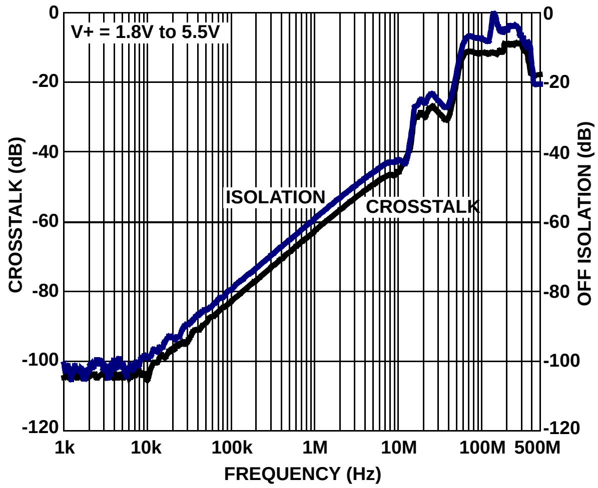


FIGURE 17. CROSSTALK AND OFF ISOLATION

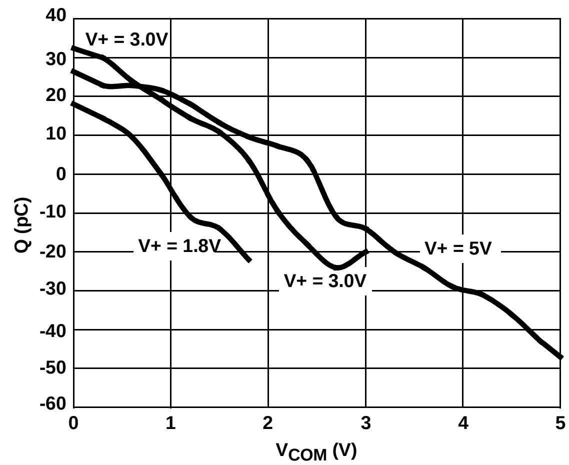


FIGURE 18. CHARGE INJECTION vs SWITCH VOLTAGE

Die Characteristics

SUBSTRATE POTENTIAL (POWERED UP):

GND

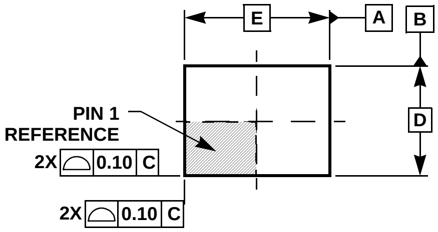
TRANSISTOR COUNT:

57

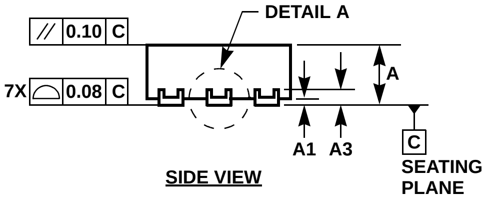
PROCESS:

Submicron CMOS

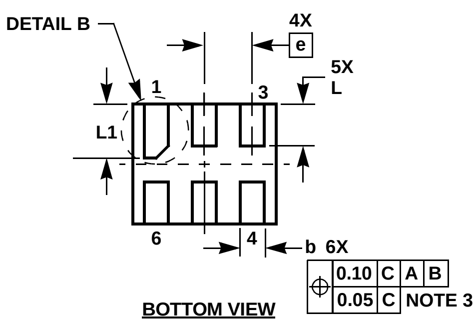
Ultra Thin Dual Flat No-Lead Plastic Package (UTDFN)



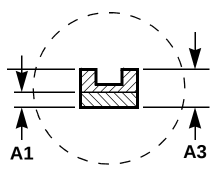
TOP VIEW



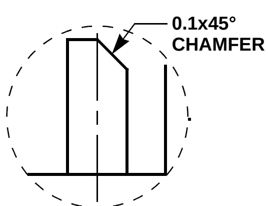
SIDE VIEW



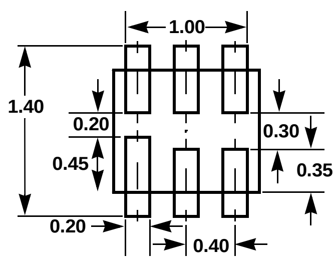
BOTTOM VIEW



DETAIL A



DETAIL B PIN 1 LEAD



LAND PATTERN 10

L6.1.2x1.0A

6 LEAD ULTRA THIN DUAL FLAT NO-LEAD PLASTIC PACKAGE

SYMBOL	MILLIMETERS			NOTES
	MIN	NOMINAL	MAX	
A	0.45	0.50	0.55	-
A1	-	-	0.05	-
A3	0.127 REF			-
b	0.15	0.20	0.25	5
D	0.95	1.00	1.05	-
E	1.15	1.20	1.25	-
e	0.40 BSC			-
L	0.30	0.35	0.40	-
L1	0.40	0.45	0.50	-
N	6			2
Ne	3			3
θ	0	-	12	4

Rev. 2 8/06

NOTES:

1. Dimensioning and tolerancing conform to ASME Y14.5-1994.
2. N is the number of terminals.
3. Ne refers to the number of terminals on E side.
4. All dimensions are in millimeters. Angles are in degrees.
5. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. Maximum package warpage is 0.05mm.
8. Maximum allowable burrs is 0.076mm in all directions.
9. JEDEC Reference MO-255.
10. For additional information, to assist with the PCB Land Pattern Design effort, see Intersil Technical Brief TB389.