Data Sheet | February 15, 2006 | FN9246.0

Three-Phase Buck PWM Controller with High Current Integrated MOSFET Drivers

The ISL8103 is a three-phase PWM control IC with integrated MOSFET drivers. It provides a precision voltage regulation system for multiple applications including, but not limited to, high current low voltage point-of-load converters, embedded applications and other general purpose low voltage medium to high current applications.The integration of power MOSFET drivers into the controller IC marks a departure from the separate PWM controller and driver configuration of previous multi-phase product families. By reducing the number of external parts, this integration allows for a cost and space saving power management solution.

Output voltage can be programmed using the on-chip DAC or an external precision reference. A two bit code programs the DAC reference to one of 4 possible values (0.6V, 0.9V, 1.2V and 1.5V). A unity gain, differential amplifier is provided for remote voltage sensing, compensating for any potential difference between remote and local grounds. The output voltage can also be offset through the use of single external resistor. An optional droop function is also implemented and can be disabled for applications having less stringent output voltage variation requirements or experiencing less severe step loads.

A unique feature of the ISL8103 is the combined use of both DCR and $r_{DS(ON)}$ current sensing. Load line voltage positioning and overcurrent protection are accomplished through continuous inductor DCR current sensing, while $r_{DS(ON)}$ current sensing is used for accurate channel-current balance. Using both methods of current sampling utilizes the best advantages of each technique.

Protection features of this controller IC include a set of sophisticated overvoltage and overcurrent protection. Overvoltage results in the converter turning the lower MOSFETs ON to clamp the rising output voltage and protect the load. An OVP output is also provided to drive an optional crowbar device. The overcurrent protection level is set through a single external resistor. Other protection features include protection against an open circuit on the remote sensing inputs. Combined, these features provide advanced protection for the output load.

Features

- Integrated Multi-Phase Power Conversion
  - 1, 2, or 3 Phase Operation
- Precision Output Voltage Regulation
  - Differential Remote Voltage Sensing
  - ±0.8% System Accuracy Over Temperature (for REF=0.6V and 0.9V)
  - ±0.5% System Accuracy Over Temperature (for REF=1.2V and 1.5V)
  - Usable for Output Voltages not Exceeding 2.3V
  - Adjustable Reference-Voltage Offset
- Precision Channel Current Sharing
  - Uses Loss-Less $r_{DS(ON)}$ Current Sampling
- Optional Load Line (Droop) Programming
  - Uses Loss-Less Inductor DCR Current Sampling
- Variable Gate-Drive Bias - 5V to 12V
- Internal or External Reference Voltage Setting
  - On-Chip Adjustable Fixed DAC Reference voltage with 2-bit Logic Input Selects from Four Fixed Reference Voltages (0.6V, 0.9V, 1.2V, 1.5V)
  - Reference can be Changed Dynamically
  - Can use an External Voltage Reference
- Overcurrent Protection
- Multi-tiered Overvoltage Protection
  - OVP Pin to Drive Optional Crowbar Device
- Selectable Operation Frequency up to 1.5MHz per Phase
- Digital Soft-Start
- Capable of Start-up in a Pre-Biased Load
- Pb-Free Plus Anneal Available (RoHS Compliant)

Applications

- High Current DDR/Chipset Core Voltage Regulators
- High Current, Low Voltage DC/DC Converters
- High Current, Low Voltage FPGA/ASIC DC/DC Converters

Ordering Information

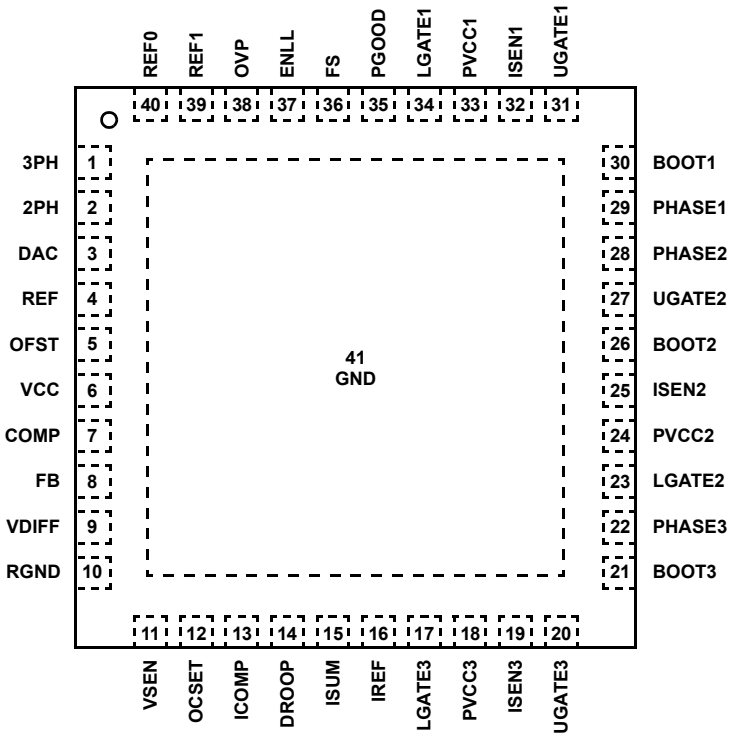
PART NUMBER*	PART MARKING	TEMERATURE (°C)	PACKAGE	PKG. DWG. #
ISL8103CRZ (Note)	ISL8103CRZ	0 to 70	40 Ld 6x6 QFN (Pb-free)	L40.6x6
ISL8103IRZ (Note)	ISL8103IRZ	-40 to 85	40 Ld 6x6 QFN (Pb-free)	L40.6x6
ISL8103EVAL1	Evaluation Platform			

* Add “-T” suffix for tape and reel.

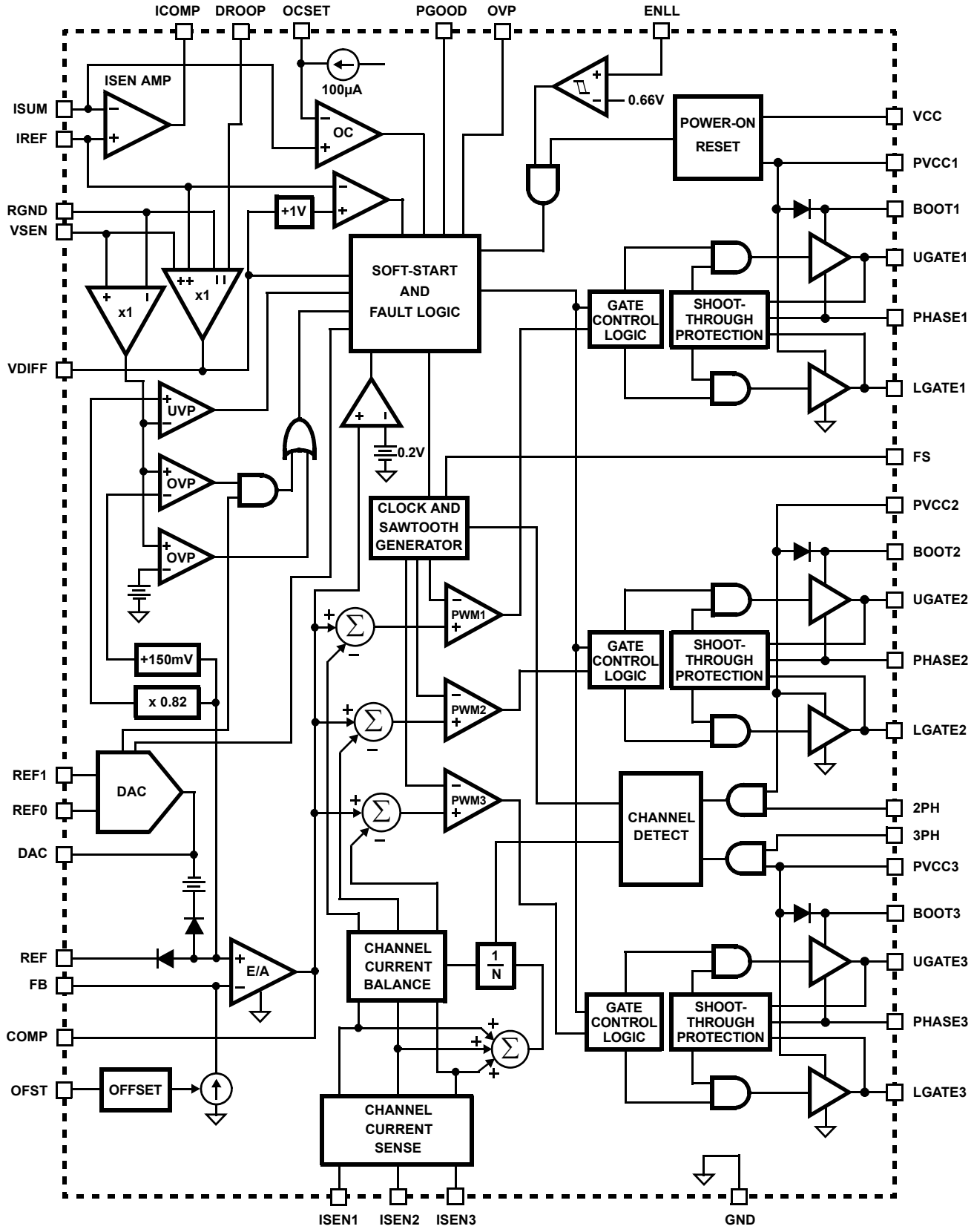
NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Pinout

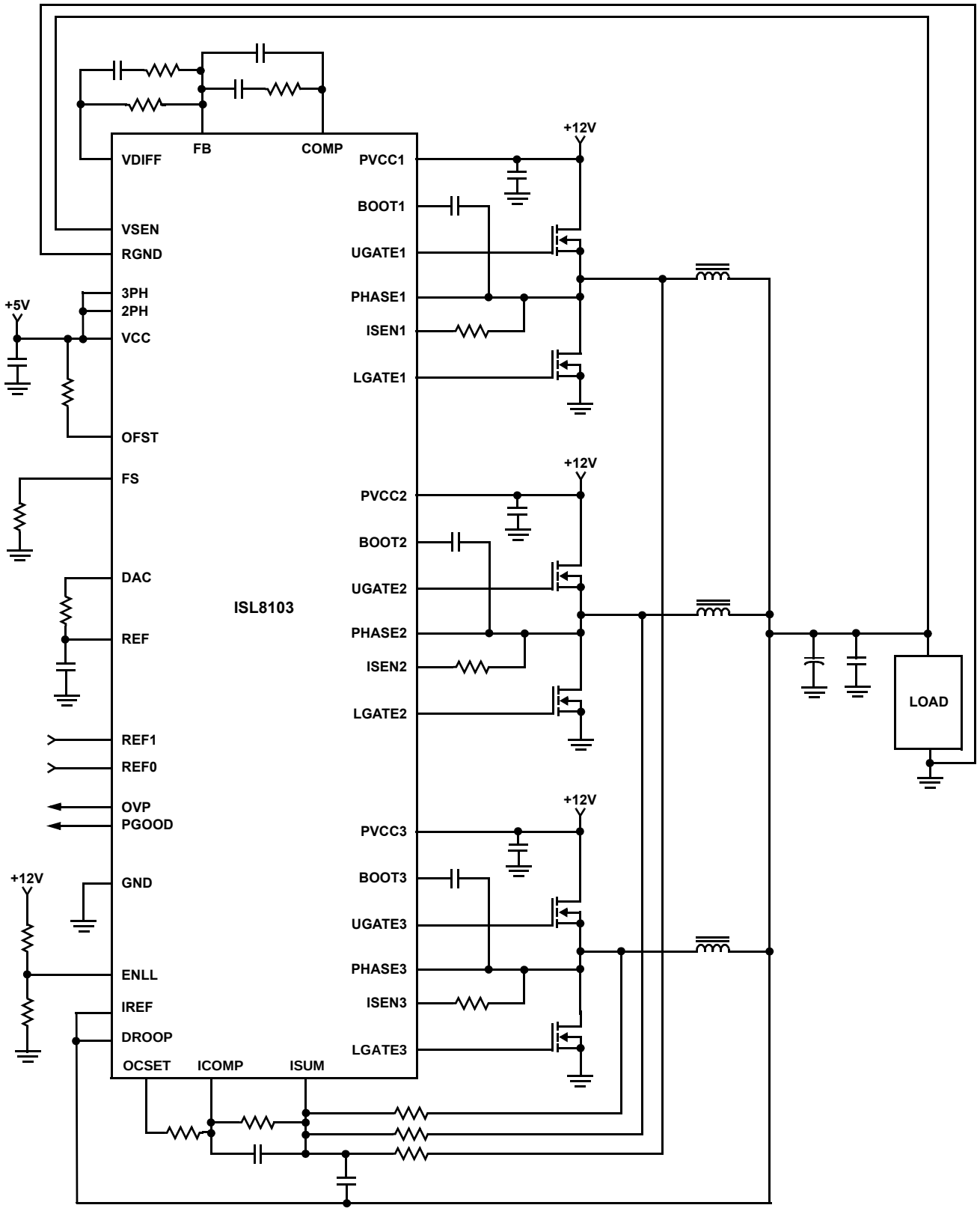
ISL8103 (6x6 QFN)
TOP VIEW



Block Diagram



Typical Application - ISL8103



Absolute Maximum Ratings

Supply Voltage, VCC . . . . . -0.3V to +6V
Supply Voltage, PVCC . . . . . -0.3V to +15V
Absolute Boot Voltage, V_{BOOT} . . . . . GND - 0.3V to GND + 36V
Phase Voltage, V_{PHASE} . . . . . GND - 0.3V to 15V (PVCC = 12)
GND - 8V (<400ns, 20µJ) to 24V (<200ns, $V_{BOOT-PHASE}$ = 12V)
Upper Gate Voltage, V_{UGATE} . . . . V_{PHASE} - 0.3V to V_{BOOT} + 0.3V
V_{PHASE} - 3.5V (<100ns Pulse Width, 2µJ) to V_{BOOT} + 0.3V
Lower Gate Voltage, V_{LGATE}. . . . . GND - 0.3V to PVCC + 0.3V
GND - 5V (<100ns Pulse Width, 2µJ) to PVCC+ 0.3V
Input, Output, or I/O Voltage . . . . . GND - 0.3V to VCC + 0.3V
ESD Classification . . . . . Class I JEDEC STD

Recommended Operating Conditions

VCC Supply Voltage . . . . . +5V ±5%
PVCC Supply Voltage . . . . . +5V to 12V ±5%
Ambient Temperature (ISL8103CRZ) . . . . . 0°C to 70°C
Ambient Temperature (ISL8103IRZ) . . . . . -40°C to 85°C

Thermal Information

Thermal Resistance	θ_{JA} (°C/W)	θ_{JC} (°C/W)
QFN Package (Notes 1, 2)	32	3.5

Maximum Junction Temperature . . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C

CAUTION: Stress above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied.

NOTES:

1. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See Tech Brief TB379.
2. For θ_{JC}, the "case temp" location is the center of the exposed metal pad on the package underside.

Electrical Specifications

Recommended Operating Conditions, Unless Otherwise Specified.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
BIAS SUPPLY AND INTERNAL OSCILLATOR					
Input Bias Supply Current	I_{VCC}; ENLL = high	-	15	20	mA
Gate Drive Bias Current	I_{PVCC}; ENLL = high; all gate outputs open, F_{sw} = 250kHz	-	0.8	2.00	mA
VCC POR (Power-On Reset) Threshold	VCC Rising	4.25	4.38	4.50	V
	VCC Falling	3.75	3.88	4.00	V
PVCC POR (Power-On Reset) Threshold	PVCC Rising	4.25	4.38	4.50	V
	PVCC Falling	3.75	3.88	4.00	V
Oscillator Ramp Amplitude (Note 3)	V_{PP}	-	1.50	-	V
Maximum Duty Cycle (Note 3)		-	66.6	-	%
CONTROL THRESHOLDS					
ENLL Rising Threshold		-	0.66	-	V
ENLL Hysteresis		-	100	-	mV
COMP Shutdown Threshold	COMP Falling	0.1	0.25	0.4	V
REFERENCE AND DAC					
System Accuracy (DAC = 0.6V, 0.9V)	DROOP connected to IREF	-0.8	-	0.8	%
System Accuracy (DAC = 1.2V, 1.50V)	DROOP connected to IREF	-0.5	-	0.5	%
DAC Input Low Voltage (REF0, REF1)		-	-	0.4	V
DAC Input High Voltage (REF0, REF1)		0.8	-	-	V
External Reference (Note 3)		0.6		1.75	V
OFS Sink Current Accuracy (Negative Offset)	R_{OFS} = 30kΩ from OFS to VCC	47.5	50.0	52.5	µA
OFS Source Current Accuracy (Positive Offset)	R_{OFS} = 10kΩ from OFS to GND	47.5	50.0	52.5	µA

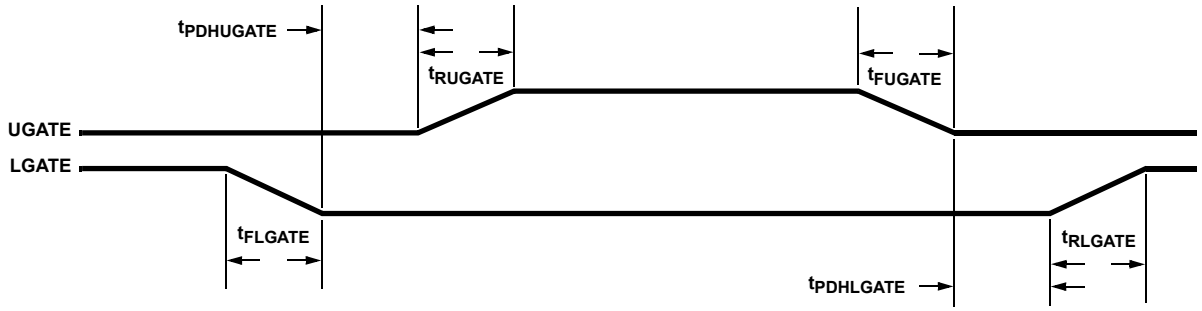
Electrical Specifications Recommended Operating Conditions, Unless Otherwise Specified. **(Continued)**

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
ERROR AMPLIFIER					
DC Gain (Note 3)	R_L = 10K to ground	-	96	-	dB
Gain-Bandwidth Product (Note 3)	C_L = 100pF, R_L = 10K to ground	-	20	-	MHz
Slew Rate (Note 3)	C_L = 100pF, Load = ±400µA	-	8	-	V/µs
Maximum Output Voltage	Load = 1mA	3.90	4.20	-	V
Minimum Output Voltage	Load = -1mA	-	0.85	1.0	V
REMOTE SENSE DIFFERENTIAL AMPLIFIER					
Input Bias Current (VSEN)	(VSEN = 1.5V)	49	55	60	µA
Bandwidth (Note 3)		-	20	-	MHz
Slew Rate (Note 3)		-	8	-	V/µs
OVERCURRENT PROTECTION					
OCSET Trip Current		93	100	107	µA
OCSET Accuracy	OC comparator offset (OCSET and ISUM Difference)	-5	0	5	mV
ICOMP Offset	ISEN amplifier offset	-5	0	5	mV
PROTECTION					
Undervoltage Threshold	VSEN falling	80	82	84	%VID
Undervoltage Hysteresis	VSEN Rising	-	3	-	%VID
Overvoltage Threshold while IC Disabled		1.62	1.67	1.72	V
Overvoltage Threshold	VSEN Rising	DAC + 125mV	DAC + 150mV	DAC + 175mV	V
Overvoltage Hysteresis	VSEN Falling	-	50	-	mV
Open Sense-Line Protection Threshold	IREF Rising and Falling	VDIFF + 0.9V	VDIFF + 1V	VDIFF + 1.1V	V
OVP Output High Drive Voltage	I_{OVP} = 50mA, VCC = 5V	2.2	3.9		V
SWITCHING TIME					
UGATE Rise Time (Note 3)	t_{RUGATE}; V_{PVCC} = 12V, 3nF Load, 10% to 90%	-	26	-	ns
LGATE Rise Time (Note 3)	t_{RLGATE}; V_{PVCC} = 12V, 3nF Load, 10% to 90%	-	18	-	ns
UGATE Fall Time (Note 3)	t_{FUGATE}; V_{PVCC} = 12V, 3nF Load, 90% to 10%	-	18	-	ns
LGATE Fall Time (Note 3)	t_{FLGATE}; V_{PVCC} = 12V, 3nF Load, 90% to 10%	-	12	-	ns
UGATE Turn-On Non-overlap (Note 3)	$t_{PDHUGATE}$; V_{PVCC} = 12V, 3nF Load, Adaptive	-	10	-	ns
LGATE Turn-On Non-overlap (Note 3)	$t_{PDHLGATE}$; V_{PVCC} = 12V, 3nF Load, Adaptive	-	10	-	ns
GATE DRIVE RESISTANCE (Note 3)					
Upper Drive Source Resistance	V_{PVCC} = 12V, 150mA Source Current	1.25	2.0	3.0	Ω
Upper Drive Sink Resistance	V_{PVCC} = 12V, 150mA Sink Current	0.9	1.6	3.0	Ω
Lower Drive Source Resistance	V_{PVCC} = 12V, 150mA Source Current	0.85	1.4	2.2	Ω
Lower Drive Sink Resistance	V_{PVCC} = 12V, 150mA Sink Current	0.60	0.94	1.35	Ω
OVER TEMPERATURE SHUTDOWN					
Thermal Shutdown Setpoint (Note 3)		-	160	-	°C
Thermal Recovery Setpoint (Note 3)		-	100	-	°C

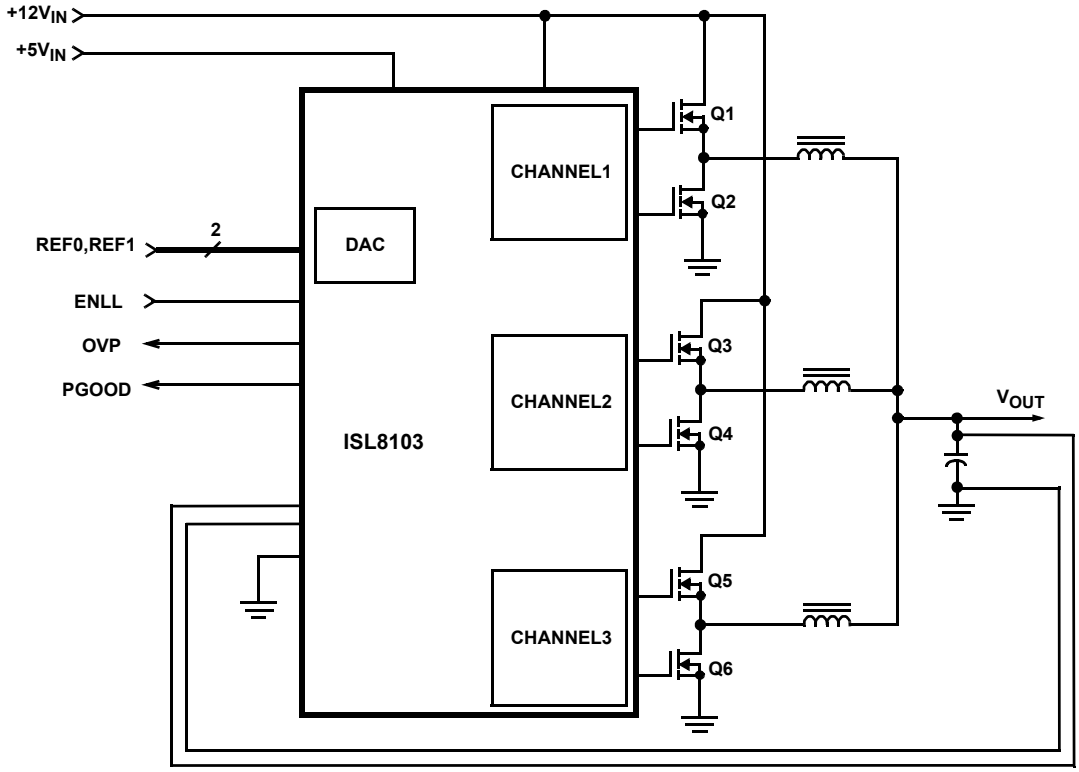
NOTE:

3. Parameter magnitude guaranteed by design. Not 100% tested.

Timing Diagram



Simplified Power System Diagram



Functional Pin Description

VCC (Pin 6)

Bias supply for the IC's small-signal circuitry. Connect this pin to a +5V supply and locally decouple using a quality 1.0µF ceramic capacitor.

PVCC1, PVCC2, PVCC3 (Pins 33, 24, 18)

Power supply pins for the corresponding channel MOSFET drive. These pins can be connected to any voltage from +5V to +12V, depending on the desired MOSFET gate drive level. Note that tying PVCC2 OR PVCC3 to GND has the same effect as tying 2PH or 3PH to GND for disabling the corresponding phase

GND (Pin 41)

Bias and reference ground for the IC.

ENLL (Pin 37)

This pin is a threshold sensitive (approximately 0.66V) enable input for the controller. Held low, this pin disables controller operation. Pulled high, the pin enables the controller for operation.

FS (Pin 36)

A resistor, placed from FS to ground, will set the switching frequency. Refer to Equation 33 and Figure 23 for proper resistor calculation

3PH and 2PH (Pins 1, 2)

These pins decide how many phases the controller will operate. Tying both pins to VCC allows for 3-phase operation. Tying the 3PH pin to GND causes the controller to operate in 2-phase mode, while connecting both 3PH and 2PH GND will allow for single phase operation.

REF0 and REF1 (Pins 40, 39)

These pins make up the 2-bit input that selects the fixed DAC reference voltage. These pins respond to TTL logic thresholds. The ISL8103 decodes these inputs to establish one of four fixed reference voltages; see “Table 1” for correspondence between REF0 and REF1 inputs and reference voltage settings.

These pins are internally pulled high, to approximately 1.2V, by 40µA (typically) internal current sources; the internal pull-up current decreases to 0 as the REF0 and REF1 voltages approach the internal pull-up voltage. Both REF0 and REF1 pins are compatible with external pull-up voltages not exceeding the IC’s bias voltage (VCC).

RGND and VSEN (Pins 10, 11)

RGND and VSEN are inputs to the precision differential remote-sense amplifier and should be connected to the sense pins of the remote load.

ICOMP, ISUM, and IREF (Pins 13, 15, 16)

ISUM, IREF, and ICOMP are the DCR current sense amplifier’s negative input, positive input, and output respectively. For accurate DCR current sensing, connect a resistor from each channel’s phase node to ISUM and connect IREF to the summing point of the output inductors. A parallel R-C feedback circuit connected between ISUM and ICOMP will then create a voltage from IREF to ICOMP proportional to the voltage drop across the inductor DCR. This voltage is referred to as the droop voltage and is added to the differential remote-sense amplifier’s output.

An optional 0.001-0.01µF ceramic capacitor can be placed from the IREF pin to the ISUM pin to help reduce common mode noise that might be introduced by the layout.

DROOP (Pin 14)

This pin enables or disables droop. Tie this pin to the ICOMP pin to enable droop. To disable droop, tie this pin to the IREF pin.

VDIFF (Pin 9)

VDIFF is the output of the differential remote-sense amplifier. The voltage on this pin is equal to the difference between VSEN and RGND added to the difference between IREF and ICOMP. VDIFF therefore represents the VOUT voltage plus the droop voltage.

FB and COMP (Pin 7, 8)

The internal error amplifier’s inverting input and output respectively. FB is connected to VDIFF through an external R or R-C network depending on the desired type of compensation (Type II or III). COMP is tied back to FB through an external R-C network to compensate the regulator.

PHASE1, PHASE2, and PHASE3 (Pins 29, 28, 22)

Connect these pins to the sources of the upper MOSFETs.

DAC (Pin 3)

The DAC pin is the direct output of the internal DAC. This pin is connected to the REF pin using a 1-5kΩ resistor. This pin can be left open if an external reference is used.

REF (Pin 4)

The REF input pin is the positive input of the error amplifier. This pin can be connected to the DAC pin using a resistor (1-5kΩ) when the internal DAC voltage is used as the reference voltage. When an external voltage reference is used, it must be connected directly to the REF pin, while the DAC pin is left unconnected. The output voltage will be regulated to the voltage at the REF pin unless this voltage is greater than the voltage at the DAC pin. If an external reference is used at this pin, its magnitude cannot exceed 1.75V.

A capacitor is used between the REF pin and ground to smooth the DAC voltage during soft-start.

OFST (Pin 5)

The OFST pin provides a means to program a DC current for generating an offset voltage across the resistor between FB and VDIFF. The offset current is generated via an external resistor and precision internal voltage references. The polarity of the offset is selected by connecting the resistor to GND or VCC. For no offset, the OFST pin should be left unconnected.

OCSET (Pin 12)

This is the overcurrent set pin. Placing a resistor from OCSET to ICOMP, allows a 100µA current to flow out of this pin, producing a voltage reference. Internal circuitry compares the voltage at OCSET to the voltage at ISUM, and if ISUM ever exceeds OCSET, the overcurrent protection activates.

ISEN1, ISEN2 and ISEN3 (Pins 32, 25, 19)

These pins are used for balancing the channel currents by sensing the current through each channel’s lower MOSFET when it is conducting. Connect a resistor between the ISEN1, ISEN2, and ISEN3 pins and their respective phase node. This resistor sets a current proportional to the current in the lower MOSFET during its conduction interval.

UGATE1, UGATE2, and UGATE3 (Pins 31, 27, 20)

Connect these pins to the upper MOSFETs’ gates. These pins are used to control the upper MOSFETs and are monitored for shoot-through prevention purposes. Maximum individual channel duty cycle is limited to 66%.

BOOT1, BOOT2, and BOOT3 (Pins 30, 26, 21)

These pins provide the bias voltage for the upper MOSFETs’ drives. Connect these pins to appropriately-chosen external bootstrap capacitors. Internal bootstrap diodes connected to the PVCC pins provide the necessary bootstrap charge.

These pins are the return path for the upper MOSFETs’ drives.

LGATE1, LGATE2, and LGATE3 (Pins 34, 23, 17)

These pins are used to control the lower MOSFETs and are monitored for shoot-through prevention purposes. Connect these pins to the lower MOSFETs' gates. Do not use external series gate resistors as this might lead to shoot-through.

PGOOD (Pin 35)

PGOOD is used as an indication of the end of soft-start. It is an open-drain logic output that is low impedance until the soft-start is completed and VOUT is equal to the VID setting. Once in normal operation PGOOD indicates whether the output voltage is within specified overvoltage and undervoltage limits. If the output voltage exceeds these limits or a reset event occurs (such as an overcurrent event), PGOOD becomes high impedance again. The potential at this pin should not exceed that of the potential at VCC pin by more than a typical forward diode drop at any time.

OVP (Pin 38)

Overvoltage protection pin. This pin pulls to VCC when an overvoltage condition is detected. Connect this pin to the gate of an SCR or MOSFET tied across V_{IN} and ground to prevent damage to a load device.

Operation

Multi-Phase Power Conversion

Modern low voltage DC/DC converter load current profiles have changed to the point that the advantages of multi-phase power conversion are impossible to ignore. The technical challenges associated with producing a single-phase converter that is both cost-effective and thermally viable have forced a change to the cost-saving approach of multi-phase. The ISL8103 controller helps simplify implementation by integrating vital functions and requiring minimal output components. The block diagram on page 3 provides a top level view of multi-phase power conversion using the ISL8103 controller.

Interleaving

The switching of each channel in a multi-phase converter is timed to be symmetrically out of phase with each of the other channels. In a 3-phase converter, each channel switches 1/3 cycle after the previous channel and 1/3 cycle before the following channel. As a result, the three-phase converter has a combined ripple frequency three times greater than the ripple frequency of any one phase. In addition, the peak-to-peak amplitude of the combined inductor currents is reduced in proportion to the number of phases (Equations 1 and 2). Increased ripple frequency and lower ripple amplitude mean that the designer can use less per-channel inductance and lower total output capacitance for any performance specification.

Figure 1 illustrates the multiplicative effect on output ripple frequency. The three channel currents (I_{L1}, I_{L2}, and I_{L3}) combine to form the AC ripple current and the DC load current. The ripple component has three times the ripple frequency of each individual channel current. Each PWM pulse is terminated 1/3 of a cycle after the PWM pulse of the previous phase. The peak-to-peak current for each phase is about 7A, and the dc components of the inductor currents combine to feed the load.

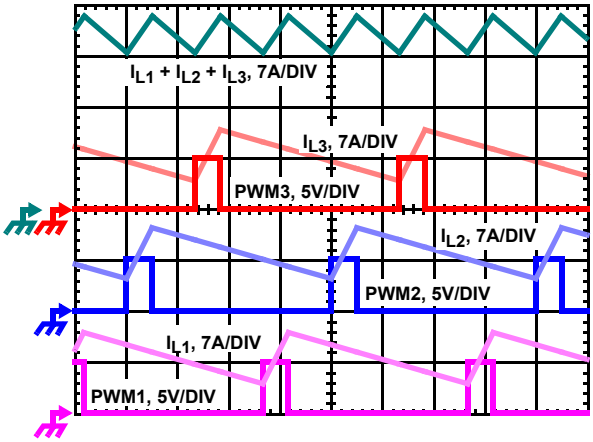


FIGURE 1. PWM AND INDUCTOR-CURRENT WAVEFORMS FOR 3-PHASE CONVERTER

To understand the reduction of ripple current amplitude in the multi-phase circuit, examine the equation representing an individual channel peak-to-peak inductor current.

$$I_{PP} = \frac{(V_{IN} - V_{OUT}) \cdot V_{OUT}}{L \cdot F_{SW} \cdot V_{IN}} \quad \text{(EQ. 1)}$$

In Equation 1, V_{IN} and V_{OUT} are the input and output voltages respectively, L is the single-channel inductor value, and F_{SW} is the switching frequency.

The output capacitors conduct the ripple component of the inductor current. In the case of multi-phase converters, the capacitor current is the sum of the ripple currents from each of the individual channels. Compare Equation 1 to the expression for the peak-to-peak current after the summation of N symmetrically phase-shifted inductor currents in Equation 2. Peak-to-peak ripple current decreases by an amount proportional to the number of channels. Output voltage ripple is a function of capacitance, capacitor equivalent series resistance (ESR), and inductor ripple current. Reducing the inductor ripple current allows the designer to use fewer or less costly output capacitors.

$$I_{C,PP} = \frac{(V_{IN} - N \cdot V_{OUT}) \cdot V_{OUT}}{L \cdot F_{SW} \cdot V_{IN}} \quad \text{(EQ. 2)}$$

Another benefit of interleaving is to reduce input ripple current. Input capacitance is determined in part by the maximum input ripple current. Multi-phase topologies can improve overall system cost and size by lowering input ripple current and allowing the designer to reduce the cost of input capacitance. The example in Figure 2 illustrates input

currents from a three-phase converter combining to reduce the total input ripple current.

The converter depicted in Figure 2 delivers 1.5V to a 36A load from a 12V input. The RMS input capacitor current is 6.1A. Compare this to a single-phase converter also stepping down 12V to 1.5V at 36A. The single-phase converter has a 13.3A RMS input capacitor current. The single-phase converter must use an input capacitor bank with twice the RMS current capacity as the equivalent three-phase converter.

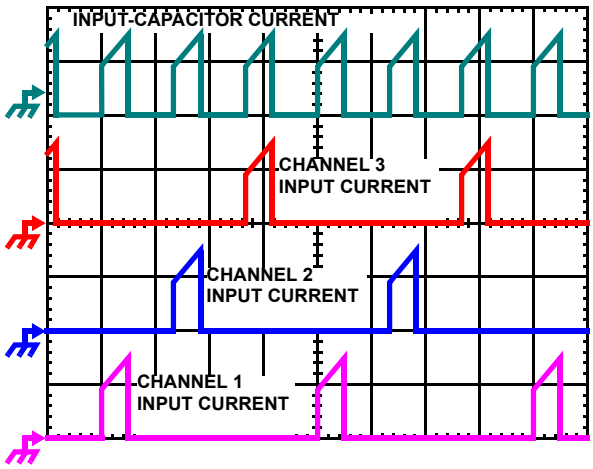


FIGURE 2. CHANNEL INPUT CURRENTS AND INPUT-CAPACITOR RMS CURRENT FOR 3-PHASE CONVERTER

Figures 24, 25 and 26 in the section entitled *Input Capacitor Selection* can be used to determine the input capacitor RMS current based on load current, duty cycle, and the number of channels. They are provided as aids in determining the optimal input capacitor solution.

PWM Operation

The timing of each converter leg is set by the number of active channels. The default channel setting for the ISL8103 is three. One switching cycle is defined as the time between the internal PWM1 pulse termination signals. The pulse termination signal is the internally generated clock signal that triggers the falling edge of PWM1. The cycle time of the pulse termination signal is the inverse of the switching frequency set by the resistor between the FS pin and ground. Each cycle begins when the clock signal commands PWM1 to go low. The PWM1 transition signals the internal channel 1 MOSFET driver to turn off the channel 1 upper MOSFET and turn on the channel 1 synchronous MOSFET. In the default channel configuration, the PWM2 pulse terminates 1/3 of a cycle after the PWM1 pulse. The PWM3 pulse terminates 1/3 of a cycle after PWM2.

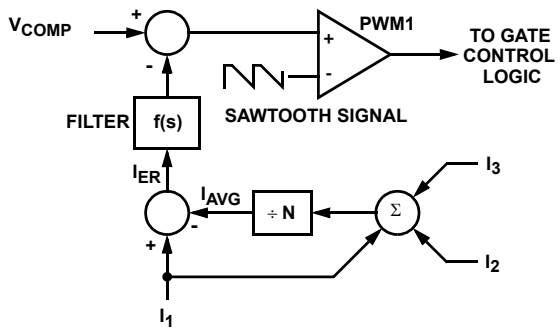
If PVCC3 is left open or connected to ground, two channel operation is selected and the PWM2 pulse terminates 1/2 of a cycle after the PWM1 pulse terminates. If both PVCC3 and PVCC2 are left open or connected to ground, single channel operation is selected. The 2PH and 3PH inputs can also be used to accomplish this function. Once a PWM pulse transitions low, it is held low for a minimum of 1/3 cycle. This forced off time is required to ensure an accurate current sample. Current sensing is described in the next section. After the forced off time expires, the PWM output is enabled. The PWM output state is driven by the position of the error amplifier output signal, VCOMP, minus the current correction signal relative to the sawtooth ramp as illustrated in Figure 3. When the modified VCOMP voltage crosses the sawtooth ramp, the PWM output transitions high. The internal MOSFET driver detects the change in state of the PWM signal and turns off the synchronous MOSFET and turns on the upper MOSFET. The PWM signal will remain high until the pulse termination signal marks the beginning of the next cycle by triggering the PWM signal low.

Channel Current Balance

One important benefit of multi-phase operation is the thermal advantage gained by distributing the dissipated heat over multiple devices and greater area. By doing this the designer avoids the complexity of driving parallel MOSFETs and the expense of using expensive heat sinks and exotic magnetic materials.

In order to realize the thermal advantage, it is important that each channel in a multi-phase converter be controlled to carry about the same amount of current at any load level. To achieve this, the currents through each channel must be sampled every switching cycle. The sampled currents, I_n, from each active channel are summed together and divided by the number of active channels. The resulting cycle average current, I_{AVG}, provides a measure of the total load current demand on the converter during each switching cycle. Channel current balance is achieved by comparing the sampled current of each channel to the cycle average current, and making the proper adjustment to each channel pulse width based on the error. Intersil's patented current-balance method is illustrated in Figure 3, with error correction for channel 1 represented. In the figure, the cycle average current, I_{AVG}, is compared with the channel 1 sample, I_1, to create an error signal I_{ER}.

The filtered error signal modifies the pulse width commanded by V_{COMP} to correct any unbalance and force I_{ER} toward zero. The same method for error signal correction is applied to each active channel.



NOTE: Channel 2 and 3 are optional.

FIGURE 3. CHANNEL 1 PWM FUNCTION AND CURRENT-BALANCE ADJUSTMENT

Current Sampling

In order to realize proper current balance, the currents in each channel must be sampled every switching cycle. This sampling occurs during the forced off-time, following a PWM transition low. During this time the current sense amplifier uses the ISEN inputs to reproduce a signal proportional to the inductor current, I_L. This sensed current, I_{SEN}, is simply a scaled version of the inductor current. The sample window opens exactly 1/6 of the switching period, t_{SW}, after the PWM transitions low. The sample window then stays open the rest of the switching cycle until PWM transitions high again, as illustrated in Figure 4.

The sampled current, at the end of the t_{SAMPLE}, is proportional to the inductor current and is held until the next switching period sample. The sampled current is used only for channel current balance.

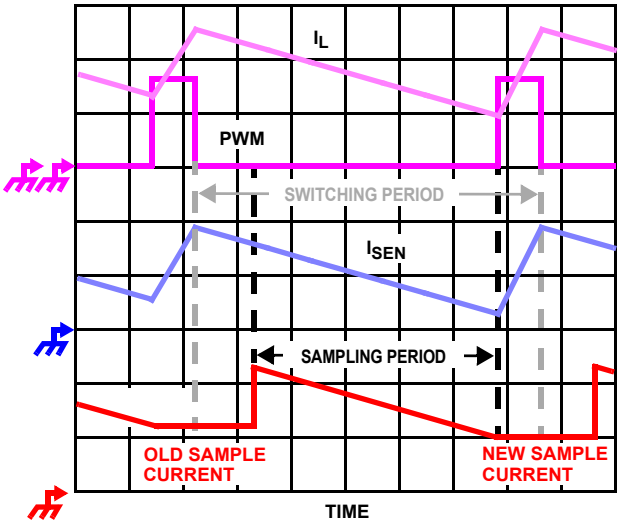


FIGURE 4. SAMPLE AND HOLD TIMING

The ISL8103 supports MOSFET $r_{DS(ON)}$ current sensing to sample each channel's current for channel current balance. The internal circuitry, shown in Figure 5 represents channel n of an N-channel converter. This circuitry is repeated for each channel in the converter, but may not be active depending on the status of the PVCC3 and PVCC2 pins, as described in the *PWM Operation* section.

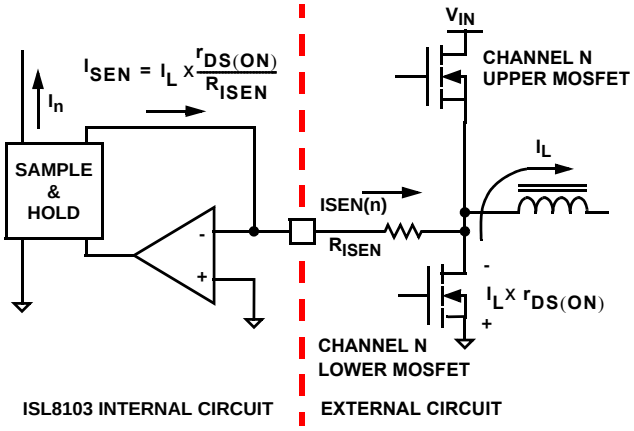


FIGURE 5. ISL8103 INTERNAL AND EXTERNAL CURRENT-SENSING CIRCUITRY FOR CURRENT BALANCE

The ISL8103 senses the channel load current by sampling the voltage across the lower MOSFET $r_{DS(ON)}$, as shown in Figure 5. A ground-referenced operational amplifier, internal to the ISL8103, is connected to the PHASE node through a resistor, R_{ISEN}. The voltage across R_{ISEN} is equivalent to the voltage drop across the $r_{DS(ON)}$ of the lower MOSFET while it is conducting. The resulting current into the ISEN pin is proportional to the channel current, I_L. The ISEN current is sampled and held as described in the *Current Sampling* section. From Figure 5, the following equation for I_n is derived where I_L is the channel current.

$$I_n = I_L \cdot \frac{r_{DS(ON)}}{R_{ISEN}} \quad \text{(EQ. 3)}$$

Output Voltage Setting

The ISL8103 uses a digital to analog converter (DAC) to generate a reference voltage based on the logic signals at the REF1, REF0 pins. The DAC decodes the 2-bit logic signals into one of the discrete voltages shown in Table 1. Each REF0 and REF1 pins are pulled up to an internal 1.2V voltage by weak current sources (40µA current, decreasing to 0 as the voltage at the REF0, REF1 pins varies from 0 to the internal 1.2V pull-up voltage). External pull-up resistors or active-high output stages can augment the pull-up current sources, up to a voltage of 5V. The DAC pin must be connected to REF pin through a 1-5kΩ resistor and a filter capacitor (0.022µF) is connected between REF and GND.

The ISL8103 accommodates the use of external voltage reference connected to REF pin if a different output voltage is required. The DAC voltage must be set at least as high as the external reference. The error amp internal noninverting input is the lower of REF or (DAC +300mV).

A third method for setting the output voltage is to use a resistor divider (R_{P1}, R_{S1}) from the output terminal (V_{OUT})

to VSEN pin to set the output voltage level as shown in Figure 6. This method is good for generating voltages up to 2.3V (with the REF voltage set to 1.5V).

For this case, the output voltage can be obtained as follows:

$$V_{OUT} = V_{REF} \cdot \frac{(R_{S1} + R_{P1})}{R_{P1}} \mp V_{OFS} - V_{DROOP} \quad \text{(EQ. 4)}$$

It is recommended to choose resistor values of less than 500Ω for R_{S1} and R_{P1} resistors in order to get better output voltage DC accuracy.

TABLE 1. ISL8103 DAC VOLTAGE SELECTION TABLE

REF1	REF0	VDAC
0	0	0.600V
0	1	0.900V
1	0	1.200V
1	1	1.500V

Voltage Regulation

In order to regulate the output voltage to a specified level, the ISL8103 uses the integrating compensation network shown in Figure 6. This compensation network insures that the steady state error in the output voltage is limited only to the error in the reference voltage (output of the DAC or the external voltage reference) and offset errors in the OFS current source, remote sense and error amplifiers. Intersil specifies the guaranteed tolerance of the ISL8103 to include the combined tolerances of each of these elements, except when an external reference or voltage divider is used, then the tolerances of these components has to be taken into account.

The ISL8103 incorporates an internal differential remote-sense amplifier in the feedback path. The amplifier removes the voltage error encountered when measuring the output voltage relative to the controller ground reference point, resulting in a more accurate means of sensing output voltage. Connect the microprocessor sense pins to the non-inverting input, VSEN, and inverting input, RGND, of the remote-sense amplifier. The droop voltage, VDROOP, also feeds into the remote-sense amplifier. The remote-sense output, VDIFF, is therefore equal to the sum of the output voltage, VOUT, and the droop voltage. VDIFF is connected to the inverting input of the error amplifier through an external resistor.

The output of the error amplifier, V_{COMP}, is compared to the sawtooth waveform to generate the PWM signals. The PWM signals control the timing of the Internal MOSFET drivers and regulate the converter output so that the voltage at FB is equal to the voltage at REF. This will regulate the output voltage to be equal to Equation 5. The internal and external circuitry that controls voltage regulation is illustrated in Figure 6.

$$V_{OUT} = V_{REF} \pm V_{OFST} - V_{DROOP} \quad \text{(EQ. 5)}$$

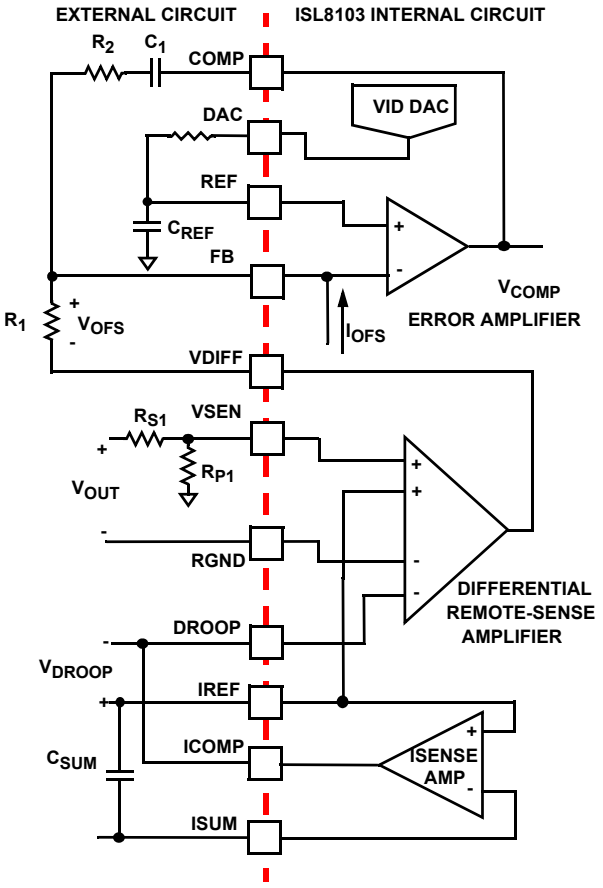


FIGURE 6. OUTPUT VOLTAGE AND LOAD-LINE REGULATION WITH OFFSET ADJUSTMENT

Load-Line (Droop) Regulation

In some high current applications, a requirement on a precisely controlled output impedance is imposed. This dependence of output voltage on load current is often termed “droop” or “load line” regulation.

The Droop is an optional feature in the ISL8103. It can be enabled by connecting ICOMP pin to DROOP pin as shown in Figure 6. To disable it, connect the DROOP pin to IREF pin.

As shown in Figure 6, a voltage, V_{DROOP}, proportional to the total current in all active channels, I_{OUT}, feeds into the differential remote-sense amplifier. The resulting voltage at the output of the remote-sense amplifier is the sum of the output voltage and the droop voltage. As Equation 4 shows, feeding this voltage into the compensation network causes the regulator to adjust the output voltage so that it’s equal to the reference voltage minus the droop voltage.

The droop voltage, V_{DROOP}, is created by sensing the current through the output inductors. This is accomplished by using a continuous DCR current sensing method.

Inductor windings have a characteristic distributed resistance or DCR (Direct Current Resistance). For simplicity, the inductor DCR is considered as a separate

lumped quantity, as shown in Figure 7. The channel current, I_L, flowing through the inductor, passes through the DCR. Equation 6 shows the s-domain equivalent voltage, V_L, across the inductor.

$$V_L(s) = I_L \cdot (s \cdot L + DCR) \quad \text{(EQ. 6)}$$

The inductor DCR is important because the voltage dropped across it is proportional to the channel current. By using a simple R-C network and a current sense amplifier, as shown in Figure 7, the voltage drop across all of the inductors DCRs can be extracted. The output of the current sense amplifier, V_{DROOP}, can be shown to be proportional to the channel currents I_{L1}, I_{L2}, and I_{L3}, shown in Equation 7.

$$V_{DROOP}(s) = \frac{\left(\frac{s \cdot L}{DCR} + 1\right)}{(s \cdot R_{COMP} \cdot C_{COMP} + 1)} \cdot \frac{R_{COMP}}{R_S} \cdot (I_{L1} + I_{L2} + I_{L3}) \cdot DCR \quad \text{(EQ. 7)}$$

If the R-C network components are selected such that the R-C time constant matches the inductor L/DCR time constant, then V_{DROOP} is equal to the sum of the voltage drops across the individual DCRs, multiplied by a gain. As Equation 8 shows, V_{DROOP} is therefore proportional to the total output current, I_{OUT}.

$$V_{DROOP} = \frac{R_{COMP}}{R_S} \cdot I_{OUT} \cdot DCR \quad \text{(EQ. 8)}$$

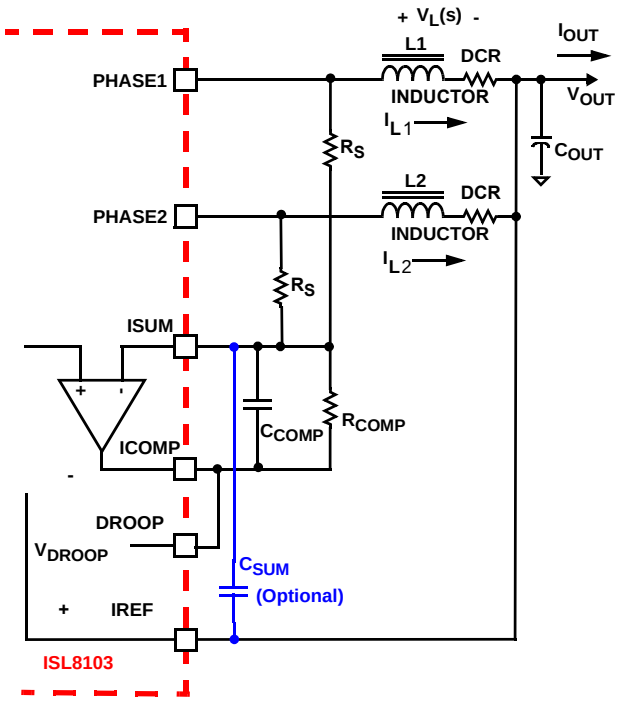


FIGURE 7. DCR SENSING CONFIGURATION

By simply adjusting the value of R_S, the load line can be set to any level, giving the converter the right amount of droop at all load currents. It may also be necessary to compensate for any changes in DCR due to temperature. These changes cause the load line to be skewed, and cause the R-C time constant to not match the L/DCR time constant. If this becomes a problem a simple negative temperature coefficient resistor network can be used in the place of R_{COMP} to compensate for the rise in DCR due to temperature.

Output Voltage Offset Programming

The ISL8103 allows the designer to accurately adjust the offset voltage by connecting a resistor, R_{OFS}, from the OFS pin to VCC or GND. When R_{OFS} is connected between OFS and VCC, the voltage across it is regulated to 1.5V. This causes a proportional current (I_{OFS}) to flow into the OFS pin and out of the FB pin. If R_{OFS} is connected to ground, the voltage across it is regulated to 0.5V, and I_{OFS} flows into the FB pin and out of the OFS pin. The offset current flowing through the resistor between VDIFF and FB will generate the desired offset voltage which is equal to the product (I_{OFS} x R_1). These functions are shown in Figures 8 and 9.

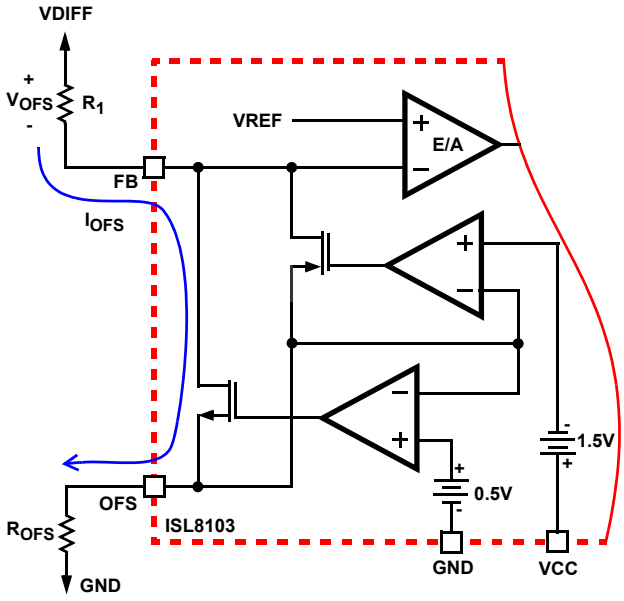


FIGURE 8. POSITIVE OFFSET OUTPUT VOLTAGE PROGRAMMING

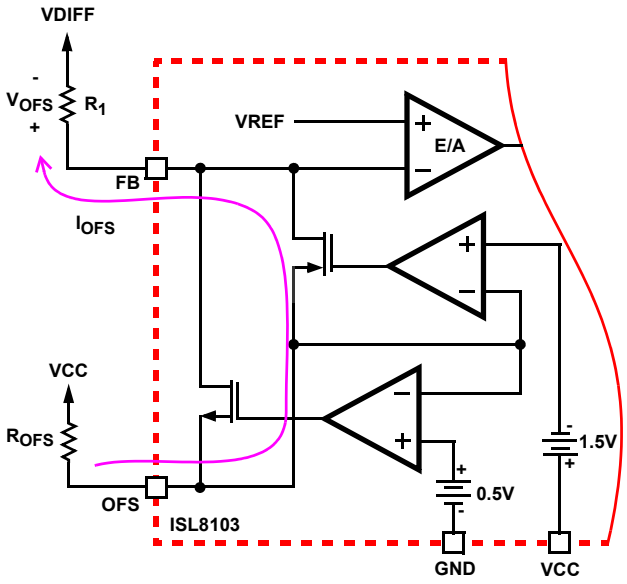


FIGURE 9. NEGATIVE OFFSET OUTPUT VOLTAGE PROGRAMMING

Once the desired output offset voltage has been determined, use the following formulas to set R_{OFS}:

For Positive Offset (connect R_{OFS} to GND):

$$R_{OFS} = \frac{0.5 \cdot R_1}{V_{OFFSET}} \quad \text{(EQ. 9)}$$

For Negative Offset (connect R_{OFS} to VCC):

$$R_{OFS} = \frac{1.5 \cdot R_1}{V_{OFFSET}} \quad \text{(EQ. 10)}$$

Advanced Adaptive Zero Shoot-Through Deadtime Control (Patent Pending)

The integrated drivers incorporate a unique adaptive deadtime control technique to minimize deadtime, resulting in high efficiency from the reduced freewheeling time of the lower MOSFET body-diode conduction, and to prevent the upper and lower MOSFETs from conducting simultaneously. This is accomplished by ensuring either rising gate turns on its MOSFET with minimum and sufficient delay after the other has turned off.

During turn-off of the lower MOSFET, the PHASE voltage is monitored until it reaches a -0.3V/+0.8V trip point for a forward/reverse current, at which time the UGATE is released to rise. An auto-zero comparator is used to correct the $r_{DS(ON)}$ drop in the phase voltage preventing false detection of the -0.3V phase level during $r_{DS(ON)}$ conduction period. In the case of zero current, the UGATE is released after 35ns delay of the LGATE dropping below 0.5V. During the phase detection, the disturbance of LGATE falling transition on the PHASE node is blanked out to prevent falsely tripping. Once the PHASE is high, the advanced adaptive shoot-through circuitry monitors the PHASE and UGATE voltages during a PWM falling edge and the subsequent UGATE turn-off. If either the UGATE falls to less than 1.75V above the PHASE or the PHASE falls to less than +0.8V, the LGATE is released to turn on.

Internal Bootstrap Device

All three integrated drivers feature an internal bootstrap schottky diode. Simply adding an external capacitor across the BOOT and PHASE pins completes the bootstrap circuit. The bootstrap function is also designed to prevent the bootstrap capacitor from overcharging due to the large negative swing at the PHASE node. This reduces voltage stress on the boot to phase pins.

The bootstrap capacitor must have a maximum voltage rating above PVCC + 5V and its capacitance value can be chosen from the following equation:

$$C_{BOOT\_CAP} \geq \frac{Q_{GATE}}{\Delta V_{BOOT\_CAP}} \quad \text{(EQ. 11)}$$

$$Q_{GATE} = \frac{Q_{G1} \cdot PVCC}{V_{GS1}} \cdot N_{Q1}$$

where Q_{G1} is the amount of gate charge per upper MOSFET at V_{GS1} gate-source voltage and N_{Q1} is the number of control MOSFETs. The ΔV_{BOOT_CAP} term is defined as the allowable droop in the rail of the upper gate drive. Figure 10 shows the boot capacitor ripple voltage as a function of boot capacitor value and total upper MOSFET gate charge.

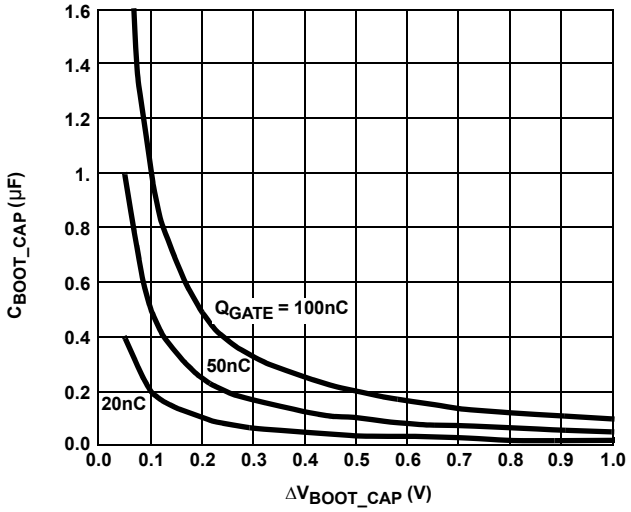


FIGURE 10. BOOTSTRAP CAPACITANCE vs BOOT RIPPLE VOLTAGE

Gate Drive Voltage Versatility

The ISL8103 provides the user flexibility in choosing the gate drive voltage for efficiency optimization. The controller ties the upper and lower drive rails together. Simply applying a voltage from 5V up to 12V on PVCC sets both gate drive rail voltages simultaneously.

Initialization

Prior to initialization, proper conditions must exist on the ENLL, VCC, PVCC and the REF0 and REF1 pins. When the conditions are met, the controller begins soft-start. Once the output voltage is within the proper window of operation, the controller asserts PGOOD.

Enable and Disable

While in shutdown mode, the PWM outputs are held in a high-impedance state to assure the drivers remain off. The following input conditions must be met before the ISL8103 is released from shutdown mode.

1. The bias voltage applied at VCC must reach the internal power-on reset (POR) rising threshold. Once this threshold is reached, proper operation of all aspects of the ISL8103 is guaranteed. Hysteresis between the rising and falling thresholds assure that once enabled, the ISL8103 will not inadvertently turn off unless the bias voltage drops substantially (see *Electrical Specifications*).

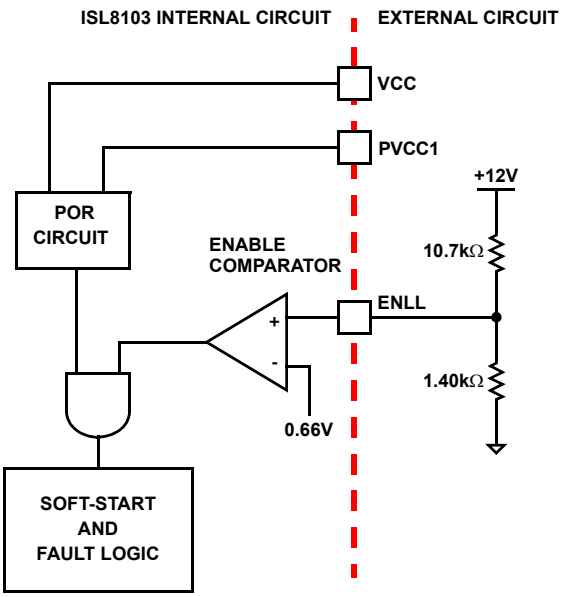


FIGURE 11. POWER SEQUENCING USING THRESHOLD-SENSITIVE ENABLE (ENLL) FUNCTION

2. The voltage on ENLL must be above 0.66V. The EN input allows for power sequencing between the controller bias voltage and another voltage rail. The enable comparator holds the ISL8103 in shutdown until the voltage at ENLL rises above 0.66V. The enable comparator has 100mV of hysteresis to prevent bounce.
3. The driver bias voltage applied at the PVCC pins must reach the internal power-on reset (POR) rising threshold. In order for the ISL8103 to begin operation, PVCC1 is the only pin that is required to have a voltage applied that exceeds POR. However, for 2 or 3-phase operation PVCC2 and PVCC3 must also exceed the POR threshold. Hysteresis between the rising and falling thresholds assure that once enabled, the ISL8103 will not inadvertently turn off unless the PVCC bias voltage drops substantially (see *Electrical Specifications*).

When each of these conditions is true, the controller immediately begins the soft-start sequence.

Soft-Start

During soft-start, the DAC voltage ramps linearly from zero to the programmed level. The PWM signals remain in the high-impedance state until the controller detects that the ramping DAC level has reached the output-voltage level. This protects the system against the large, negative inductor currents that would otherwise occur when starting with a pre-existing charge on the output as the controller attempted to regulate to zero volts at the beginning of the soft-start cycle. The Output soft-start time, T_{SS}, begins with a delay period equal to 64 switching cycles after the ENLL has exceeded its POR level, followed by a linear ramp with a rate determined by the switching period, $1/F_{sw}$.

$$T_{SS} = \frac{64 + DAC \cdot 1280}{F_{SW}} \quad \text{(EQ. 12)}$$

For example, a regulator with 450kHz switching frequency having REF voltage set to 1.2V has T_{SS} equal to 3.55ms.

A 100mV offset exists on the remote-sense amplifier at the beginning of soft-start and ramps to zero during the first 640 cycles of soft-start (704 cycles following enable). This prevents the large inrush current that would otherwise occur should the output voltage start out with a slight negative bias.

The ISL8103 also has the ability to start up into a pre-charged output as shown in Figure 12, without causing any unnecessary disturbance. The FB pin is monitored during soft-start, and should it be higher than the equivalent internal ramping reference voltage, the output drives hold both MOSFETs off. Once the internal ramping reference exceeds the FB pin potential, the output drives are enabled, allowing the output to ramp from the pre-charged level to the final level dictated by the reference setting. Should the output be pre-charged to a level exceeding the reference setting, the output drives are enabled at the end of the soft-start period, leading to an abrupt correction in the output voltage down to the “reference set” level.

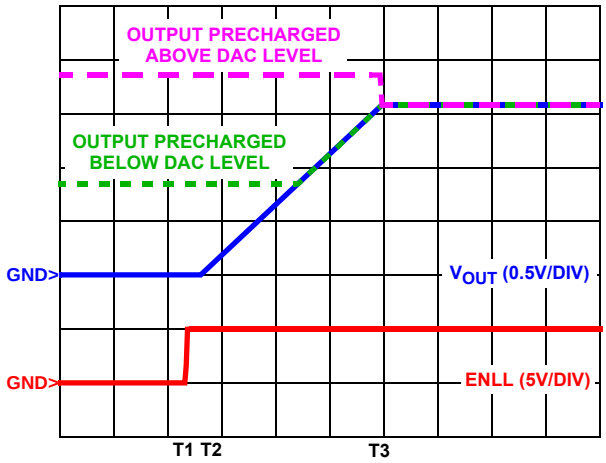


FIGURE 12. SOFT-START WAVEFORMS FOR ISL8103-BASED MULTI-PHASE CONVERTER

Fault Monitoring and Protection

The ISL8103 actively monitors output voltage and current to detect fault conditions. Fault monitors trigger protective measures to prevent damage to the load.

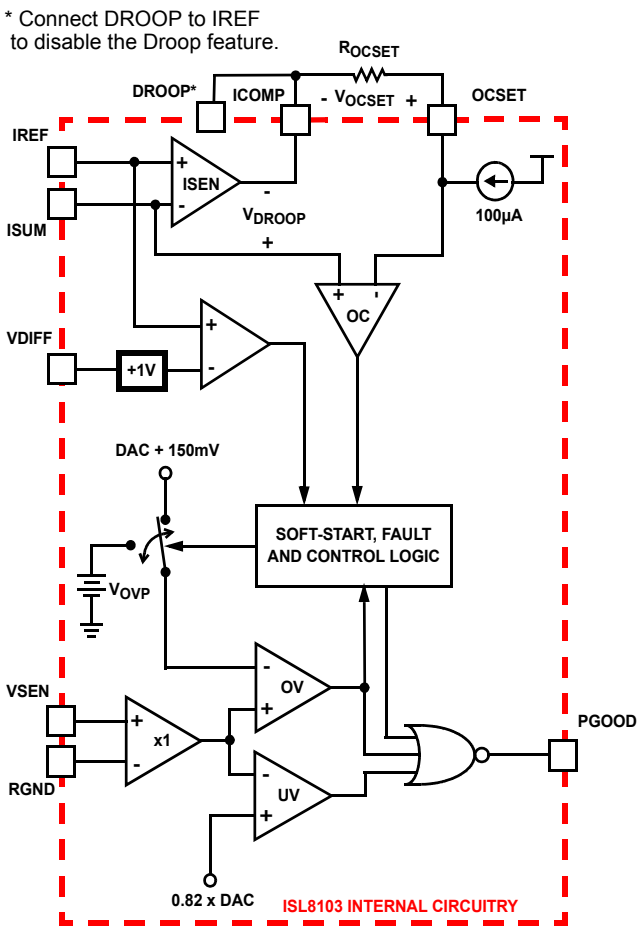


FIGURE 13. POWER GOOD AND PROTECTION CIRCUITRY

One common power good indicator is provided for linking to external system monitors. The schematic in Figure 13 outlines the interaction between the fault monitors and the power good signal

Power Good Signal

The power good pin (PGOOD) is an open-drain logic output that transitions high when the converter is operating after soft-start. PGOOD pulls low during shutdown and releases high after a successful soft-start. PGOOD transitions low when an undervoltage, overvoltage, or overcurrent condition is detected or when the controller is disabled by a reset from ENLL or POR. If after an undervoltage or overvoltage event occurs the output returns to within under and overvoltage limits, PGOOD will return high.

Undervoltage Detection

The undervoltage threshold is set at 82% of the REF voltage. When the output voltage (VSEN-RGND) is below the undervoltage threshold, PGOOD gets pulled low. No other action is taken by the controller. PGOOD will return high if the output voltage rises above 85% of the REF voltage.

Overvoltage Protection

The ISL8103 constantly monitors the difference between the VSEN and RGND voltages to detect if an overvoltage event occurs. During soft-start, while the DAC/REF is ramping up, the overvoltage trip level is the higher of REF plus 150mV or a fixed voltage, V_{OVP}. The fixed voltage, V_{OVP}, is 1.67V. Upon successful soft-start, the overvoltage trip level is only REF plus 150mV. OVP releases 50mV below its trip point if it was “REF plus 150mV” that tripped it, and releases 100mV below its trip point if it was the fixed voltage, V_{OVP}, that tripped it. Actions are taken by the ISL8103 to protect the load when an overvoltage condition occurs, until the output voltage falls back within set limits.

At the inception of an overvoltage event, all LGATE signals are commanded high, and the PGOOD signal is driven low. This causes the controller to turn on the lower MOSFETs and pull the output voltage below a level that might cause damage to the load. The LGATE outputs remain high until VDIFF falls to within the overvoltage limits explained above. The ISL8103 will continue to protect the load in this fashion as long as the overvoltage condition recurs.

Once an overvoltage condition ends the ISL8103 continues normal operation and PGOOD returns high.

Pre-POR Overvoltage Protection

Prior to PVCC and VCC exceeding their POR levels, the ISL8103 is designed to protect the load from any overvoltage events that may occur. This is accomplished by means of an internal 10kΩ resistor tied from PHASE to LGATE, which turns on the lower MOSFET to control the output voltage until the overvoltage event ceases or the input power supply cuts off. For complete protection, the low side MOSFET

should have a gate threshold well below the maximum voltage rating of the load/microprocessor.

In the event that during normal operation the PVCC or VCC voltage falls back below the POR threshold, the pre-POR overvoltage protection circuitry reactivates to protect from any more pre-POR overvoltage events.

Open Sense Line Protection

In the case that either of the remote sense lines, VSEN or GND, become open, the ISL8103 is designed to detect this and shut down the controller. This event is detected by monitoring the voltage on the IREF pin, which is a local version of V_{OUT} sensed at the outputs of the inductors.

If VSEN or RGND become opened, VDIFF falls, causing the duty cycle to increase and the output voltage on IREF to increase. If the voltage on IREF exceeds “VDIFF+1V”, the controller will shut down. Once the voltage on IREF falls below “VDIFF+1V”, the ISL8103 will restart at the beginning of soft-start.

Overcurrent Protection

The ISL8103 detects overcurrent events by comparing the droop voltage, V_{DROOP}, to the OCSET voltage, V_{OCSET}, as shown in Figure 13. The droop voltage, set by the external current sensing circuitry, is proportional to the output current as shown in Equation 8. A constant 100µA flows through R_{OCSET}, creating the OCSET voltage. When the droop voltage exceeds the OCSET voltage, the overcurrent protection circuitry activates. Since the droop voltage is proportional to the output current, the overcurrent trip level, I_{MAX}, can be set by selecting the proper value for R_{OCSET}, as shown in Equation 13.

$$R_{OCSET} = \frac{I_{MAX} \cdot R_{COMP} \cdot DCR}{100\mu A \cdot R_S} \quad \text{(EQ. 13)}$$

Once the output current exceeds the overcurrent trip level, V_{DROOP} will exceed V_{OCSET}, and a comparator will trigger the converter to begin overcurrent protection procedures. At the beginning of overcurrent shutdown, the controller turns off both upper and lower MOSFETs. The system remains in this state for a period of 4096 switching cycles. If the controller is still enabled at the end of this wait period, it will attempt a soft-start (as shown in Figure 14). If the fault remains, the trip-retry cycles will continue indefinitely until either the controller is disabled or the fault is cleared. Note that the energy delivered during trip-retry cycling is much less than during full-load operation, so there is no thermal hazard.

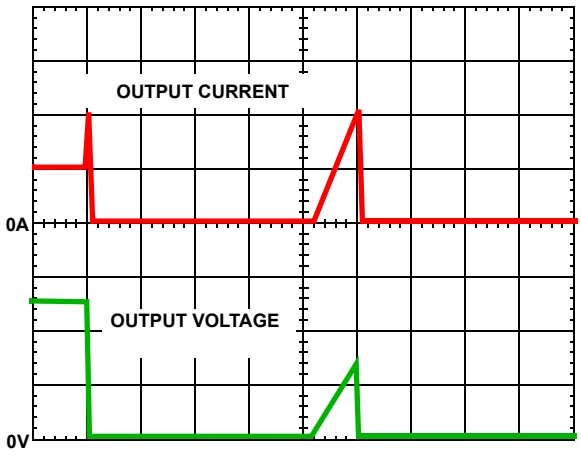


FIGURE 14. OVERCURRENT BEHAVIOR IN HICCUP MODE

General Design Guide

This design guide is intended to provide a high-level explanation of the steps necessary to create a multi-phase power converter. It is assumed that the reader is familiar with many of the basic skills and techniques referenced below. In addition to this guide, Intersil provides complete reference designs that include schematics, bills of materials, and example board layouts for many applications.

Power Stages

The first step in designing a multi-phase converter is to determine the number of phases. This determination depends heavily on the cost analysis which in turn depends on system constraints that differ from one design to the next. Principally, the designer will be concerned with whether components can be mounted on both sides of the circuit board, whether through-hole components are permitted, the total board space available for power-supply circuitry, and the maximum amount of load current. Generally speaking, the most economical solutions are those in which each phase handles between 25 and 30A. All surface-mount designs will tend toward the lower end of this current range. If through-hole MOSFETs and inductors can be used, higher per-phase currents are possible. In cases where board space is the limiting constraint, current can be pushed as high as 40A per phase, but these designs require heat sinks and forced air to cool the MOSFETs, inductors and heat-dissipating surfaces.

MOSFETs

The choice of MOSFETs depends on the current each MOSFET will be required to conduct, the switching frequency, the capability of the MOSFETs to dissipate heat, and the availability and nature of heat sinking and air flow.

LOWER MOSFET POWER CALCULATION

The calculation for the approximate power loss in the lower MOSFET can be simplified, since virtually all of the loss in the lower MOSFET is due to current conducted through the channel resistance ($r_{DS(ON)}$). In Equation 14, I_M is the maximum continuous output current, I_{PP} is the peak-to-peak inductor current (see Equation 1), and d is the duty cycle (V_{OUT}/V_{IN}).

$$P_{LOW,1} = r_{DS(ON)} \cdot \left[\left(\frac{I_M}{N}\right)^2 \cdot (1-d) + \frac{I_{L,PP}^2 \cdot (1-d)}{12}\right] \quad \text{(EQ. 14)}$$

An additional term can be added to the lower-MOSFET loss equation to account for additional loss accrued during the dead time when inductor current is flowing through the lower-MOSFET body diode. This term is dependent on the diode forward voltage at I_M, $V_{D(ON)}$, the switching frequency, F_{SW}, and the length of dead times, t_{d1} and t_{d2}, at the beginning and the end of the lower-MOSFET conduction interval respectively.

$$P_{LOW,2} = V_{D(ON)} \cdot F_{SW} \cdot \left[\left(\frac{I_M}{N} + \frac{I_{PP}}{2}\right) \cdot t_{d1} + \left(\frac{I_M}{N} - \frac{I_{PP}}{2}\right) \cdot t_{d2}\right] \quad \text{(EQ. 15)}$$

The total maximum power dissipated in each lower MOSFET is approximated by the summation of $P_{LOW,1}$ and $P_{LOW,2}$.

UPPER MOSFET POWER CALCULATION

In addition to $r_{DS(ON)}$ losses, a large portion of the upper-MOSFET losses are due to currents conducted across the input voltage (V_{IN}) during switching. Since a substantially higher portion of the upper-MOSFET losses are dependent on switching frequency, the power calculation is more complex. Upper MOSFET losses can be divided into separate components involving the upper-MOSFET switching times, the lower-MOSFET body-diode reverse-recovery charge, Q_{rr}, and the upper MOSFET $r_{DS(ON)}$ conduction loss.

When the upper MOSFET turns off, the lower MOSFET does not conduct any portion of the inductor current until the voltage at the phase node falls below ground. Once the lower MOSFET begins conducting, the current in the upper MOSFET falls to zero as the current in the lower MOSFET ramps up to assume the full inductor current. In Equation 16, the required time for this commutation is t_1 and the approximated associated power loss is $P_{UP,1}$.

$$P_{UP,1} \approx V_{IN} \cdot \left(\frac{I_M}{N} + \frac{I_{PP}}{2}\right) \cdot \left(\frac{t_1}{2}\right) \cdot F_{SW} \quad \text{(EQ. 16)}$$

At turn on, the upper MOSFET begins to conduct and this transition occurs over a time t_2. In Equation 17, the approximate power loss is $P_{UP,2}$.

$$P_{UP,2} \approx V_{IN} \cdot \left(\frac{I_M}{N} - \frac{I_{PP}}{2}\right) \cdot \left(\frac{t_2}{2}\right) \cdot F_{SW} \quad \text{(EQ. 17)}$$

A third component involves the lower MOSFET reverse-recovery charge, Q_{rr}. Since the inductor current has fully commutated to the upper MOSFET before the lower-MOSFET body diode can recover all of Q_{rr}, it is conducted through the upper MOSFET across V_{IN}. The power dissipated as a result is $P_{UP,3}$.

$$P_{UP,3} = V_{IN} \cdot Q_{rr} \cdot F_{SW} \quad \text{(EQ. 18)}$$

Finally, the resistive part of the upper MOSFET is given in Equation 19 as $P_{UP,4}$.

$$P_{UP,4} \approx r_{DS(ON)} \cdot \left[\left(\frac{I_M}{N}\right)^2 \cdot d + \frac{I_{PP}^2}{12}\right] \quad \text{(EQ. 19)}$$

The total power dissipated by the upper MOSFET at full load can now be approximated as the summation of the results from Equations 16, 17, 18 and 19. Since the power equations depend on MOSFET parameters, choosing the correct MOSFETs can be an iterative process involving repetitive solutions to the loss equations for different MOSFETs and different switching frequencies.

Package Power Dissipation

When choosing MOSFETs it is important to consider the amount of power being dissipated in the integrated drivers located in the controller. Since there are a total of three drivers in the controller package, the total power dissipated by all three drivers must be less than the maximum allowable power dissipation for the QFN package.

Calculating the power dissipation in the drivers for a desired application is critical to ensure safe operation. Exceeding the maximum allowable power dissipation level will push the IC beyond the maximum recommended operating junction temperature of 125°C. The maximum allowable IC power dissipation for the 6x6 QFN package is approximately 4W at room temperature. See *Layout Considerations* paragraph for thermal transfer improvement suggestions.

When designing the ISL8103 into an application, it is recommended that the following calculation is used to ensure safe operation at the desired frequency for the selected MOSFETs. The total gate drive power losses, P_{Qg_TOT}, due to the gate charge of MOSFETs and the integrated driver's internal circuitry and their corresponding average driver current can be estimated with Equations 20 and 21, respectively.

$$P_{Qg\_TOT} = P_{Qg\_Q1} + P_{Qg\_Q2} + I_Q \cdot VCC \quad \text{(EQ. 20)}$$

$$P_{Qg\_Q1} = \frac{3}{2} \cdot Q_{G1} \cdot PVCC \cdot F_{SW} \cdot N_{Q1} \cdot N_{PHASE}$$

$$P_{Qg\_Q2} = Q_{G2} \cdot PVCC \cdot F_{SW} \cdot N_{Q2} \cdot N_{PHASE}$$

$$I_{DR} = \left(\frac{3}{2} \bullet Q_{G1} \bullet N_{Q1} + Q_{G2} \bullet N_{Q2}\right) \bullet N_{PHASE} \bullet F_{SW} + I_Q \quad \text{(EQ. 21)}$$

In Equations 20 and 21, P_{Qg_Q1} is the total upper gate drive power loss and P_{Qg_Q2} is the total lower gate drive power loss; the gate charge (Q_{G1} and Q_{G2}) is defined at the particular gate to source drive voltage PVCC in the corresponding MOSFET data sheet; I_Q is the driver total quiescent current with no load at both drive outputs; N_{Q1} and N_{Q2} are the number of upper and lower MOSFETs per phase, respectively; N_{PHASE} is the number of active phases. The I_Q*VCC product is the quiescent power of the controller without capacitive load and is typically 75mW at 300kHz.

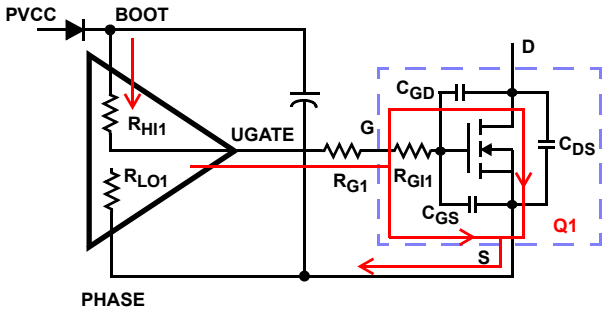


FIGURE 15. TYPICAL UPPER-GATE DRIVE TURN-ON PATH

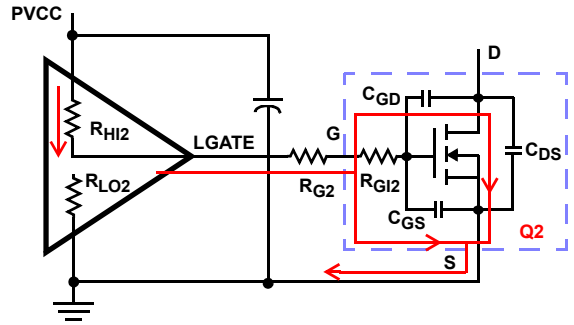


FIGURE 16. TYPICAL LOWER-GATE DRIVE TURN-ON PATH

The total gate drive power losses are dissipated among the resistive components along the transition path and in the bootstrap diode. The portion of the total power dissipated in the controller itself is the power dissipated in the upper drive path resistance, P_{DR_UP}, the lower drive path resistance, P_{DR_UP}, and in the boot strap diode, P_{BOOT}. The rest of the power will be dissipated by the external gate resistors (R_{G1} and R_{G2}) and the internal gate resistors (R_{GI1} and R_{GI2}) of the MOSFETs. Figures 15 and 16 show the typical upper and lower gate drives turn-on transition path. The total power dissipation in the controller itself, P_{DR}, can be roughly estimated as:

$$P_{DR} = P_{DR\_UP} + P_{DR\_LOW} + P_{BOOT} + (I_Q \bullet VCC) \quad \text{(EQ. 22)}$$

$$P_{BOOT} = \frac{P_{Qg\_Q1}}{3}$$

$$P_{DR\_UP} = \left(\frac{R_{HI1}}{R_{HI1} + R_{EXT1}} + \frac{R_{LO1}}{R_{LO1} + R_{EXT1}}\right) \bullet \frac{P_{Qg\_Q1}}{3}$$

$$P_{DR\_LOW} = \left(\frac{R_{HI2}}{R_{HI2} + R_{EXT2}} + \frac{R_{LO2}}{R_{LO2} + R_{EXT2}}\right) \bullet \frac{P_{Qg\_Q2}}{2}$$

$$R_{EXT1} = R_{G1} + \frac{R_{GI1}}{N_{Q1}} \qquad R_{EXT2} = R_{G2} + \frac{R_{GI2}}{N_{Q2}}$$

Current Balancing Component Selection

The ISL8103 senses the channel load current by sampling the voltage across the lower MOSFET $r_{DS(ON)}$, as shown in Figure 17. The ISEN pins are denoted ISEN1, ISEN2, and ISEN3. The resistors connected between these pins and the respective phase nodes determine the gains in the channel current balance loop.

Select values for these resistors based on the room temperature $r_{DS(ON)}$ of the lower MOSFETs; the full load operating current, I_{FL}; and the number of phases, N using Equation 23.

$$R_{ISEN} = \frac{r_{DS(ON)}}{50 \cdot 10^{-6}} \cdot \frac{I_{FL}}{N} \quad \text{(EQ. 23)}$$

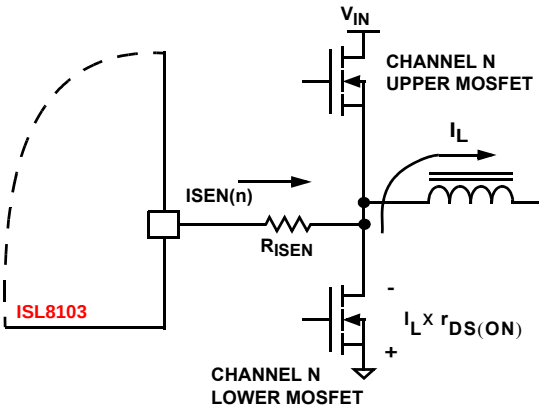


FIGURE 17. ISL8103 INTERNAL AND EXTERNAL CURRENT-SENSING CIRCUITRY

In certain circumstances, it may be necessary to adjust the value of one or more ISEN resistors. When the components of one or more channels are inhibited from effectively

dissipating their heat so that the affected channels run hotter than desired, choose new, smaller values of R_{ISEN} for the affected phases (see the section entitled Channel Current Balance). Choose $R_{ISEN,2}$ in proportion to the desired decrease in temperature rise in order to cause proportionally less current to flow in the hotter phase.

$$R_{ISEN,2} = R_{ISEN} \cdot \frac{\Delta T_2}{\Delta T_1} \quad \text{(EQ. 24)}$$

In Equation 24, make sure that ΔT_2 is the desired temperature rise above the ambient temperature, and ΔT_1 is the measured temperature rise above the ambient temperature. While a single adjustment according to Equation 24 is usually sufficient, it may occasionally be necessary to adjust R_{ISEN} two or more times to achieve optimal thermal balance between all channels.

Load Line Regulation Component Selection (DCR Current Sensing)

For accurate load line regulation, the ISL8103 senses the total output current by detecting the voltage across the output inductor DCR of each channel (As described in the *Load Line Regulation* section). As Figure 7 illustrates, an R-C network is required to accurately sense the inductor DCR voltage and convert this information into a droop voltage, which is proportional to the total output current.

Choosing the components for this current sense network is a two step process. First, R_{COMP} and C_{COMP} must be chosen so that the time constant of this R_{COMP}-C_{COMP} network matches the time constant of the inductor L/DCR. Then the resistor R_S must be chosen to set the current sense network gain, obtaining the desired full load droop voltage. Follow the steps below to choose the component values for this R-C network.

1. Choose an arbitrary value for C_{COMP}. The recommended value is 0.01µF.
2. Plug the inductor L and DCR component values, and the values for C_{COMP} chosen in steps 1, into Equation 25 to calculate the value for R_{COMP}.

$$R_{COMP} = \frac{L}{DCR \cdot C_{COMP}} \quad \text{(EQ. 25)}$$

3. Use the new value for R_{COMP} obtained from Equation 25, as well as the desired full load current, I_{FL}, full load droop voltage, V_{DROOP}, and inductor DCR in Equation 26 to calculate the value for R_S.

$$R_S = \frac{I_{FL}}{V_{DROOP}} \cdot R_{COMP} \cdot DCR \quad \text{(EQ. 26)}$$

Due to errors in the inductance or DCR it may be necessary to adjust the value of R_{COMP} to match the time constants correctly. The effects of time constant mismatch can be seen in the form of droop overshoot or undershoot during the initial load transient spike, as shown in Figure 18. Follow the steps below to ensure the R-C and inductor L/DCR time constants are matched accurately.

1. Capture a transient event with the oscilloscope set to about L/DCR/2 (sec/div). For example, with L = 1µH and DCR = 1mΩ, set the oscilloscope to 500µs/div.
2. Record ΔV1 and ΔV2 as shown in Figure 18.
3. Select a new value, $R_{COMP,2}$, for the time constant resistor based on the original value, $R_{COMP,1}$, using the following equation.

$$R_{COMP,2} = R_{COMP,1} \cdot \frac{\Delta V_1}{\Delta V_2} \quad \text{(EQ. 27)}$$

4. Replace R_{COMP} with the new value and check to see that the error is corrected. Repeat the procedure if necessary.

After choosing a new value for R_{COMP}, it will most likely be necessary to adjust the value of R_S to obtain the desired full load droop voltage. Use Equation 26 to obtain the new value for R_S.

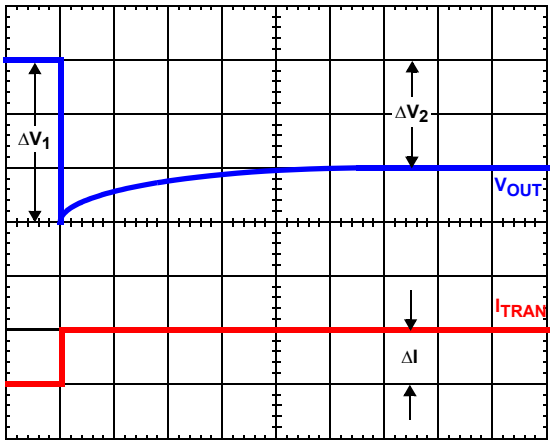


FIGURE 18. TIME CONSTANT MISMATCH BEHAVIOR

Compensation

The two opposing goals of compensating the voltage regulator are stability and speed. Depending on whether the regulator employs the optional load-line regulation as described in "*Load-Line Regulation*", there are two distinct methods for achieving these goals.

Compensating the Load-Line Regulated Converter

The load-line regulated converter behaves in a similar manner to a peak current mode controller because the two poles at the output filter L-C resonant frequency split with the introduction of current information into the control loop. The final location of these poles is determined by the system function, the gain of the current signal, and the value of the compensation components, R_2 and C_1.

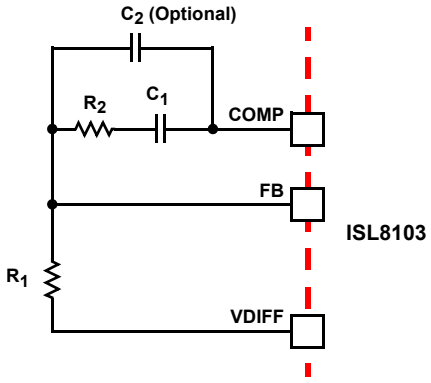


FIGURE 19. COMPENSATION CONFIGURATION FOR LOAD-LINE REGULATED ISL8103 CIRCUIT

Since the system poles and zero are affected by the values of the components that are meant to compensate them, the solution to the system equation becomes fairly complicated. Fortunately, there is a simple approximation that comes very close to an optimal solution. Treating the system as though it were a voltage-mode regulator, by compensating the L-C poles and the ESR zero of the voltage mode approximation, yields a solution that is always stable with very close to ideal transient performance.

The feedback resistor, R_1, has already been chosen as outlined in *Load-Line Regulation Resistor.* Select a target bandwidth for the compensated system, F_0. The target bandwidth must be large enough to assure adequate transient performance, but smaller than 1/3 of the per-channel switching frequency. The values of the compensation components depend on the relationships of F_0 to the L-C double pole frequency and the ESR zero frequency. For each of the following three, there is a separate set of equations for the compensation components.

Case 1: $$\frac{1}{2\pi \cdot \sqrt{L \cdot C}} > F_0$$

$$R_2 = R_1 \cdot \frac{2\pi \cdot F_0 \cdot V_{OSC} \cdot \sqrt{L \cdot C}}{0.66 \cdot V_{IN}}$$

$$C_1 = \frac{0.66 \cdot V_{IN}}{2\pi \cdot V_{OSC} \cdot R_1 \cdot f_0}$$

Case 2: $$\frac{1}{2\pi \cdot \sqrt{L \cdot C}} \leq F_0 < \frac{1}{2\pi \cdot C \cdot ESR}$$

$$R_2 = R_1 \cdot \frac{V_{OSC} \cdot (2\pi)^2 \cdot F_0^2 \cdot L \cdot C}{0.66 \cdot V_{IN}} \qquad \text{(EQ. 28)}$$

$$C_1 = \frac{0.66 \cdot V_{IN}}{(2\pi)^2 \cdot F_0^2 \cdot V_{OSC} \cdot R_1 \cdot \sqrt{L \cdot C}}$$

Case 3: $$F_0 > \frac{1}{2\pi \cdot C \cdot ESR}$$

$$R_2 = R_1 \cdot \frac{2\pi \cdot F_0 \cdot V_{OSC} \cdot L}{0.66 \cdot V_{IN} \cdot ESR}$$

$$C_2 = \frac{0.66 \cdot V_{IN} \cdot ESR \cdot \sqrt{C}}{2\pi \cdot V_{OSC} \cdot R_1 \cdot F_0 \cdot \sqrt{L}}$$

In Equations 28, L is the per-channel filter inductance divided by the number of active channels; C is the sum total of all output capacitors; ESR is the equivalent series resistance of the bulk output filter capacitance; and V_{PP} is the peak-to-peak sawtooth signal amplitude as described in the *Electrical Specifications*.

Once selected, the compensation values in Equations 28 assure a stable converter with reasonable transient performance. In most cases, transient performance can be improved by making adjustments to R_2. Slowly increase the value of R_2 while observing the transient performance on an oscilloscope until no further improvement is noted. Normally, C_1 will not need adjustment. Keep the value of C_1 from Equations 28 unless some performance issue is noted.

The optional capacitor C_2, is sometimes needed to bypass noise away from the PWM comparator (see Figure 19). Keep a position available for C_2, and be prepared to install a high frequency capacitor of between 22pF and 150pF in case any leading edge jitter problem is noted.

Compensating the Converter operating without Load-Line Regulation

The ISL8103 multi-phase converter operating without load line regulation behaves in a similar manner to a voltage-mode controller. This section highlights the design consideration for a voltage-mode controller requiring external compensation. To address a broad range of applications, a type-3 feedback network is recommended (see Figure 20).

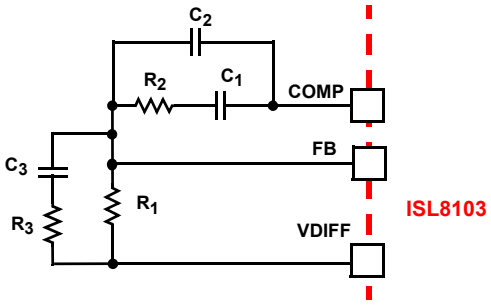


FIGURE 20. COMPENSATION CONFIGURATION FOR NON-LOAD-LINE REGULATED ISL8103 CIRCUIT

Figure 21 highlights the voltage-mode control loop for a synchronous-rectified buck converter, applicable, with a small number of adjustments, to the multi-phase ISL8103 circuit. The output voltage (V_{OUT}) is regulated to the reference voltage, VREF, level. The error amplifier output (COMP pin voltage) is compared with the oscillator (OSC) modified saw-tooth wave to provide a pulse-width modulated wave with an amplitude of V_{IN} at the PHASE node. The PWM wave is smoothed by the output filter (L and C). The output filter capacitor bank's equivalent series resistance is represented by the series resistor E.

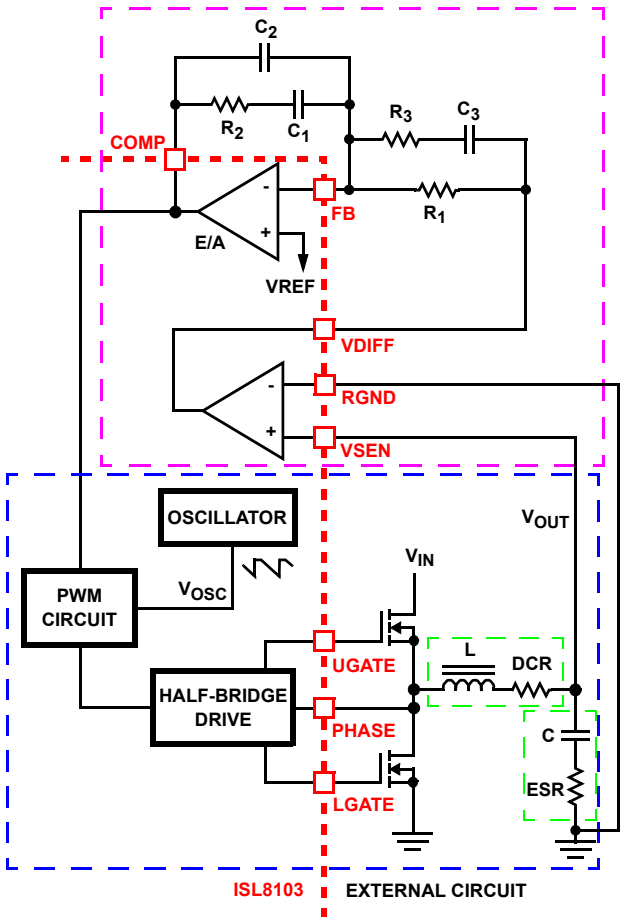


FIGURE 21. VOLTAGE-MODE BUCK CONVERTER COMPENSATION DESIGN

The modulator transfer function is the small-signal transfer function of V_{OUT}/V_{COMP}. This function is dominated by a DC gain, given by $d_{MAX}V_{IN}/V_{OSC}$, and shaped by the output filter, with a double pole break frequency at F_{LC} and a zero at F_{CE}. For the purpose of this analysis, L and DCR represent the individual channel inductance and its DCR divided by 3 (equivalent parallel value of the three output inductors), while C and ESR represents the total output capacitance and its equivalent series resistance.

$$F_{LC} = \frac{1}{2\pi \cdot \sqrt{L \cdot C}} \qquad F_{CE} = \frac{1}{2\pi \cdot C \cdot ESR}$$

The compensation network consists of the error amplifier (internal to the ISL8103) and the external R_1-R_3, C_1-C_3 components. The goal of the compensation network is to provide a closed loop transfer function with high 0dB crossing frequency (F_0; typically 0.1 to 0.3 of F_{SW}) and adequate phase margin (better than 45 degrees). Phase margin is the difference between the closed loop phase at F_{0dB} and 180°. The equations that follow relate the compensation network's poles, zeros and gain to the components (R_1, R_2, R_3, C_1, C_2, and C_3) in Figure 20 and 21. Use the following guidelines for locating the poles and zeros of the compensation network:

1. Select a value for R_1 (1kΩ to 5kΩ, typically). Calculate value for R_2 for desired converter bandwidth (F_0).

$$R_2 = \frac{V_{OSC} \cdot R_1 \cdot F_0}{d_{MAX} \cdot V_{IN} \cdot F_{LC}}$$

If setting the output voltage to be equal to the reference set voltage as shown in Figure 21, the design procedure can be followed as presented. However, when setting the output voltage via a resistor divider placed at the input of the differential amplifier (as shown in Figure 6), in order to compensate for the attenuation introduced by the resistor divider, the obtained R_2 value needs be multiplied by a factor of $(R_P+R_S)/R_P$. The remainder of the calculations remain unchanged, as long as the compensated R_2 value is used.

2. Calculate C_1 such that F_{Z1} is placed at a fraction of the F_{LC}, at 0.1 to 0.75 of F_{LC} (to adjust, change the 0.5 factor to desired number). The higher the quality factor of the output filter and/or the higher the ratio F_{CE}/F_{LC}, the lower the F_{Z1} frequency (to maximize phase boost at F_{LC}).

$$C_1 = \frac{1}{2\pi \cdot R_2 \cdot 0.5 \cdot F_{LC}}$$

3. Calculate C_2 such that F_{P1} is placed at F_{CE}.

$$C_2 = \frac{C_1}{2\pi \cdot R_2 \cdot C_1 \cdot F_{CE} - 1}$$

4. Calculate R_3 such that F_{Z2} is placed at F_{LC}. Calculate C_3 such that F_{P2} is placed below F_{SW} (typically, 0.5 to 1.0 times F_{SW}). F_{SW} represents the per-channel switching frequency. Change the numerical factor to reflect desired placement of this pole. Placement of F_{P2} lower in frequency helps reduce the gain of the compensation network at high frequency, in turn reducing the HF ripple component at the COMP pin and minimizing resultant duty cycle jitter.

$$R_3 = \frac{R_1}{\frac{F_{SW}}{F_{LC}} - 1}$$

$$C_3 = \frac{1}{2\pi \cdot R_3 \cdot 0.7 \cdot F_{SW}}$$

It is recommended a mathematical model is used to plot the loop response. Check the loop gain against the error amplifier's open-loop gain. Verify phase margin results and adjust as necessary. The following equations describe the frequency response of the modulator (G_{MOD}), feedback compensation (G_{FB}) and closed-loop response (G_{CL}):

$$G_{MOD}(f) = \frac{d_{MAX} \cdot V_{IN}}{V_{OSC}} \cdot \frac{1 + s(f) \cdot ESR \cdot C}{1 + s(f) \cdot (ESR + DCR) \cdot C + s^2(f) \cdot L \cdot C}$$

$$G_{FB}(f) = \frac{1 + s(f) \cdot R_2 \cdot C_1}{s(f) \cdot R_1 \cdot (C_1 + C_2)} \cdot \frac{1 + s(f) \cdot (R_1 + R_3) \cdot C_3}{(1 + s(f) \cdot R_3 \cdot C_3) \cdot \left(1 + s(f) \cdot R_2 \cdot \left(\frac{C_1 \cdot C_2}{C_1 + C_2}\right)\right)}$$

$$G_{CL}(f) = G_{MOD}(f) \cdot G_{FB}(f) \qquad \text{where, } s(f) = 2\pi \cdot f \cdot j$$

COMPENSATION BREAK FREQUENCY EQUATIONS

$$F_{Z1} = \frac{1}{2\pi \cdot R_2 \cdot C_1} \qquad F_{P1} = \frac{1}{2\pi \cdot R_2 \cdot \frac{C_1 \cdot C_2}{C_1 + C_2}}$$

$$F_{Z2} = \frac{1}{2\pi \cdot (R_1 + R_3) \cdot C_3} \qquad F_{P2} = \frac{1}{2\pi \cdot R_3 \cdot C_3}$$

Figure 22 shows an asymptotic plot of the DC/DC converter's gain vs. frequency. The actual Modulator Gain has a high gain peak dependent on the quality factor (Q) of the output filter, which is not shown. Using the above guidelines should yield a compensation gain similar to the curve plotted. The open loop error amplifier gain bounds the compensation gain. Check the compensation gain at F_{P2} against the capabilities of the error amplifier. The closed loop gain, G_{CL}, is constructed on the log-log graph of Figure 22 by adding the modulator gain, G_{MOD} (in dB), to the feedback compensation gain, G_{FB} (in dB). This is equivalent to multiplying the modulator transfer function and the compensation transfer function and then plotting the resulting gain.

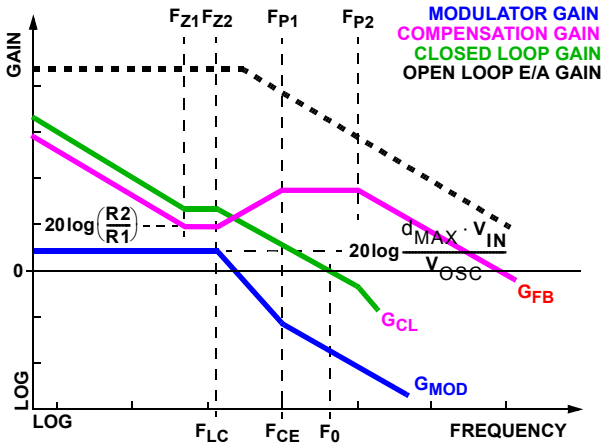


FIGURE 22. ASYMPTOTIC BODE PLOT OF CONVERTER GAIN

A stable control loop has a gain crossing with close to a -20dB/decade slope and a phase margin greater than 45 degrees. Include worst case component variations when determining phase margin. The mathematical model presented makes a number of approximations and is generally not accurate at frequencies approaching or exceeding half the switching frequency. When designing compensation networks, select target crossover frequencies in the range of 10% to 30% of the per-channel switching frequency, F_{SW}.

Output Filter Design

The output inductors and the output capacitor bank together to form a low-pass filter responsible for smoothing the pulsating voltage at the phase nodes. The output filter also must provide the transient energy until the regulator can respond. Because it has a low bandwidth compared to the switching frequency, the output filter limits the system transient response. The output capacitors must supply or sink load current while the current in the output inductors increases or decreases to meet the demand.

In high-speed converters, the output capacitor bank is usually the most costly (and often the largest) part of the circuit. Output filter design begins with minimizing the cost of this part of the circuit. The critical load parameters in choosing the output capacitors are the maximum size of the load step, ΔI, the load-current slew rate, di/dt, and the maximum allowable output-voltage deviation under transient loading, ΔV_{MAX}. Capacitors are characterized according to their capacitance, ESR, and ESL (equivalent series inductance).

At the beginning of the load transient, the output capacitors supply all of the transient current. The output voltage will initially deviate by an amount approximated by the voltage drop across the ESL. As the load current increases, the voltage drop across the ESR increases linearly until the load current reaches its final value. The capacitors selected must have sufficiently low ESL and ESR so that the total output-voltage deviation is less than the allowable maximum. Neglecting the contribution of inductor current and regulator response, the output voltage initially deviates by an amount

$$\Delta V \approx (ESL) \cdot \frac{di}{dt} + (ESR) \cdot \Delta I \qquad \text{(EQ. 29)}$$

The filter capacitor must have sufficiently low ESL and ESR so that $\Delta V < \Delta V_{MAX}$.

Most capacitor solutions rely on a mixture of high frequency capacitors with relatively low capacitance in combination with bulk capacitors having high capacitance but limited high-frequency performance. Minimizing the ESL of the high-frequency capacitors allows them to support the output voltage as the current increases. Minimizing the ESR of the bulk capacitors allows them to supply the increased current with less output voltage deviation.

The ESR of the bulk capacitors also creates the majority of the output-voltage ripple. As the bulk capacitors sink and source the inductor ac ripple current (see *Interleaving* and Equation 2), a voltage develops across the bulk capacitor ESR equal to $I_{C,PP}(ESR)$. Thus, once the output capacitors are selected, the maximum allowable ripple voltage, $V_{PP(MAX)}$, determines the lower limit on the inductance.

$$L \geq (ESR) \cdot \frac{\left(V_{IN} - N \cdot V_{OUT}\right) \cdot V_{OUT}}{F_{SW} \cdot V_{IN} \cdot V_{PP(MAX)}} \qquad \text{(EQ. 30)}$$

Since the capacitors are supplying a decreasing portion of the load current while the regulator recovers from the transient, the capacitor voltage becomes slightly depleted. The output inductors must be capable of assuming the entire load current before the output voltage decreases more than ΔV_{MAX}. This places an upper limit on inductance.

Equation 31 gives the upper limit on L for the cases when the trailing edge of the current transient causes a greater output-voltage deviation than the leading edge. Equation 32 addresses the leading edge. Normally, the trailing edge dictates the selection of L because duty cycles are usually less than 50%. Nevertheless, both inequalities should be evaluated, and L should be selected based on the lower of the two results. In each equation, L is the per-channel inductance, C is the total output capacitance, and N is the number of active channels.

$$L \leq \frac{2 \cdot N \cdot C \cdot V_O}{(\Delta I)^2} \cdot \left[\Delta V_{MAX} - (\Delta I \cdot ESR)\right] \quad \text{(EQ. 31)}$$

$$L \leq \frac{(1.25) \cdot N \cdot C}{(\Delta I)^2} \cdot \left[\Delta V_{MAX} - (\Delta I \cdot ESR)\right] \cdot \left(V_{IN} - V_O\right) \quad \text{(EQ. 32)}$$

Switching Frequency

There are a number of variables to consider when choosing the switching frequency, as there are considerable effects on the upper MOSFET loss calculation. These effects are outlined in *MOSFETs*, and they establish the upper limit for the switching frequency. The lower limit is established by the requirement for fast transient response and small output-voltage ripple as outlined in *Output Filter Design*. Choose the lowest switching frequency that allows the regulator to meet the transient-response requirements.

Switching frequency is determined by the selection of the frequency-setting resistor, R_{FS}. Figure 23 and Equation 33 are provided to assist in selecting the correct value for R_{FS}

$$R_{FS} = 10^{[10.61 - 1.035 \cdot \log(F_{SW})]} \quad \text{(EQ. 33)}$$

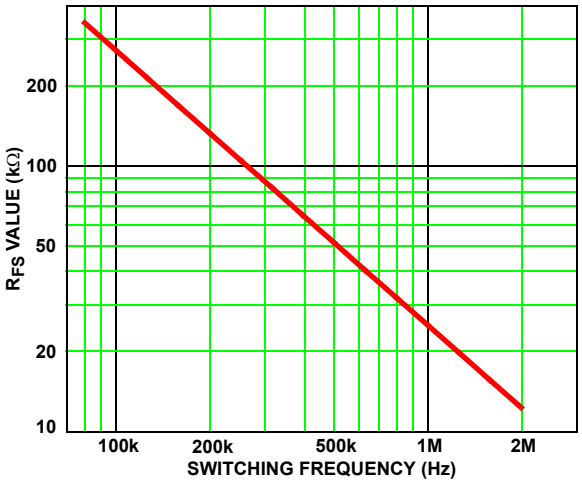


FIGURE 23. R_{FS} vs SWITCHING FREQUENCY

Input Capacitor Selection

The input capacitors are responsible for sourcing the AC component of the input current flowing into the upper MOSFETs. Their RMS current capacity must be sufficient to handle the AC component of the current drawn by the upper MOSFETs which is related to duty cycle and the number of active phases.

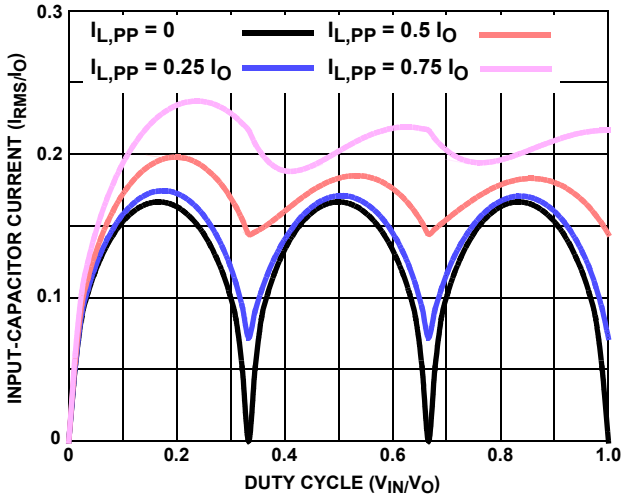


FIGURE 24. NORMALIZED INPUT-CAPACITOR RMS CURRENT FOR 3-PHASE CONVERTER

For a three-phase design, use Figure 24 to determine the input-capacitor RMS current requirement set by the duty cycle, maximum sustained output current (I_O), and the ratio of the peak-to-peak inductor current ($I_{L,PP}$) to I_O. Select a bulk capacitor with a ripple current rating which will minimize the total number of input capacitors required to support the RMS current calculated. The voltage rating of the capacitors should also be at least 1.25 times greater than the maximum input voltage. Figures 25 and 26 provide the same input RMS current information for two-phase and single-phase designs respectively. Use the same approach for selecting the bulk capacitor type and number.

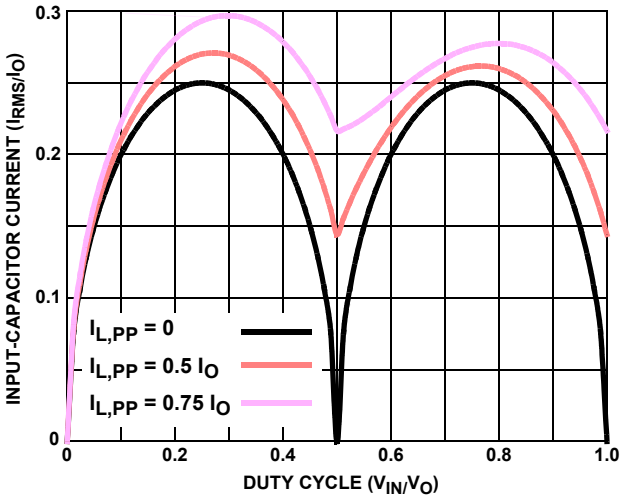


FIGURE 25. NORMALIZED INPUT-CAPACITOR RMS CURRENT FOR 2-PHASE CONVERTER

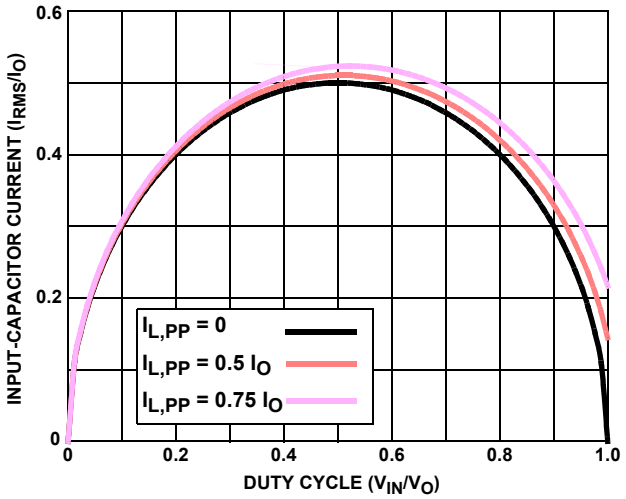


FIGURE 26. NORMALIZED INPUT-CAPACITOR RMS CURRENT FOR SINGLE-PHASE CONVERTER

Low ESL, high-frequency ceramic capacitors are needed in addition to the input bulk capacitors to suppress leading and falling edge voltage spikes. The spikes result from the high current slew rate produced by the upper MOSFET turn on and off. Place them as close as possible to each upper MOSFET drain to minimize board parasitics and maximize suppression.

Layout Considerations

MOSFETs switch very fast and efficiently. The speed with which the current transitions from one device to another causes voltage spikes across the interconnecting impedances and parasitic circuit elements. These voltage spikes can degrade efficiency, radiate noise into the circuit and lead to device overvoltage stress. Careful component layout and printed circuit design minimizes the voltage spikes in the converter. Consider, as an example, the turnoff transition of the upper PWM MOSFET. Prior to turnoff, the upper MOSFET was carrying channel current. During the turnoff, current stops flowing in the upper MOSFET and is picked up by the lower MOSFET. Any inductance in the switched current path generates a large voltage spike during the switching interval. Careful component selection, tight layout of the critical components, and short, wide circuit traces minimize the magnitude of voltage spikes.

There are two sets of critical components in a DC/DC converter using a ISL8103 controller. The power components are the most critical because they switch large amounts of energy. Next are small signal components that connect to sensitive nodes or supply critical bypassing current and signal coupling.

It is important to have a symmetrical layout, preferably with the controller equidistantly located from the three power trains it controls. Equally important are the gate drive lines (UGATE, LGATE, PHASE): since they drive the power train MOSFETs using short, high current pulses, it is important to size them as large and as short as possible to reduce their overall impedance and inductance. Extra care should be given to the LGATE traces in particular since keeping the impedance and inductance of these traces helps to significantly reduce the possibility of shoot-through. Equidistant placement of the controller to the three power trains also helps to keep these traces equally short (equal impedances, resulting in similar driving of both sets of MOSFETs).

The power components should be placed first. Locate the input capacitors close to the power switches. Minimize the length of the connections between the input capacitors, CIN, and the power switches. Locate the output inductors and output capacitors between the MOSFETs and the load. Locate the high-frequency decoupling capacitors (ceramic) as close as practicable to the decoupling target, making use of the shortest connection paths to any internal planes, such as vias to GND immediately next, or even onto the capacitor solder pad.

The critical small components include the bypass capacitors for VCC and PVCC. Locate the bypass capacitors, CBP, close to the device. It is especially important to locate the components associated with the feedback circuit close to their respective controller pins, since they belong to a high-impedance circuit loop, sensitive to EMI pick-up. It is also important to place current sense components close to their respective pins on the ISL8103, including the RISEN resistors, RS, RCOMP, CCOMP. For proper current sharing route three separate symmetrical as possible traces from the corresponding phase node for each RISEN.

A multi-layer printed circuit board is recommended. Figure 27 shows the connections of the critical components for the converter. Note that capacitors C_{xxIN} and C_{xxOUT} could each represent numerous physical capacitors. Dedicate one solid layer, usually the one underneath the component side of the board, for a ground plane and make all critical component ground connections with vias to this layer. Dedicate another solid layer as a power plane and break this plane into smaller islands of common voltage levels. Keep the metal runs from the PHASE terminal to inductor L_{OUT} short. The power plane should support the input power and output power nodes. Use copper filled polygons on the top and bottom circuit layers for the phase nodes. Use the remaining printed circuit layers for small signal wiring. The wiring traces from the IC to the MOSFETs' gates and sources should be sized to carry at least one ampere of current (0.02" to 0.05").

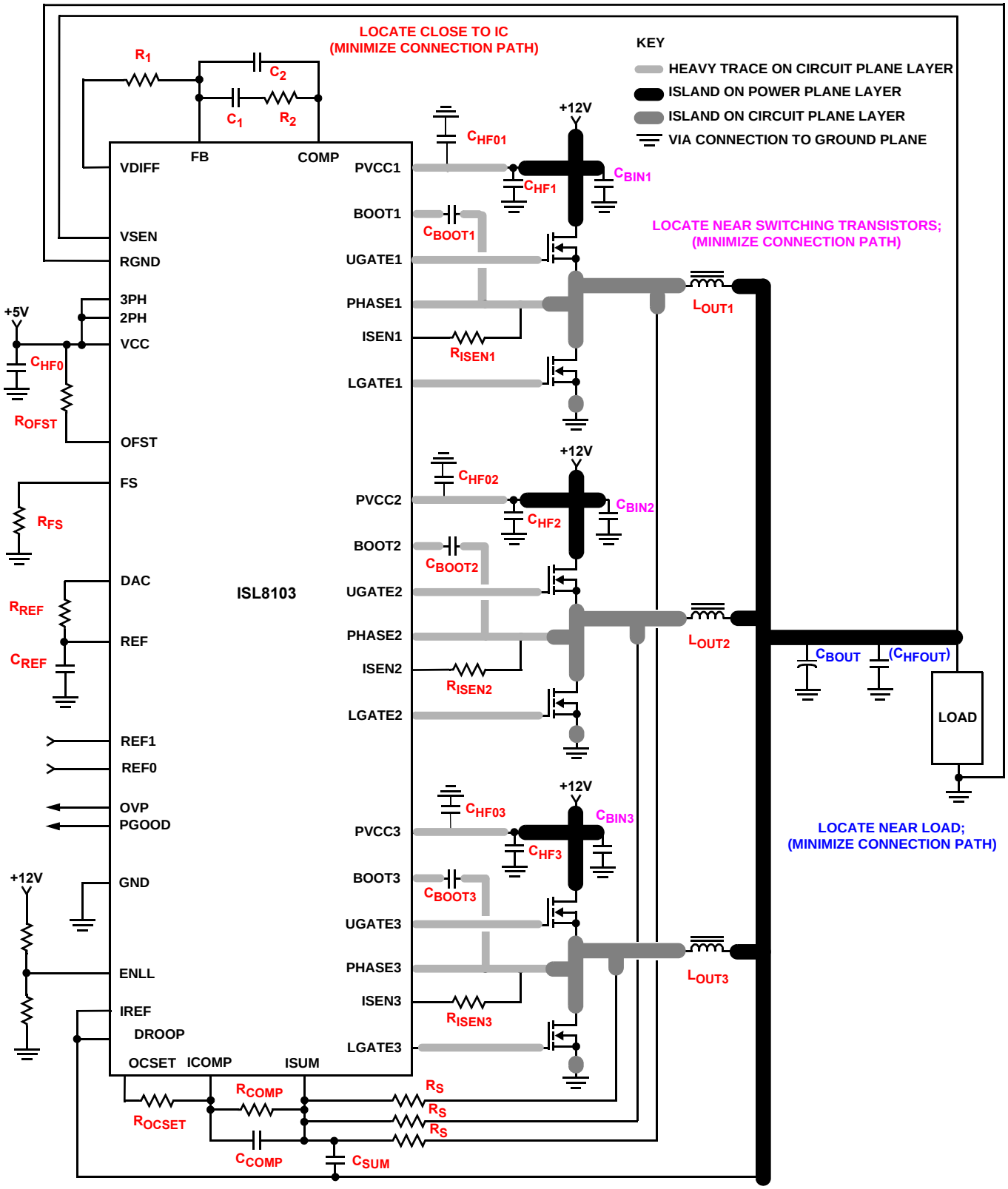
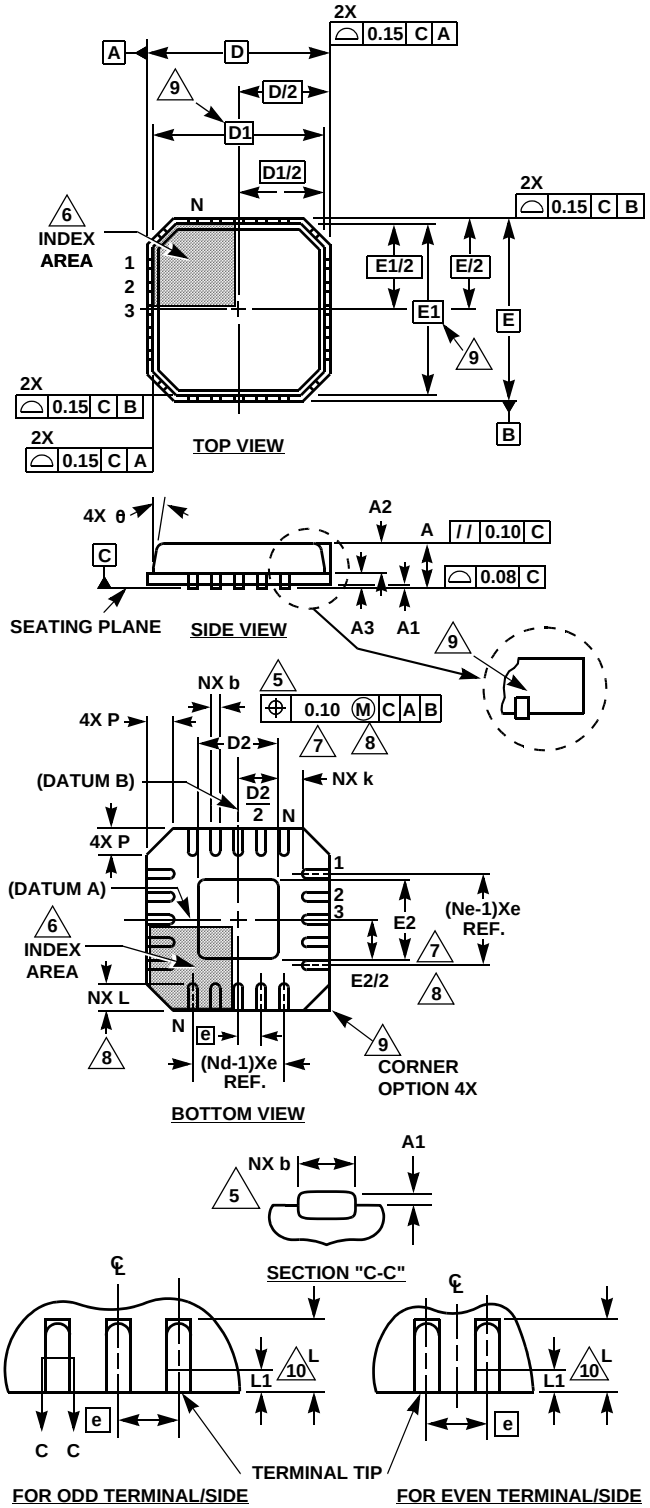


FIGURE 27. PRINTED CIRCUIT BOARD POWER PLANES AND ISLANDS

Quad Flat No-Lead Plastic Package (QFN)
Micro Lead Frame Plastic Package (MLFP)



L40.6x6

40 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE (COMPLIANT TO JEDEC MO-220VJJD-2 ISSUE C)

SYMBOL	MILLIMETERS			NOTES
	MIN	NOMINAL	MAX	
A	0.80	0.90	1.00	-
A1	-	-	0.05	-
A2	-	-	1.00	9
A3		0.20 REF		9
b	0.18	0.23	0.30	5, 8
D		6.00 BSC		-
D1		5.75 BSC		9
D2	3.95	4.10	4.25	7, 8
E		6.00 BSC		-
E1		5.75 BSC		9
E2	3.95	4.10	4.25	7, 8
e		0.50 BSC		-
k	0.25	-	-	-
L	0.30	0.40	0.50	8
L1	-	-	0.15	10
N		40		2
Nd		10		3
Ne		10		3
P	-	-	0.60	9
θ	-	-	12	9

Rev. 1 10/02

NOTES:

1. Dimensioning and tolerancing conform to ASME Y14.5-1994.
2. N is the number of terminals.
3. Nd and Ne refer to the number of terminals on each D and E.
4. All dimensions are in millimeters. Angles are in degrees.
5. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. Dimensions D2 and E2 are for the exposed pads which provide improved electrical and thermal performance.
8. Nominal dimensions are provided to assist with PCB Land Pattern Design efforts, see Intersil Technical Brief TB389.
9. Features and dimensions A2, A3, D1, E1, P & θ are present when Anvil singulation method is used and not present for saw singulation.
10. Depending on the method of lead termination at the edge of the package, a maximum 0.15mm pull back (L1) maybe present. L minus L1 to be equal to or greater than 0.3mm.