

## ***μP Supervisor with Watchdog Timer, Power-Fail Comparator, Manual Reset and Adjustable Power-On Reset***

Designed with high reset threshold accuracy and low power consumption, the ISL88705, ISL88706, ISL88707, ISL88708, ISL88716 and ISL88813 devices are microprocessor supervisors that are designed to monitor power-supply and battery functions in microprocessor systems. They can help to lower system cost, reduce board space requirements and increase the reliability of systems.

These devices provide essential functions such as supply voltage supervision by asserting a reset output during power-up and power-down as well as during brownout conditions. An auxiliary voltage monitor is provided for detecting power failures warning the system of low battery conditions or presence detection. In addition, an independent watchdog timer helps to monitor microprocessor activity every 1.6s (typical). An active-low manual reset is offered and reset signals remain asserted until  $V_{DD}$  returns to proper operating levels.

Users can increase the nominal 200ms power-on reset time-out delay by adding an external capacitor to the  $C_{POR}$  pin on the ISL88707 and ISL88708.

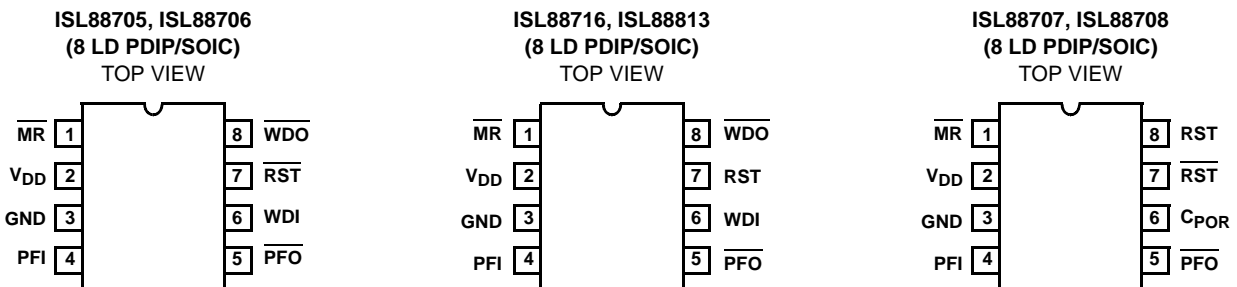
## **Features**

- Fixed-Voltage Options Allow Precise Monitoring of +3.0V, +3.3V, and +5.0V Power Supplies
- Additional Voltage Monitor for Power-Fail Detection or Low-Battery Warning
  - Monitors Voltages Down to 1.25V
  - Adjustable Power-Fail Input Threshold
- Watchdog Timer Capability With 1.6s Time-out
- Both RST and  $\overline{RST}$  Outputs Available
- 140ms Minimum Reset Pulse Width with Option to Customize Using an External Capacitor
- Manual Reset Input On All Devices
- Reset Signal Valid Down to  $V_{DD} = 1V$
- Accurate  $\pm 1.8\%$  Voltage Threshold
- Immune to Power-Supply Transients
- Ultra Low 10 $\mu$ A Maximum Supply Current at 3V
- Pb-Free Plus Anneal Available (RoHS Compliant)

## **Applications**

- Portable/Battery Powered Equipment
- Notebook/Desktop Computer Systems
- Designs Using DSPs, Microcontrollers or Microprocessors
- Controllers
- Intelligent Instruments
- Communications Systems
- Industrial Equipment

## **Pinouts**



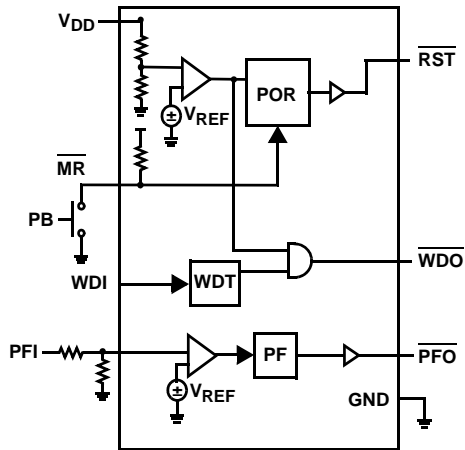
**Ordering Information**

PART NUMBER (Notes 1, 2)	PART MARKING	V <sub>TH</sub>	TEMP RANGE (°C)	PACKAGE (Pb-Free)	PKG. DWG. #
ISL88705IP846Z	88705 I46Z	4.64V	-40 to +85	8 Ld PDIP*	MDP0031
ISL88706IP844Z	88706 I44Z	4.38V	-40 to +85	8 Ld PDIP*	MDP0031
ISL88706IP831Z	88706 I31Z	3.09V	-40 to +85	8 Ld PDIP*	MDP0031
ISL88706IP829Z	88706 I29Z	2.92V	-40 to +85	8 Ld PDIP*	MDP0031
ISL88706IP826Z	88706 I26Z	2.63V	-40 to +85	8 Ld PDIP*	MDP0031
ISL88813IP846Z	88813 I46Z	4.64V	-40 to +85	8 Ld PDIP*	MDP0031
ISL88716IP826Z	88716 I26Z	2.63V	-40 to +85	8 Ld PDIP*	MDP0031
ISL88707IP846Z	88707 I46Z	4.64V	-40 to +85	8 Ld PDIP*	MDP0031
ISL88708IP844Z	88708 I44Z	4.38V	-40 to +85	8 Ld PDIP*	MDP0031
ISL88708IP831Z	88708 I31Z	3.09V	-40 to +85	8 Ld PDIP*	MDP0031
ISL88708IP829Z	88708 I29Z	2.92V	-40 to +85	8 Ld PDIP*	MDP0031
ISL88708IP826Z	88708 I26Z	2.63V	-40 to +85	8 Ld PDIP*	MDP0031
ISL88705IB846Z	88705 I46Z	4.64V	-40 to +85	8 Ld SOIC (Tape and Reel)	M8.15
ISL88706IB844Z	88706 I44Z	4.38V	-40 to +85	8 Ld SOIC (Tape and Reel)	M8.15
ISL88706IB831Z	88706 I31Z	3.09V	-40 to +85	8 Ld SOIC (Tape and Reel)	M8.15
ISL88706IB829Z	88706 I29Z	2.92V	-40 to +85	8 Ld SOIC (Tape and Reel)	M8.15
ISL88706IB826Z	88706 I26Z	2.63V	-40 to +85	8 Ld SOIC (Tape and Reel)	M8.15
ISL88813IB846Z	88813 I46Z	4.64V	-40 to +85	8 Ld SOIC (Tape and Reel)	M8.15
ISL88716IB826Z	88716 I26Z	2.63V	-40 to +85	8 Ld SOIC (Tape and Reel)	M8.15
ISL88707IB846Z	88707 I46Z	4.64V	-40 to +85	8 Ld SOIC (Tape and Reel)	M8.15
ISL88708IB844Z	88708 I44Z	4.38V	-40 to +85	8 Ld SOIC (Tape and Reel)	M8.15
ISL88708IB831Z	88708 I31Z	3.09V	-40 to +85	8 Ld SOIC (Tape and Reel)	M8.15
ISL88708IB829Z	88708 I29Z	2.92V	-40 to +85	8 Ld SOIC (Tape and Reel)	M8.15
ISL88708IB826Z	88708 I26Z	2.63V	-40 to +85	8 Ld SOIC (Tape and Reel)	M8.15

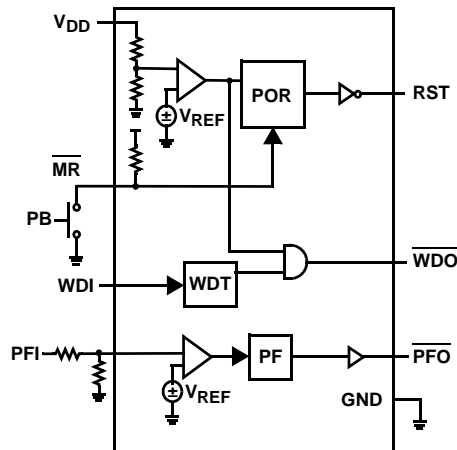
NOTES:

1. Add "-TK" suffix for SOIC Tape and Reel Packaging
  2. Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
- \*Pb-free PDIPs can be used for through hole wave solder processing only. They are not intended for use in Reflow solder processing applications.

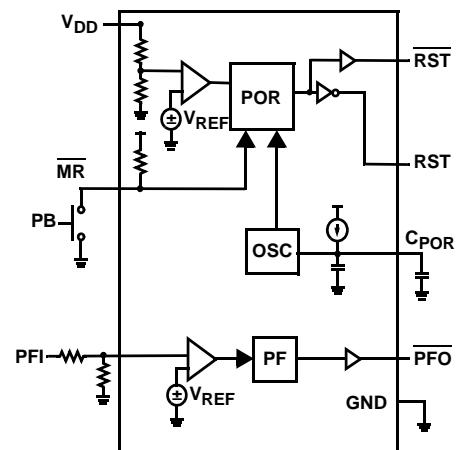
Functional Block Diagrams



ISL88705, ISL88706



ISL88716, ISL88813



ISL88707, ISL88708

## Pin Descriptions

ISL88705, ISL88706	ISL88716, ISL88813	ISL88707, ISL88708	NAME	DESCRIPTION
1	1	1	$\overline{\text{MR}}$	<b>Manual Reset Input.</b> A reset signal is generated when this input is pulled low. The $\overline{\text{MR}}$ input is an active low debounced input to which a user can connect a push-button to add manual reset capability or drive with a signal. The MR pin has an internal 20k $\Omega$ pull-up.
2	2	2	$V_{\text{DD}}$	<b>Power Supply Terminal.</b> The voltage at this pin is compared against an internal factory-programmed voltage trip point, $V_{\text{TH1}}$ . A reset is first asserted when the device is initially powered up to ensure that the power supply has stabilized. Thereafter, reset is again asserted whenever $V_{\text{DD}}$ falls below $V_{\text{TH1}}$ . The device is designed with hysteresis to help prevent chattering due to noise and is immune to brief power-supply transients. The voltage threshold $V_{\text{TH1}}$ is specified in the part number suffix.
3	3	3	GND	<b>Ground Connection</b>
4	4	4	PFI	<b>Power-Fail Input</b> This is an auxiliary monitored voltage input with a 1.25V threshold that causes $\overline{\text{PFO}}$ state to follow the PFI input state.
5	5	5	$\overline{\text{PFO}}$	<b>Power-Fail Output.</b> This output goes high if the voltage on PFI is greater than 1.25V, otherwise $\overline{\text{PFO}}$ stays low.
		6	$C_{\text{POR}}$	<b>Adjustable POR Time-out Delay Input.</b> Connecting an external capacitor from $C_{\text{POR}}$ to ground allows the user to increase the Power On Reset timeout ( $t_{\text{POR}}$ ) from the nominal 200ms.
6	6		WDI	<b>Watchdog Input.</b> The Watchdog Input takes an input from a microprocessor and ensures that it periodically toggles the WDI pin, otherwise the internal nominal 1.6s watchdog timer runs out, then reset is asserted and WDO is pulled low. The internal Watchdog Timer is cleared whenever the WDI sees a rising or falling edge or the device is manually reset. Floating WDI or connecting WDI to a high-impedance three-state buffer disables the watchdog feature.
7		7	$\overline{\text{RST}}$	<b>Active-Low Reset Output.</b> The $\overline{\text{RST}}$ output is an active low output with an internal PMOS pull-up that is pulled low to GND when reset is asserted. Reset is asserted whenever: <ol style="list-style-type: none"> <li>1. The device is first powered up,</li> <li>2. <math>V_{\text{DD}}</math> falls below its minimum voltage sense level or</li> <li>3. <math>\overline{\text{MR}}</math> is asserted.</li> </ol> The reset output continues to be asserted for typically 200ms after $V_{\text{DD}}$ rises above the reset threshold or $\overline{\text{MR}}$ input goes from low to high. A watchdog time-out will not trigger a reset unless WDO is connected to $\overline{\text{MR}}$ .
	7	8	RST	<b>Active-High Reset Output.</b> The RST pin functions identically to its complementary $\overline{\text{RST}}$ output but is an active high push pull output. RST is set high to $V_{\text{DD}}$ when reset is asserted. See the $\overline{\text{RST}}$ description for more details on conditions that cause a reset.
8	8		$\overline{\text{WDO}}$	<b>Watchdog Output.</b> This output is pulled low when the nominal 1.6s internal Watchdog Timer expires and does not go high again until the watchdog is cleared. WDO also goes low during low $V_{\text{DD}}$ conditions. Whenever $V_{\text{DD}}$ is below the reset threshold, WDO stays low. However, unlike RESET, WDO does not have a minimum pulse width. As soon as $V_{\text{DD}}$ rises above the reset threshold, WDO goes high with no delay.

**Absolute Maximum Ratings**

Temperature Under Bias	-40°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on any Pin with Respect to GND	-1.0V to +7V
DC Output Current	5mA
Lead Temperature (Soldering, 10s)	+300°C

**Recommended Operating Conditions**

Temperature Range (Industrial)	-40°C to +85°C
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**Thermal Information**

Thermal Resistance (Typical, Note 3)	$\theta_{JA}$ (°C/W)
PDIP Package* (4-layer test board)	83
SOIC Package (4-layer test board)	110

\*Pb-free PDIPs can be used for through hole wave solder processing only. They are not intended for use in Reflow solder processing applications.

*CAUTION: Absolute Maximum Ratings indicate limits beyond which permanent damage to the device and impaired reliability may occur. These are stress ratings provided for information only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification are not implied.*

*For guaranteed specifications and test conditions, see Electrical Specifications. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.*

**NOTE:**

- $\theta_{JA}$  is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.

**Electrical Specifications** Over the recommended operating conditions unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
$V_{DD}$	Supply Voltage Range		2.0		5.5	V
$I_{DD}$		$V_{DD} = 5V$ , WDT Inactive		10	19	$\mu A$
		$V_{DD} = 3V$ , WDT Inactive		8	10	$\mu A$
$I_{LI}$	Input Leakage Current (PFI)				100	nA
$I_{LO}$	Output Leakage Current				100	nA

**VOLTAGE THRESHOLDS**

$V_{TH1}$	Fixed $V_{DD}$ Voltage Trip Point		4.556	4.640	4.724	V
			4.301	4.380	4.459	V
			3.034	3.090	3.146	V
			2.867	2.920	2.973	V
			2.583	2.630	2.677	V
$V_{TH1HYST}$	Hysteresis at $V_{TH1}$ Input Temperature = +25°C	$V_{TH1} = 4.64V$		46		mV
		$V_{TH1} = 4.38V$		44		mV
		$V_{TH1} = 3.09V$		37		mV
		$V_{TH1} = 2.92V$		29		mV
		$V_{TH1} = 2.63V$		31		mV

**RST AND  $\overline{RST}$**

$V_{OL}$	Reset Output Voltage Low	$V_{DD} \geq 3.3V$ , Sinking 2.5mA		0.05	0.40	V
		$V_{DD} < 3.3V$ , Sinking 1.5mA		0.05	0.40	V
$V_{OH}$	RST Output Voltage High	$V_{DD} \geq 3.3V$ , Sourcing 2.5mA	$V_{DD}-0.6$	$V_{DD}-0.4$		V
		$V_{DD} < 3.3V$ , Sourcing 1.5mA	$V_{DD}-0.6$	$V_{DD}-0.4$		V
	$\overline{RST}$ Output Voltage High	$V_{DD} \geq 3.3V$ , Sourcing 0.8mA	$V_{DD}-0.6$	$V_{DD}-0.4$		V
		$V_{DD} < 3.3V$ , Sourcing 0.5mA	$V_{DD}-0.6$	$V_{DD}-0.4$		V
$t_{RPD}$	$V_{TH}$ to Reset Asserted Delay			45		$\mu s$
$t_{POR}$	POR Time-Out Delay	$C_{POR}$ is open	140	200	260	ms
$C_{LOAD}$	Load Capacitance on Reset Pins			5		pF

**Electrical Specifications** Over the recommended operating conditions unless otherwise specified. (Continued)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
<b>MANUAL RESET</b>						
V <sub>MRL</sub>	$\overline{MR}$ Input Voltage Low				0.8	V
V <sub>MRH</sub>	$\overline{MR}$ Input Voltage High		V <sub>DD</sub> -0.6			V
t <sub>MR</sub>	$\overline{MR}$ Minimum Pulse Width		550			ns
R <sub>PU</sub>	Internal $\overline{MR}$ Pull-Up Resistor			20		kΩ
<b>WATCHDOG TIMER (Note 4)</b>						
t <sub>WDT</sub>	Watchdog Time-out Period		1.0	1.6	2.0	s
t <sub>WDPS</sub>	WDI Minimum Pulse Width		100			ns
V <sub>IL</sub>	Watchdog Input Voltage Low				0.3 x V <sub>DD</sub>	V
V <sub>IH</sub>	Watchdog Input Voltage High		0.7 x V <sub>DD</sub>			V
V <sub>WDOL</sub>	$\overline{WDO}$ Output Voltage Low	V <sub>DD</sub> ≥ 3.3V, Sinking 2.5mA		0.05	0.40	V
		V <sub>DD</sub> < 3.3V, Sinking 1.5mA		0.05	0.40	V
V <sub>WDOH</sub>	$\overline{WDO}$ Output Voltage High	V <sub>DD</sub> ≥ 3.3V, Sourcing 2.5mA	V <sub>DD</sub> -0.6	V <sub>DD</sub> -0.4		V
		V <sub>DD</sub> < 3.3V, Sourcing 1.5mA	V <sub>DD</sub> -0.6	V <sub>DD</sub> -0.4		V
I <sub>WDT</sub>	Watchdog Input Current				1	μA
<b>POWER-FAIL DETECTION</b>						
V <sub>THPFI</sub>	PFI Input Threshold Voltage		1.20	1.25	1.30	V
PFI <sub>VTHYST</sub>	Hysteresis Voltage			20		mV
V <sub>PFO</sub>	PFO Output Voltage Low	V <sub>DD</sub> ≥ 3.3V, Sinking 2.5mA		0.05	0.40	V
		V <sub>DD</sub> < 3.3V, Sinking 1.5mA		0.05	0.40	V
V <sub>PFOH</sub>	PFO Output Voltage High	V <sub>DD</sub> ≥ 3.3V, Sourcing 2.5mA	V <sub>DD</sub> -0.6	V <sub>DD</sub> -0.4		V
		V <sub>DD</sub> < 3.3V, Sourcing 1.5mA	V <sub>DD</sub> -0.6	V <sub>DD</sub> -0.4		V

NOTE:

4. Applies to ISL88705, ISL88706, ISL88716, and ISL88813.

**Principles of Operation**

The ISL88705 - ISL88813 devices provide those functions needed for monitoring critical voltages such as power-supply and battery functions in microprocessor systems. Features of these supervisors include Power On Reset control, Supply Voltage Supervision, Power-Fail Detection and Manual Reset Assertion. The integration of all these features along with high reset threshold accuracy and low power consumption make these devices ideal for portable or battery-powered equipment.

**Power-On Reset (POR)**

Applying power to the device activates a POR circuit which asserts reset (i.e. RST goes high while  $\overline{RST}$  goes low). These signals provide several benefits:

- It prevents the system microprocessor from starting to operate with insufficient voltage.
- It prevents the processor from operating prior to stabilization of the oscillator.
- It ensures that the monitored device is held out of operation until internal registers are properly loaded.
- It allows time for an FPGA to download its configuration prior to initialization of the circuit.

The reset signals remain active until V<sub>DD</sub> rises above the minimum voltage sense level for time period t<sub>POR</sub>. This ensures that the supply voltage has stabilized to sufficient operating levels.

### Low Voltage Monitoring

These devices monitor both the voltage level of  $V_{DD}$  and an auxiliary voltage on PFI.

When IC is initially biased reset is asserted until the  $V_{DD}$  voltage is greater than the specific IC fixed-voltage trip point for the  $t_{POR}$  duration of 200ms. At any subsequent time that  $V_{DD}$  does not exceed its voltage threshold, reset is once again asserted, i.e.  $\overline{RST}$  is high and  $\overline{RST}$  is low.

### Power Failure Monitor

These devices also have a Power-Failure Monitor that helps to monitor an additional critical voltage on the Power-Fail Input (PFI) pin. For example, the PFI pin could be used to provide an early power-fail warning, detect a low-battery condition, presence detection or simply monitor a power supply other than +5V. The 1.25V threshold detector can be adjusted using an external resistor divider network to provide custom voltage monitoring of voltages greater than 1.25V, according to the following formula (See Figure 1):

$$PFI V_{TH} = 1.25 (R1 + R2/R2)$$

$\overline{PFO}$  goes low whenever PFI is less than the 1.25V (or user-set) threshold voltage.

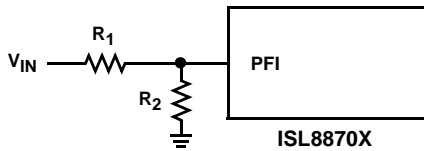
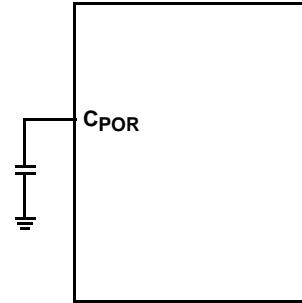


FIGURE 1. CUSTOM  $V_{TH}$  WITH RESISTOR DIVIDER ON PFI

### Adjusting $t_{POR}$

On the ISL88707 and ISL88708, users can adjust the Power On Reset timeout delay ( $t_{POR}$ ) to many times the nominal  $t_{POR}$  of 200ms. To do this, connect a capacitor between  $C_{POR}$  and ground (see Figure 3). For example, connecting a 50pF capacitor to CPOR will increase  $t_{POR}$  from 200ms to ~1.4s. Care should be taken in PCB layout and capacitor placement in order to reduce stray capacitance as much as possible, which contributes to  $t_{POR}$  error.



ISL88707, ISL88708

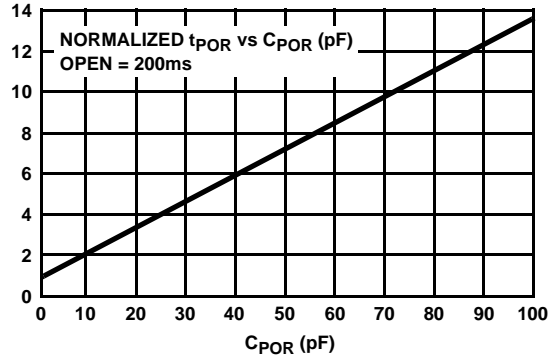


FIGURE 3. ADJUSTING  $t_{POR}$  WITH A CAPACITOR

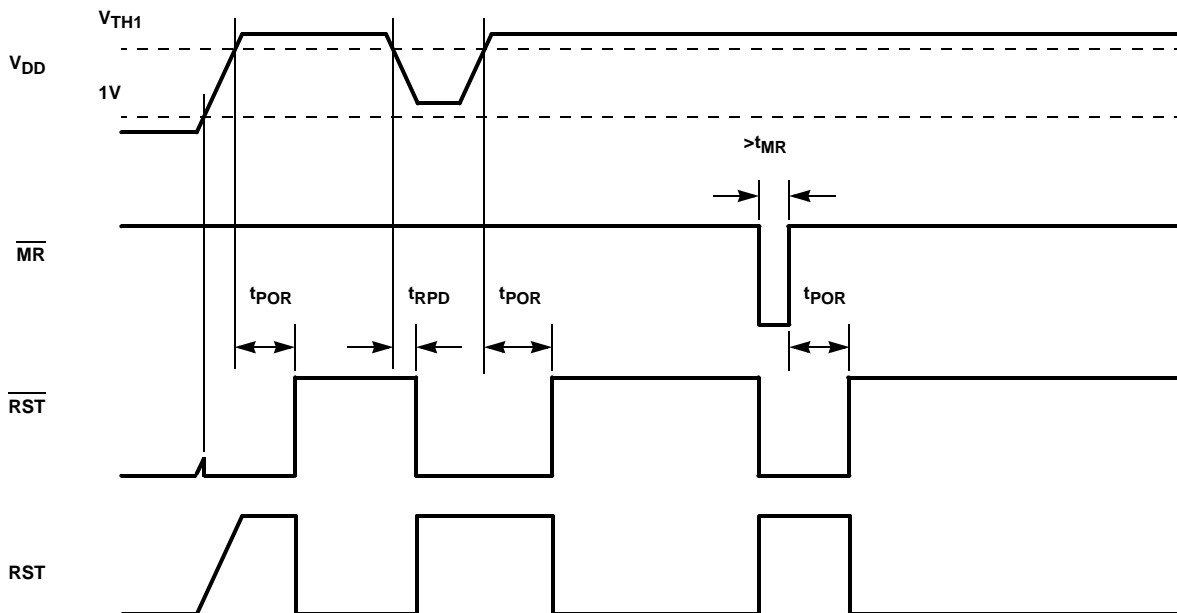


FIGURE 2. POWER-SUPPLY MONITORING TIMING DIAGRAM (WDI TRI-STATED)

**Manual Reset**

The manual-reset input ( $\overline{MR}$ ) allows the user to trigger a reset by using a push-button switch. The  $\overline{MR}$  input is an active low debounced input. By connecting a push-button switch directly from  $\overline{MR}$  to ground, the designer adds manual system reset capability (see Figure 4). Reset is asserted if the MR pin is pulled low to less than 100mV for the minimum  $\overline{MR}$  pulse width or longer while the push-button is closed. After MR is released, the reset outputs remain asserted for  $t_{POR}$  (200ms) and then released.

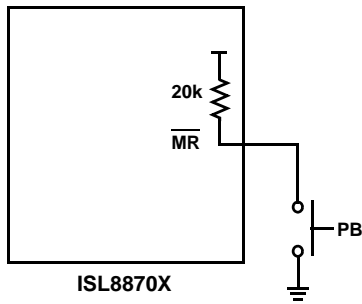


FIGURE 4. CONNECTING A MANUAL RESET PUSH-BUTTON

**Watchdog Timer**

The Watchdog Timer circuit checks microprocessor activity by monitoring the WDI input pin. The microprocessor must periodically toggle the WDI pin within  $t_{WDT}$  (typically 1.6s), otherwise the  $\overline{WDO}$  pin goes low (see Figure 5). Internally, the 1.6s timer is cleared by either a reset or by toggling the WDI input, which can detect pulses longer than 50ns.

Whenever there is a low-voltage  $V_{DD}$  condition,  $\overline{WDO}$  goes low. Unlike the reset outputs, however,  $\overline{WDO}$  does not have a minimum reset pulse width ( $t_{POR}$ ).  $\overline{WDO}$  goes high as soon as  $V_{DD}$  rises above its voltage trip point (see Figure 5). With WDI open or connected to a tristated high impedance input, the Watchdog Timer is disabled and only pulls low when  $V_{DD} < V_{TH1}$ .

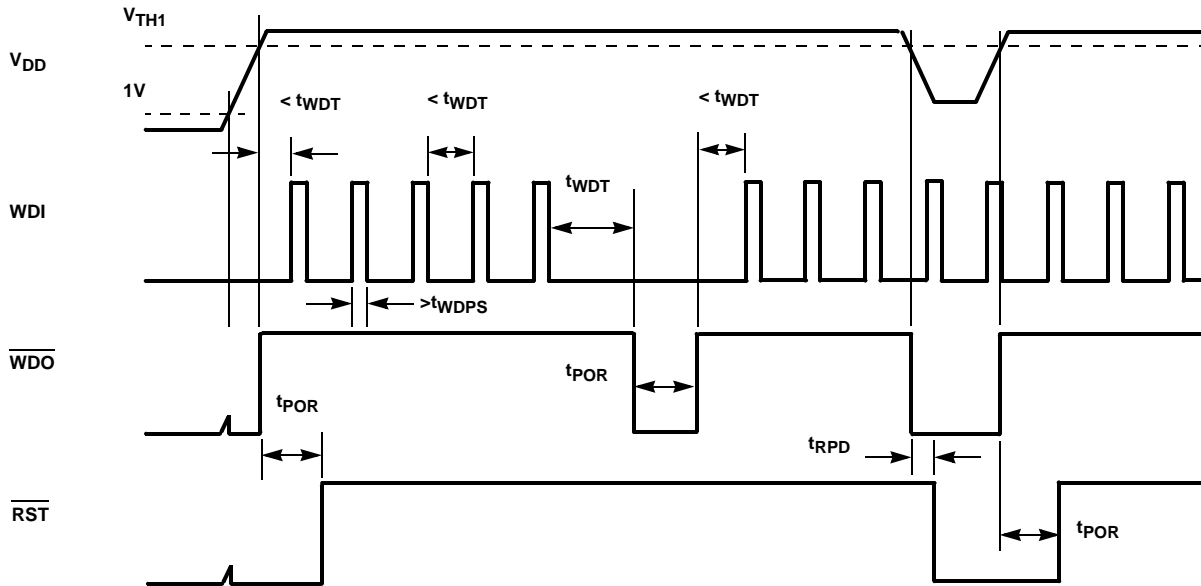


FIGURE 5. WATCHDOG TIMING DIAGRAM



Parametric Performance

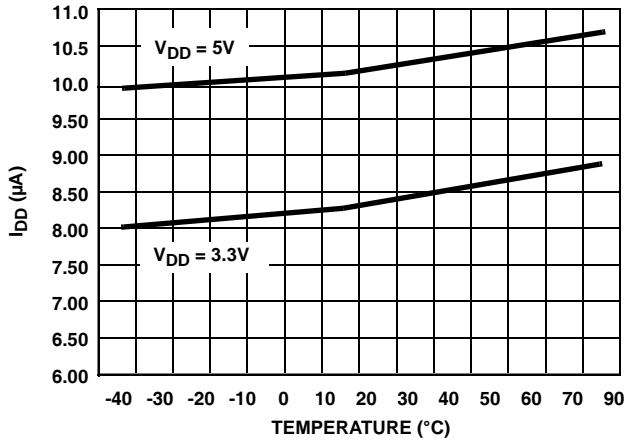


FIGURE 6. I<sub>DD</sub> vs TEMPERATURE

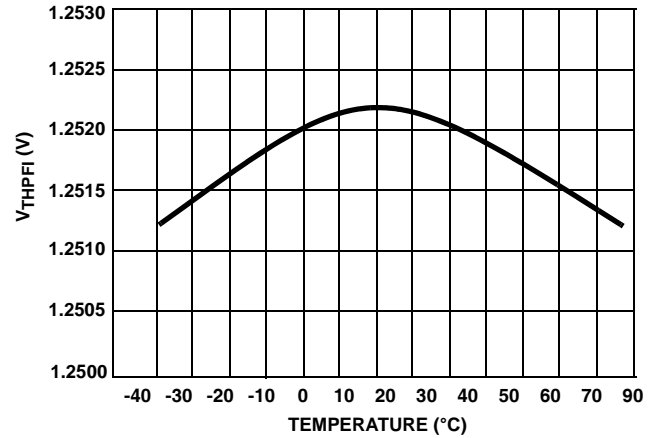


FIGURE 9. V<sub>THPF1</sub> vs TEMPERATURE

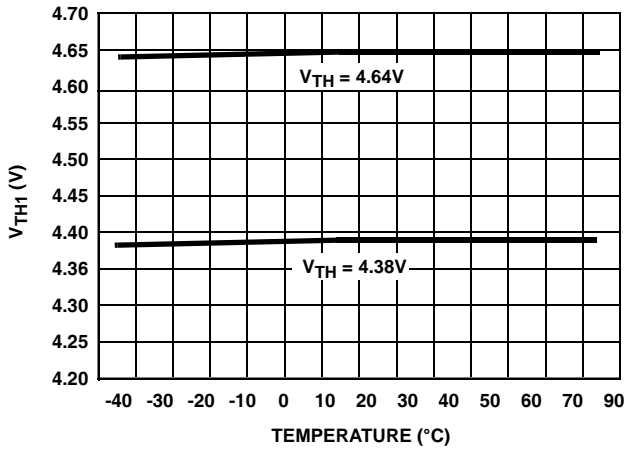


FIGURE 7. V<sub>TH1</sub> vs TEMPERATURE FOR 5V SUPPLY

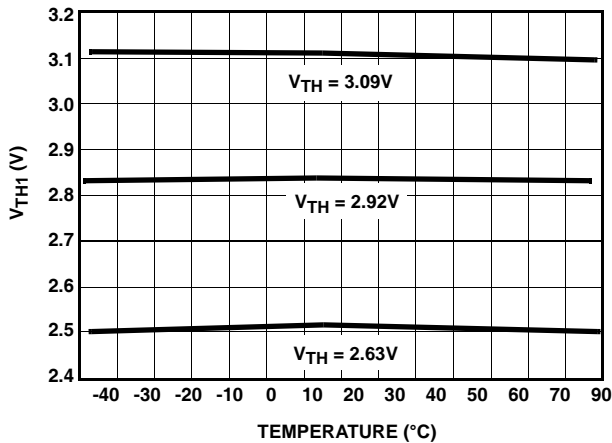


FIGURE 8. V<sub>TH1</sub> vs TEMPERATURE < 5V SUPPLY

ISL88705EVAL1 and Applications

The ISL88705EVAL1 supports all six of the ISL88705- ISL88813 devices, enabling evaluation of basic functional operation and common application implementations. Figures 15 and 17 illustrate the ISL88705EVAL1 in photographic and schematic forms respectively.

The ISL88705EVAL1 is divided into two banks; each bank having one each of the three available pinouts. The top bank is fully populated and immediately usable whereas the bottom bank is unpopulated. Samples of other sample variants can be evaluated singularly or in combination with any other variant to provide a specific voltage monitoring solution. The left position has a ISL88705IB846Z monitoring the V<sub>DD</sub> rail voltage for a minimum of 4.64V with reset signaling. In addition, the power fail input (PFI) is being compared to the internal PFI voltage reference of 1.25V and the power fail output (PFO) will report the PFI condition. This feature can be used for monitoring an auxiliary voltage, providing an early warning of a brownout or power failure or presence detection in a system.

The middle position has the ISL88813IB846Z installed and is set up as a 5V window detector with jumper J1 installed. The V<sub>DD</sub> monitors for UV and the PFI for OV via the R3, R4 divider. The PFO output is inverted and connected to the manual reset input (MR) via U4. Hence a reset signal is generated when 4.64V < V<sub>DD</sub> > 5.38V. With J1 removed the PFO will be an OV indicator but no reset signal will be generated. Both of these positions share a common Watchdog input (WDI) signal although each has its own Watchdog output (WDO).

The right position has the ISL88707IB846Z and is set up as a +12V and +5V UV monitor with reset signal. The PFI allows monitoring of any voltage above the 1.25V PFI reference and with a resistor divider this is used to monitor the 12V. The ISL88707 and ISL88708 have the unique feature of an adjustable time to reset (t<sub>POR</sub>) signal

generation capability via the  $C_{POR}$  pin with an external capacitor to GND. This evaluation platform has an adjustable SMD capacitor, C4 (8pF to 45pF) that allows easy evaluation of this feature. Also unique to the ISL88707 and ISL88708 are both the RESET and  $\overline{RESET}$  outputs, all other variants having only one or the other.

Figures 10, 11, 12, 13 and 14 illustrate the basic IC functions and performance of the 3 implementations.

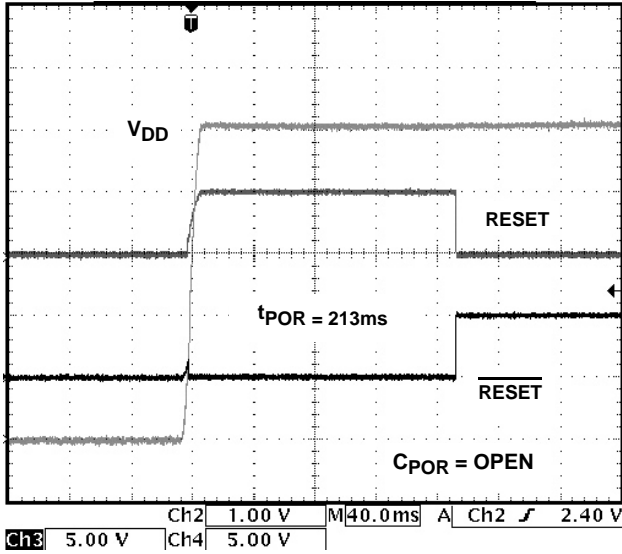


FIGURE 10. RESET AND  $\overline{RESET}$  ASSERTION

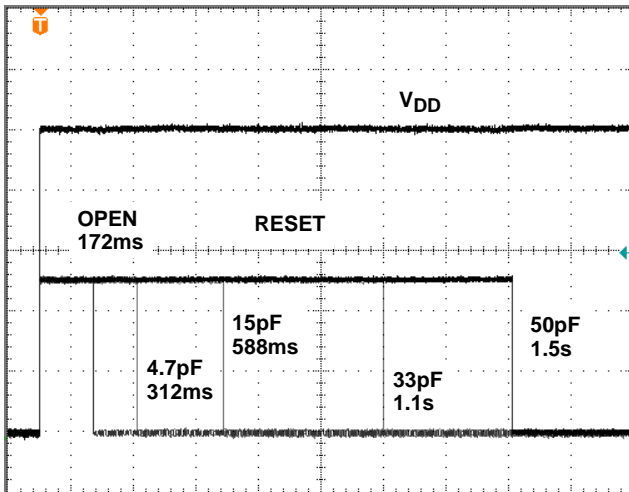


FIGURE 11. RESET ASSERTION vs  $C_{POR}$

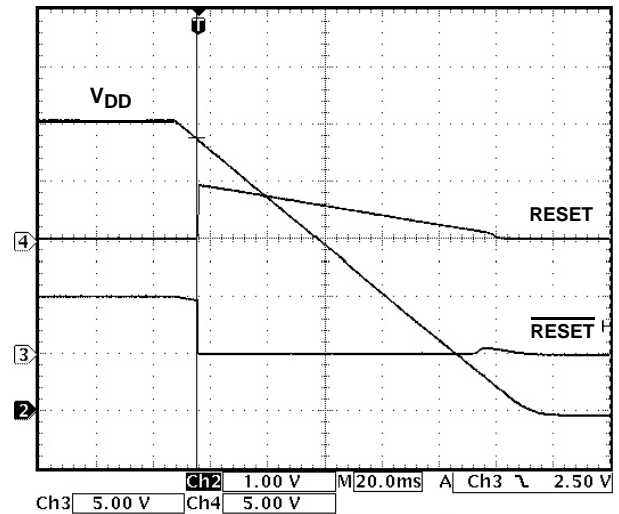


FIGURE 12. RESET AND  $\overline{RESET}$  DEASSERTION

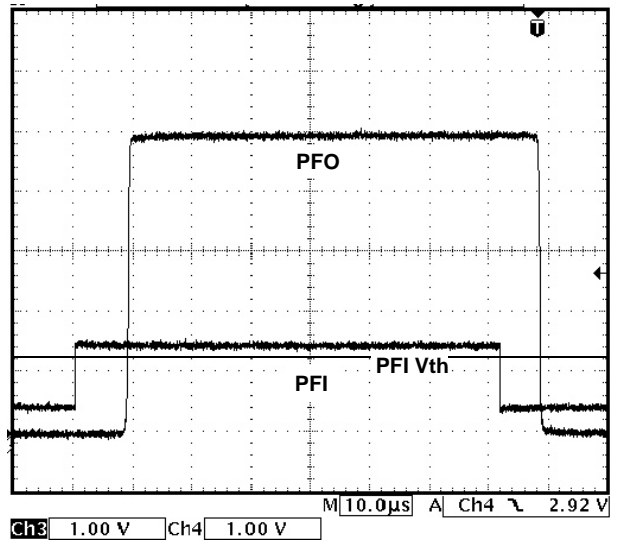


FIGURE 13. 5V PFI TO PFO RESPONSE

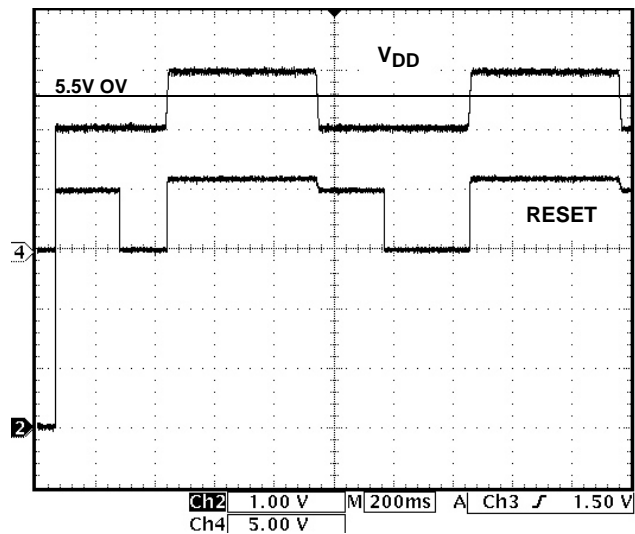


FIGURE 14. 5V OV/UV MONITORING

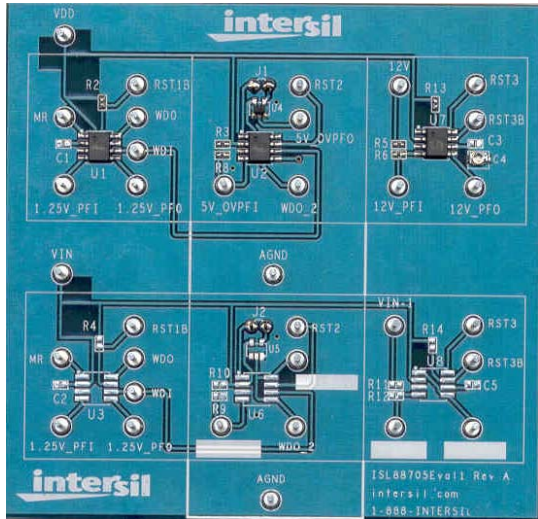


FIGURE 15. ISL88705EVAL1

**Bipolar Voltage Sensing**

Any of the ISL88705 - ISL88813 devices can be used to sense and report the presence of both a positive and negative voltage via the PFI and PFO as shown in Figure 16. The V<sub>DD</sub> monitors the positive voltage as normal and the PFI monitors the presence of the negative supply. As the differential voltage across the R<sub>1</sub>, R<sub>2</sub> divider is increased the resistor values must be chosen such that the PFI node is <1.25V when the -V supply is satisfactory and the positive supply is at its maximum specified value. This allows the positive supply to fluctuate within its acceptable range without signaling a reset. Driving the MR with the inverted PFO signal as shown provides for reset generation when -V is not satisfactorily present. Reset will remain asserted as long as PFO is high.

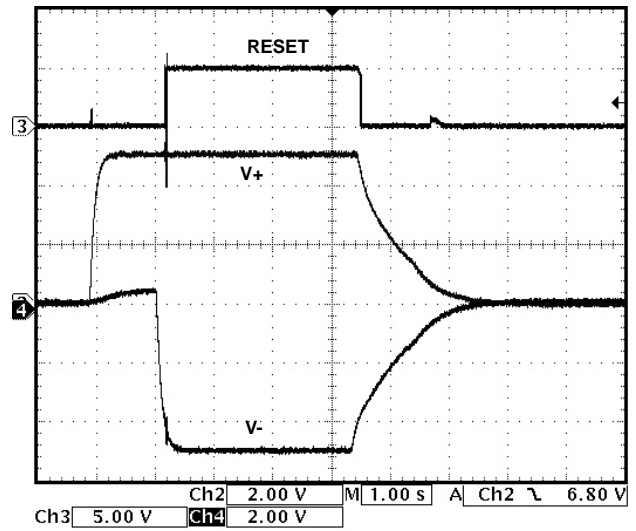
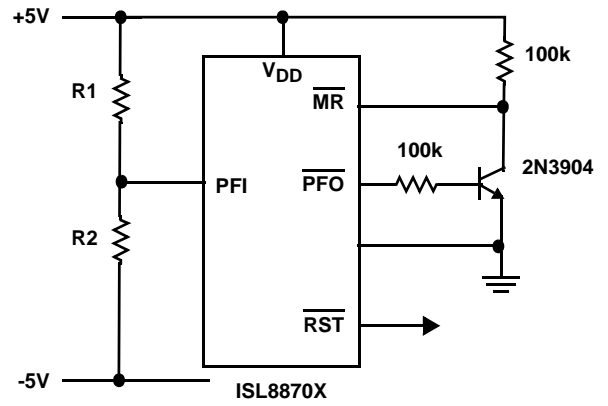


FIGURE 16. ±5V MONITORING

**Special Application Considerations**

Using good decoupling practices will prevent transients (i.e., due to switching noises and short duration droops in the supply voltage) from causing unwanted resets.

When using the C<sub>POR</sub> pin, avoid stray capacitance during layout as much as possible in order to minimize its effect on the t<sub>POR</sub> timing.

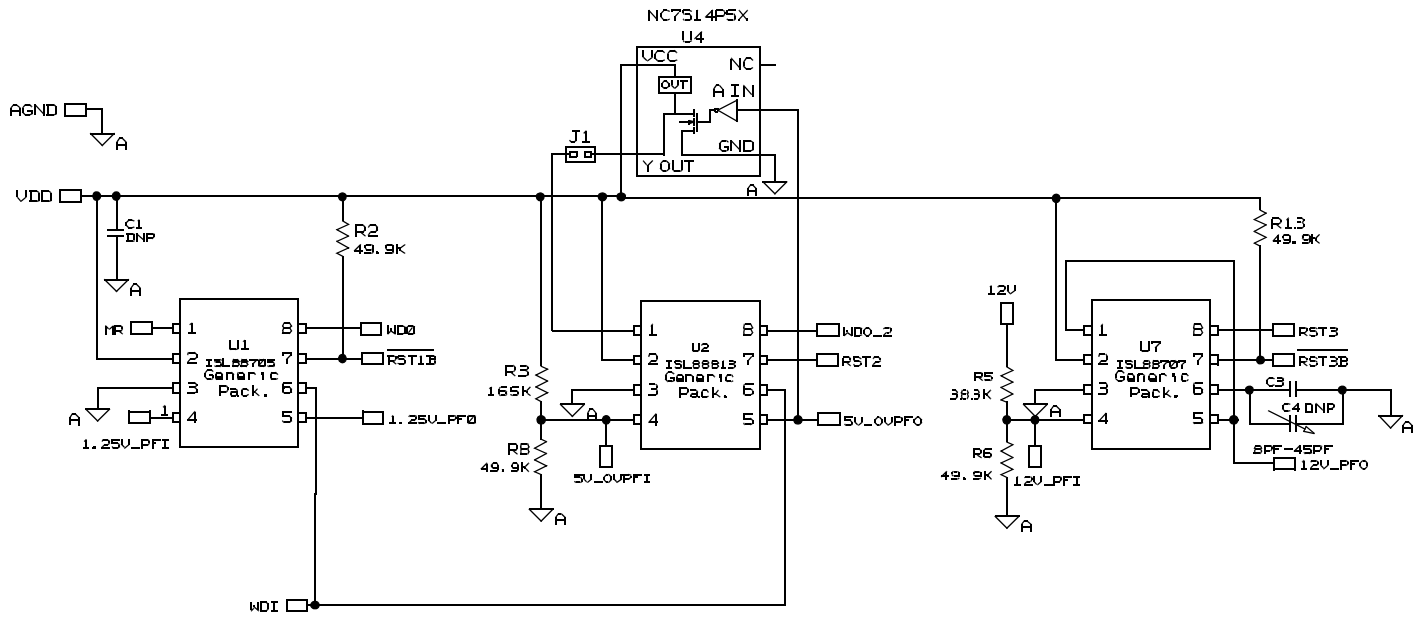
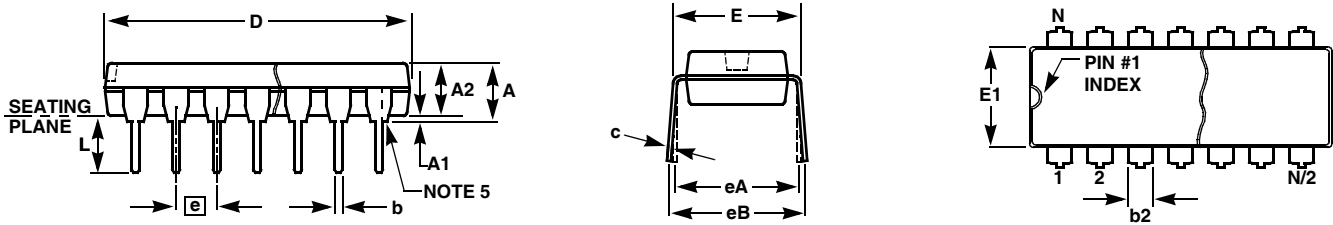


FIGURE 17. ISL88705EVAL1 SCHEMATIC (TOP BANK)

**Plastic Dual-In-Line Packages (PDIP)**



**MDP0031**

**PLASTIC DUAL-IN-LINE PACKAGE**

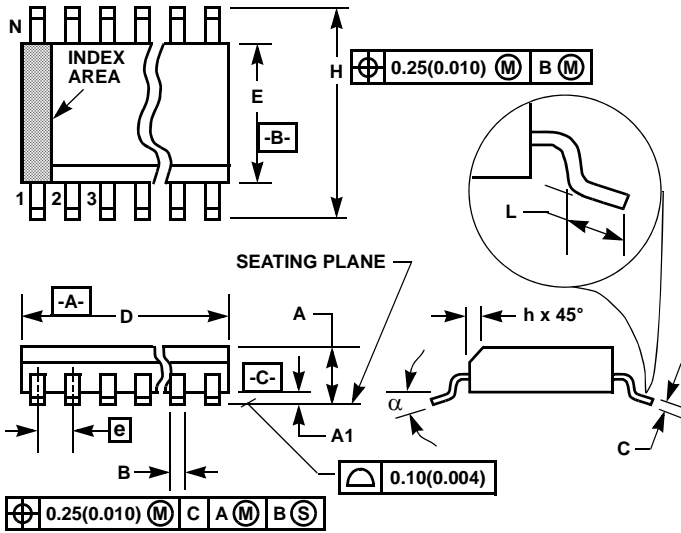
SYMBOL	PDIP8	PDIP14	PDIP16	PDIP18	PDIP20	TOLERANCE	NOTES
A	0.210	0.210	0.210	0.210	0.210	MAX	
A1	0.015	0.015	0.015	0.015	0.015	MIN	
A2	0.130	0.130	0.130	0.130	0.130	±0.005	
b	0.018	0.018	0.018	0.018	0.018	±0.002	
b2	0.060	0.060	0.060	0.060	0.060	+0.010/-0.015	
c	0.010	0.010	0.010	0.010	0.010	+0.004/-0.002	
D	0.375	0.750	0.750	0.890	1.020	±0.010	1
E	0.310	0.310	0.310	0.310	0.310	+0.015/-0.010	
E1	0.250	0.250	0.250	0.250	0.250	±0.005	2
e	0.100	0.100	0.100	0.100	0.100	Basic	
eA	0.300	0.300	0.300	0.300	0.300	Basic	
eB	0.345	0.345	0.345	0.345	0.345	±0.025	
L	0.125	0.125	0.125	0.125	0.125	±0.010	
N	8	14	16	18	20	Reference	

Rev. B 2/99

**NOTES:**

1. Plastic or metal protrusions of 0.010" maximum per side are not included.
2. Plastic interlead protrusions of 0.010" maximum per side are not included.
3. Dimensions E and eA are measured with the leads constrained perpendicular to the seating plane.
4. Dimension eB is measured with the lead tips unconstrained.
5. 8 and 16 lead packages have half end-leads as shown.

Small Outline Plastic Packages (SOIC)



M8.15 (JEDEC MS-012-AA ISSUE C)  
8 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0532	0.0688	1.35	1.75	-
A1	0.0040	0.0098	0.10	0.25	-
B	0.013	0.020	0.33	0.51	9
C	0.0075	0.0098	0.19	0.25	-
D	0.1890	0.1968	4.80	5.00	3
E	0.1497	0.1574	3.80	4.00	4
e	0.050 BSC		1.27 BSC		-
H	0.2284	0.2440	5.80	6.20	-
h	0.0099	0.0196	0.25	0.50	5
L	0.016	0.050	0.40	1.27	6
N	8		8		7
α	0°	8°	0°	8°	-

NOTES:

1. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension "E" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. "L" is the length of terminal for soldering to a substrate.
7. "N" is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width "B", as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

Rev. 1 6/05

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