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VL-FS-MGLS128128-02C REV. A
(MGLS128128-HV-LED03-SCH C)

DOCUMENT TITLE:

SPECIFICATION

OF

LCD MODULE TYPE

ITEM NO.: MGLS128128-02C

APPROVALS:

EFFECTIVE DATE

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A	2001.12.05	The specification was modified based on the document VL-TS-MGLS128128-02C REV. A (2001.03.01)	PHILIP CHENG	MICHAEL TSE



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VARITRONIX LIMITED

Specification of LCD Module Type Item No.: MGLS128128-02C

1. General Description

- 128 x 128 dots STN Positive Yellow Transflective LCD graphic module.
- Driving scheme: 1:128 multiplexed drive, 1/12.4 bias.
- Viewing direction: 6 O'clock.
- 'TOSHIBA' T6963C flat pack or equivalent LCD controller.
- 'TOSHIBA' T6A39 flat pack or equivalent LCD segment drivers.
- 'TOSHIBA' T6A40 flat pack or equivalent LCD common drivers.
- 8K byte display SRAM.
- Yellow-Green LED03 backlight.

2. Mechanical Specifications

The mechanical detail is shown in Fig. 1 and summarized in Table 1 below.

Table 1

Parameter	Specifications	Unit
Outline dimensions	92.0 (W) x 106.0(H) x 14.5(D)	mm
Viewing area	73.0(W) x 73.0(H)	mm
Active area	70.35(W) x 70.35(H)	mm
Display format	128 x 128	Dots
Dot size	0.50(W) x 0.50(H)	mm
Dot spacing	0.05(W) x 0.05(H)	mm
Dot pitch	0.55(W) x 0.55(H)	mm
Weight	TBD	Grams

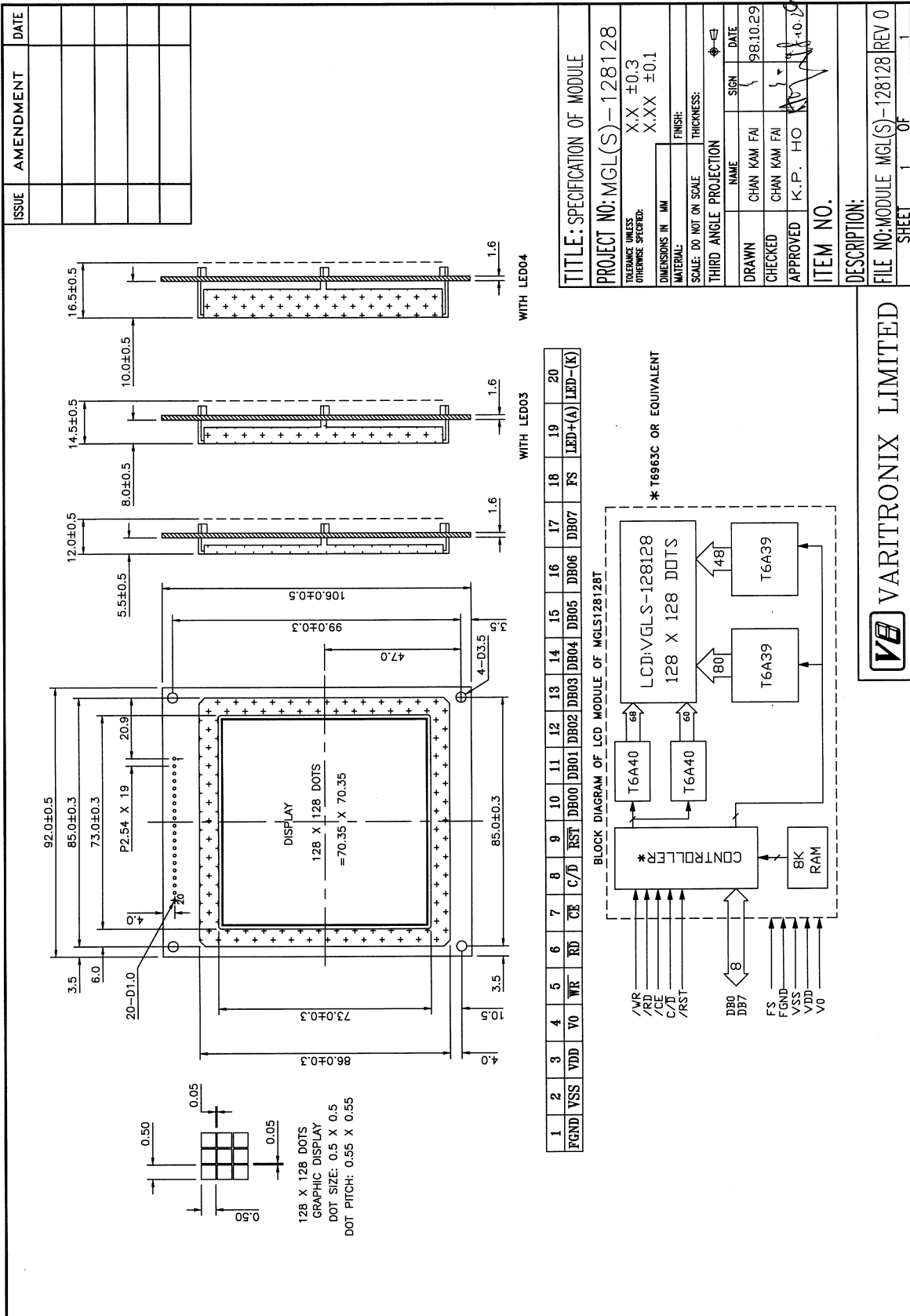


Figure 1: Outline drawing of MGLS128128-HV-LED03-SCH C module.



3. Absolute Maximum Ratings

3.1 Electrical Maximum Ratings(Ta = 25 °C)

Table 2

Parameter	Symbol	Min.	Max.	Unit
Supply voltage (Logic)	VDD - VSS	-0.3	+7.0	V
Supply voltage (LCD drive)	VLCD=VDD – V0	-0.3	+28.0	V
Input voltage	Vin	-0.3	VDD +0.3	V

Note:

The modules may be destroyed if they are used beyond the absolute maximum ratings.
All voltage values are referenced to VSS = 0V.

3.2 Environmental Condition

Table 3

Item	Operating Temperature (Topr)		Storage Temperature (Tstg)		Remark
	Min.	Max.	Min.	Max.	
Ambient Temperature	-10°C	+60°C	-20°C	+70°C	Dry
Humidity	95% max. RH for Ta ≤ 40°C < 95% RH for Ta > 40°C				no condensation
Vibration (IEC 68-2-6) cells must be mounted on a suitable connector	Frequency: 10 ~ 55 Hz Amplitude: 0.75 mm Duration: 20 cycles in each direction.				3 directions
Shock (IEC 68-2-27) Half-sine pulse shape	Pulse duration : 11 ms Peak acceleration: 981 m/s ² = 100g Number of shocks : 3 shocks in 3 mutually perpendicular axes.				3 directions



4. Electrical Specifications

4.1 Interface signals

Table 4

Pin No.	Symbol	Description
1	FGND	Frame Ground (see note 1)
2	VSS	Ground(0V)
3	VDD	Power supply for logic (+5V)
4	V0	Power supply for LCD drive
5	\overline{WR}	Command/Data write to module when "L"
6	\overline{RD}	Command/Data read from module when "L"
7	\overline{CE}	Chip enable of controller when "L"
8	C/D	Command/Data read /write. "H" for command read/write and "L" for data read/write.
9	\overline{RST}	Controller reset when "L"
10	DB00	Data input/output (LSB)
11	DB01	Data input/output
12	DB02	Data input/output
13	DB03	Data input/output
14	DB04	Data input/output
15	DB05	Data input/output
16	DB06	Data input/output
17	DB07	Data input/output (MSB)
18	FS	Font select. "H" for 6 x 8 font & "L" for 8 x 8 font
19	LED+(A)	Anode of LED backlight.
20	LED-(K)	Cathode of LED backlight.

Note 1: This pin is electrically connected to the metal bezel(frame).
User can choose to connect this pin to VSS or leave it open.



4.2 Typical Electrical Characteristics

At $T_a = 25\text{ }^\circ\text{C}$, $V_{DD} = 5V \pm 5\%$, $V_{SS} = 0V$.

Table 5

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply voltage (Logic)	$V_{DD} - V_{SS}$		4.75	5.00	5.25	V
Supply voltage (LCD)	$V_{LCD} = V_{DD} - V_0$	$V_{DD} = 5V$, Note 1	17.6	18.5	19.4	V
Input signal voltage	V_{IN}	"H" level	$V_{DD} - 2.2$	-	V_{DD}	V
		"L" level	0	-	0.8	V
Supply current (Logic & LCD)	I_{DD}	Character mode, $V_{DD} = 5V$, Note 1	-	7.5	11.2	mA
		Checker board mode, $V_{DD} = 5V$, Note 1	-	8.0	12.0	mA
Supply current (LCD)	I_0	Character mode, $V_{DD} = 5V$, Note 1	-	3.8	5.7	mA
		Checker board mode, $V_{DD} = 5V$, Note 1	-	4.1	6.1	mA
Supply voltage of LED03 backlight	V_{LED03}	Forward current = 120mA. Number of LED chips = 24.	3.8	4.1	4.5	V

Note 1: There is tolerance in optimum LCD driving voltage during production and it will be within the specified range.



4.3 Timing Specifications

At $T_a = -10^{\circ}\text{C}$ To $+60^{\circ}\text{C}$, $V_{DD} = 5\text{V} \pm 5\%$, $V_{SS} = 0\text{V}$

Refer to Fig. 2, the bus timing diagram.

Table 6

Parameter	Symbol	Min.	Max.	Unit
C/D Set-up time	t_{CDS}	100	-	ns
C/D Hold Time	t_{CDH}	10	-	ns
/CE,/RD,/WR Pulse Width	t_{CE}, t_{RD}, t_{WR}	80	-	ns
Data Set-up Time	t_{DS}	80	-	ns
Data Hold Time	t_{DH}	40	-	ns
Access Time	t_{ACC}	-	150	ns
Output Hold Time	t_{OH}	10	50	ns

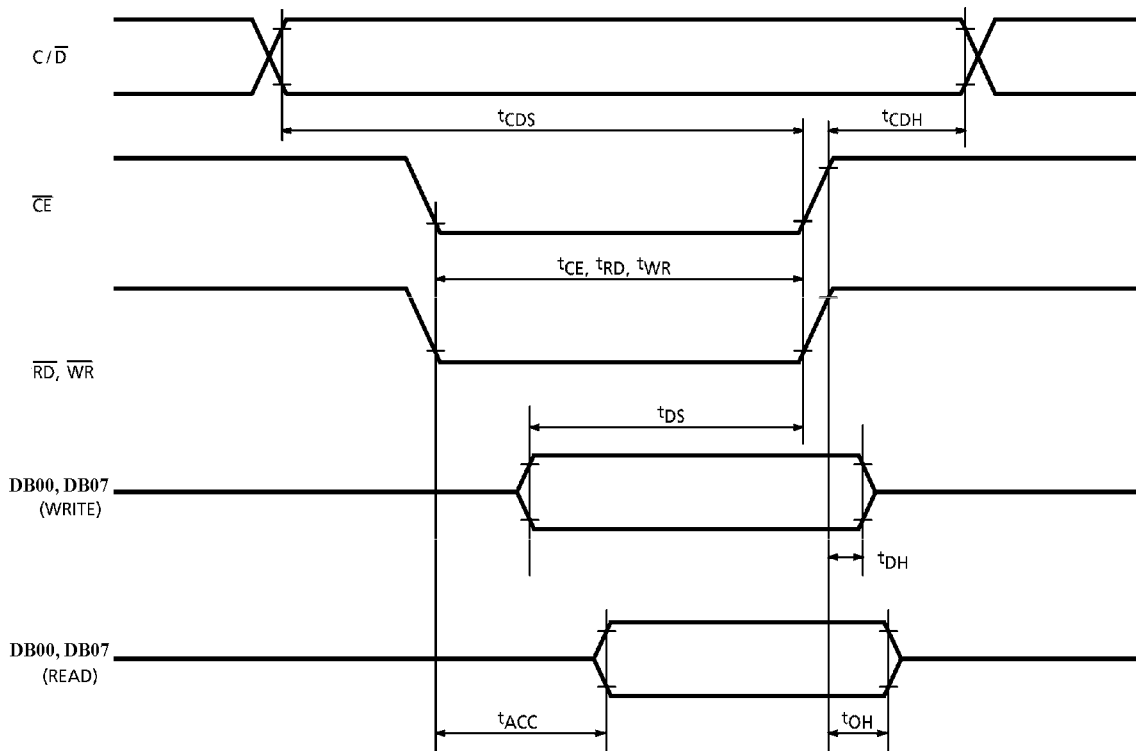


Figure 2: Bus Timing Diagram



4.4 Timing Diagram of VDD Against V0.

Power on sequence shall meet the requirement of Figure 3, the timing diagram of VDD against V0.

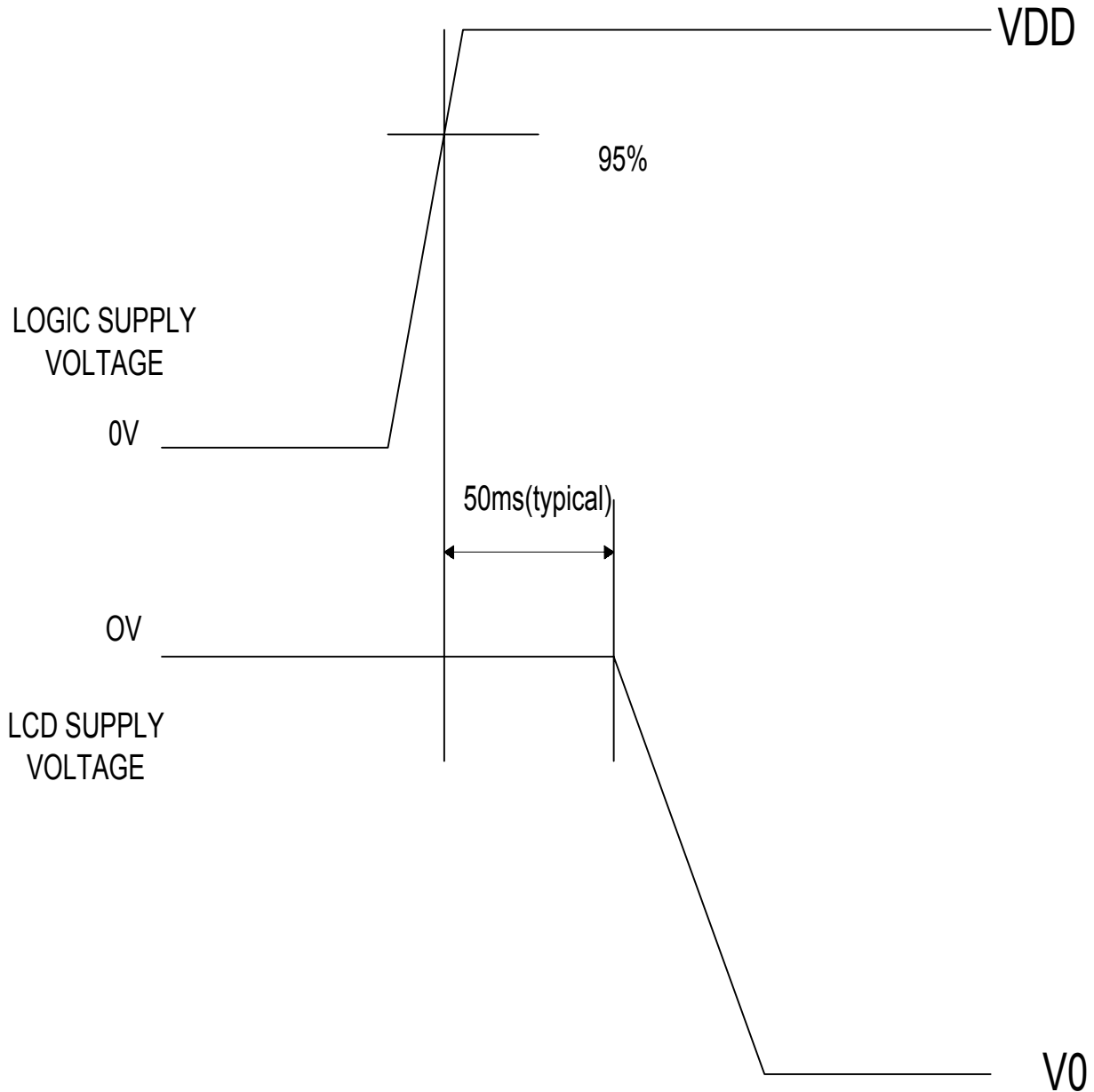


Figure 3: Timing Diagram of VDD Against V0.

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