TZA3036
SDH/SONET STM1/OC3 transimpedance amplifier

Rev. 01 — 24 March 2006　　　　　　　　　　　　　**Product data sheet**

1. General description

The TZA3036 is a transimpedance amplifier with Automatic Gain Control (AGC), designed to be used in STM1/OC3 fiber optic links. It amplifies the current generated by a photo detector (PIN diode or avalanche photodiode) and converts it to a differential output voltage. It offers a current mirror of average photo current for RSSI monitoring to be used in SFF-8472 compliant modules.

The low noise characteristics makes it suitable for STM1/OC3 applications, but also for FTTx applications.

CAUTION
⚠ This device is sensitive to ElectroStatic Discharge (ESD). Therefore care should be taken during transport and handling.

2. Features

- Low equivalent input noise, typically 12 nA (RMS)
- Wide dynamic range, typically 0.18 μA to 1.5 mA (p-p)
- Differential transimpedance of 69 kΩ (typical)
- Bandwidth from DC to 160 MHz (typical)
- Differential outputs
- On-chip (AGC) with possibility of external control
- Single supply voltage 3.3 V; range 2.9 V to 3.6 V
- Bias voltage for PIN diode
- On-chip current mirror of average photo current for RSSI monitoring
- Identical ports available on both sides of die for easy bond layout and RF polarity selection

3. Applications

- Digital fiber optic receiver modules in telecommunications transmission systems, in high speed data networks or in FTTx systems.

PHILIPS

4. Ordering information

Table 1.   Ordering information

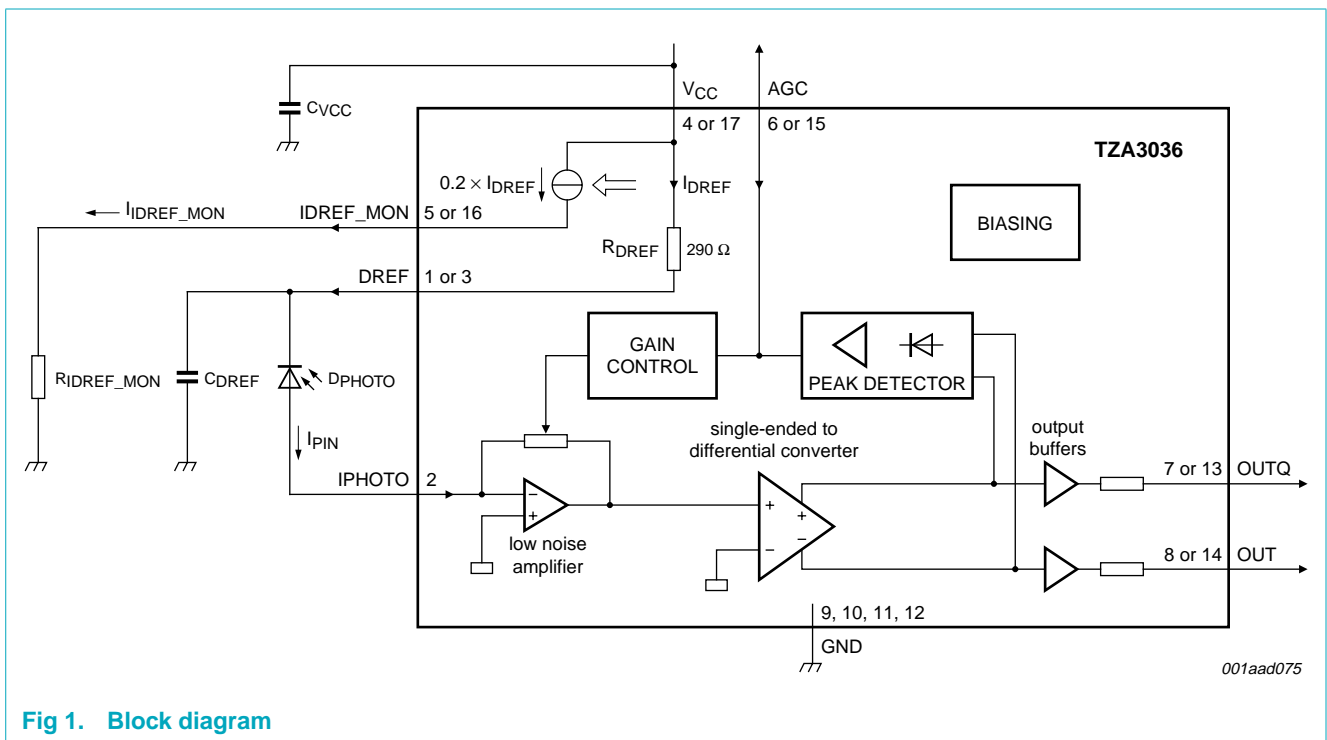| Type number	Package		
	Name	**Description**	**Version**
TZA3036U	-	bare die, dimensions approximately 0.82 mm × 1.3 mm	-

5. Block diagram

Fig 1.   Block diagram

6. Pinning information
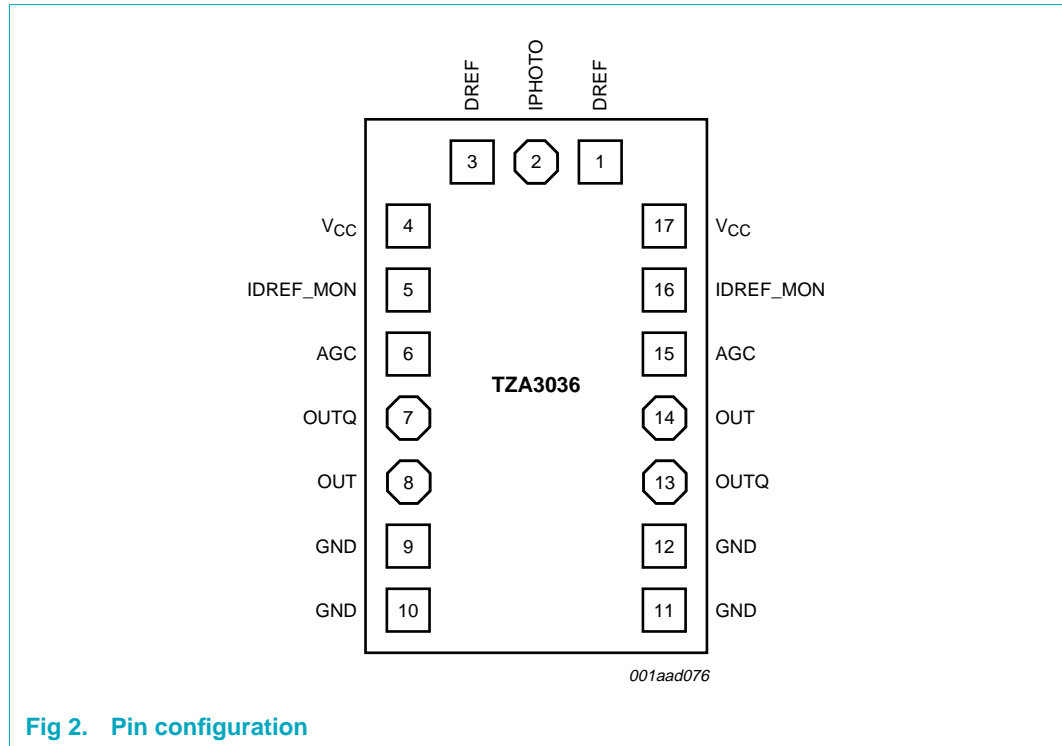
6.1 Pinning

Fig 2. Pin configuration

6.2 Pin description

Table 2.   Bonding pad description

Bonding pad locations with respect to the center of the die (see Figure 10); X and Y are in μm.

Symbol	Pad	X	Y	Type	Description
DREF	1	−493.6	140	output	bias voltage output for PIN diode; connect cathode of PIN diode to pad 1 or pad 3
IPHOTO	2	−493.6	0	input	current input; anode of PIN diode should be connected to this pad
DREF	3	−493.6	−140	output	bias voltage output for PIN diode; connect cathode of PIN diode to pad 1 or pad 3
V_{CC}	4	−353.6	−278.6	supply	supply voltage; connect supply to pad 4 or pad 17
IDREF_MON	5	−213.6	−278.6	output	current output for RSSI measurements; connect a resistor to pad 5 or pad 16 and ground
AGC	6	−73.6	−278.6	input	AGC voltage; use pad 6 or pad 15
OUTQ	7	66.4	−278.6	output	data output; complement of pad OUT; use pad 7 or pad 13
OUT	8	206.4	−278.6	output	data output; use pad 8 or pad 14 [1]
GND	9	346.4	−278.6	ground	ground; connect together pads 9, 10, 11 and 12 as many as possible
GND	10	486.4	−278.6	ground	ground; connect together pads 9, 10, 11 and 12 as many as possible

TZA3036_1

Product data sheet

Rev. 01 — 24 March 2006

3 of 15

Table 2. **Bonding pad description** …*continued*
Bonding pad locations with respect to the center of the die (see *Figure 10*); X and Y are in μm.

Symbol	Pad	X	Y	Type	Description
GND	11	486.4	278.6	ground	ground; connect together pads 9, 10, 11 and 12 as many as possible
GND	12	346.4	278.6	ground	ground; connect together pads 9, 10, 11 and 12 as many as possible
OUTQ	13	206.4	278.6	output	data output; complement of pad OUT; use pad 7 or pad 13
OUT	14	66.4	278.6	output	data output; use pad 8 or pad 14 [1]
AGC	15	−73.6	278.6	input	AGC voltage; use pad 6 or pad 15
IDREF_MON	16	−213.6	278.6	output	current output for RSSI measurements; connect a resistor to pad 5 or pad 16 and ground
V_{CC}	17	−353.6	278.6	supply	supply voltage; connect supply to pad 4 or pad 17

[1] These pads go HIGH when current flows into pad IPHOTO.

7. Functional description

The TZA3036 is a TransImpedance Amplifier (TIA) intended for use in fiber optic links for signal recovery in STM1/OC3 or FTTx applications. It amplifies the current generated by a photo detector (PIN diode or avalanche photodiode) and converts it to a differential output voltage.

The most important characteristics of the TZA3036 are high receiver sensitivity, wide dynamic range and large bandwidth. Excellent receiver sensitivity is achieved by minimizing transimpedance amplifier noise.

The TZA3036 has a wide dynamic range to handle the signal current generated by the PIN diode which can vary from 0.18 μA to 1.5 mA (p-p). This is implemented by an AGC loop which reduces the preamplifier feedback resistance so that the amplifier remains linear over the whole input range. The AGC loop hold capacitor is integrated on-chip, so an external capacitor is not required.

The bandwidth of TZA3036 is optimized for STM1/OC3 application. It works from DC onward due to the absence of offset control loops. This allows for excellent performance regardless of signal content (long sequences of identical bits can be converted). A differential amplifier converts the output of the preamplifier to a differential voltage.

7.1 PIN diode connections

The performance of an optical receiver is largely determined by the combined effect of the transimpedance amplifier and the PIN diode. In particular, the method used to connect the PIN diode to the input (pad IPHOTO) and the layout around the input pad strongly influences the main parameters of a transimpedance amplifier, such as sensitivity, bandwidth, and PSRR.

Sensitivity is most affected by the value of the total capacitance at the input pad. Therefore, to obtain the highest possible sensitivity the total capacitance should be as low as possible.

The parasitic capacitance can be minimized through:

1. Reducing the capacitance of the PIN diode. This is achieved by proper choice of PIN diode and typically a high reverse voltage.

2. Reducing the parasitics around the input pad. This is achieved by placing the PIN diode as close as possible to the TIA.

The PIN diode can be biased with a positive or a negative voltage. Figure 3 shows the PIN diode biased positively, using the on-chip bias pad DREF. The voltage at DREF is derived from V_{CC} by a low-pass filter comprising internal resistor R_{DREF} and external capacitor C2 which decouples any supply voltage noise. The value of external capacitor C2 affects the value of PSRR and should have a minimum value of 470 pF. Increasing this value improves the value of PSRR. The current through R_{DREF} is measured and sourced at pad IDREF_MON, see Section 7.3.

If the biasing for the PIN diode is done external to the IC, pad DREF can be left unconnected. If a negative bias voltage is used, the configuration shown in Figure 4 can be used. In this configuration, the direction of the signal current is reversed to that shown in Figure 3. It is essential that in these applications, the PIN diode bias voltage is filtered to achieve the best sensitivity.

For maximum freedom on bonding location, 2 outputs are available for DREF (pads 1 and 3). These are internally connected. Both outputs can be used if necessary. If only one is used, the other can be left open.
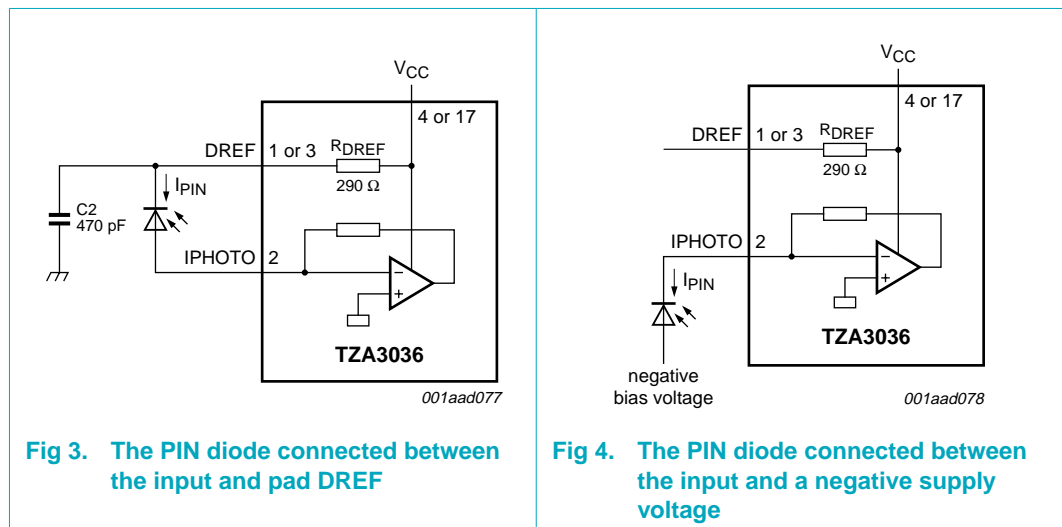

Fig 3. **The PIN diode connected between the input and pad DREF**

Fig 4. **The PIN diode connected between the input and a negative supply voltage**

7.2 Automatic gain control

The TZA3036 transimpedance amplifier can handle input currents from 0.18 µA to 1.5 mA which is equivalent to a dynamic range of 78 dB (electrical equivalent with 39 dB optical). At low input currents, the transimpedance must be high to obtain enough output voltage, and the noise should be low enough to guarantee a minimum bit error rate. At high input currents however, the transimpedance should be low to prevent excessive distortion at the output stage. To achieve the dynamic range, the gain of the amplifier depends on the level of the input signal. This is achieved in the TZA3036 by an AGC loop.

The AGC loop comprises a peak detector and a gain control circuit. The peak detector detects the amplitude of the signal and stores it in a hold capacitor. The hold capacitor voltage is compared to a threshold voltage. The AGC is only active when the input signal level is larger than the threshold level and is inactive when the input signal is smaller than the threshold level.

When the AGC is inactive, the transimpedance is at its maximum. When the AGC is active, the feedback resistor value of the transimpedance amplifier is reduced, reducing its transimpedance, to keep the output voltage constant. Figure 5 shows the transimpedance as function of the input current.

To reduce sensitivity to offsets and output loads, the AGC detector senses the output just before the output buffer. Figure 6 shows the AGC voltage as function of the input current.
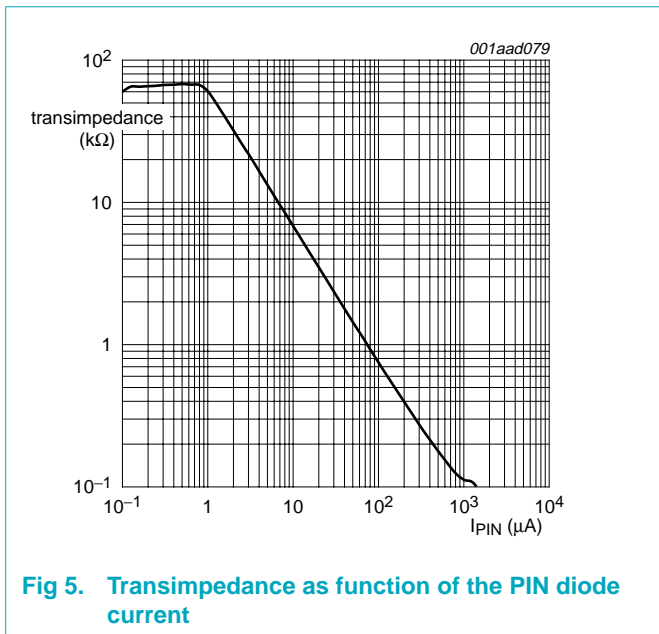

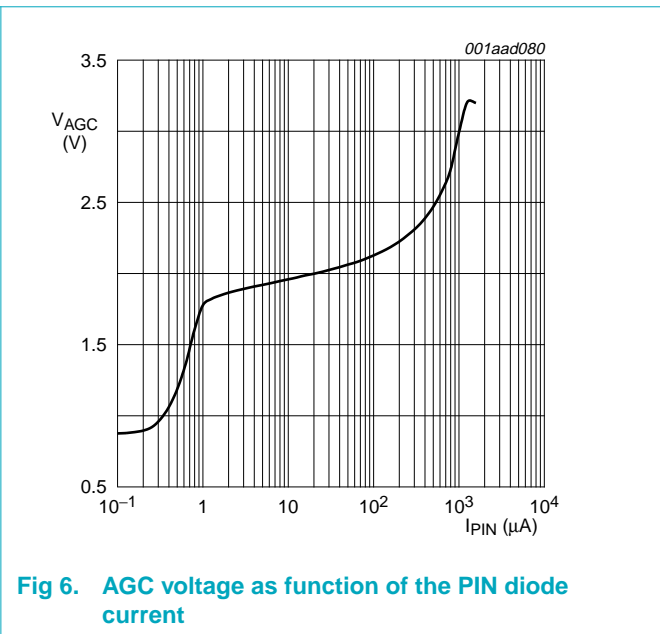**Fig 5. Transimpedance as function of the PIN diode current**

Fig 6. AGC voltage as function of the PIN diode current

For applications where the transimpedance is controlled by the TIA it is advised to leave the AGC pads unconnected to achieve fast attack and decay times.

The AGC function can be overruled by applying a voltage to pad AGC. In this configuration, connecting pad AGC to ground gives maximum transimpedance and connecting it to V_{CC} gives minimum transimpedance. This is depicted in Figure 7. The AGC voltage should be derived from the V_{CC} for proper functioning.

For maximum freedom on bonding location, 2 pads are available for AGC (pads 6 and 15). These pads are internally connected. Both pads can be used if necessary.
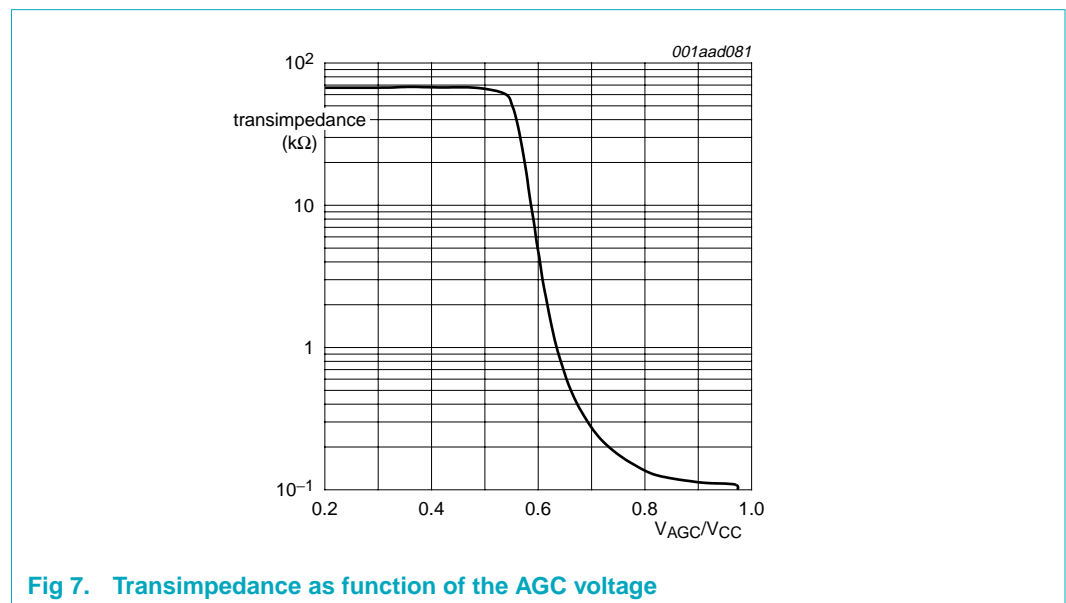

Fig 7. Transimpedance as function of the AGC voltage

7.3 Monitoring RSSI via IDREF_MON

To facilitate RSSI monitoring in modules (e.g. SFF-8472 compliant SFP modules), a current output is provided. This output gives a current which is 20 % of the average DREF current through the 290 Ω bias resistor. By connecting a resistor to the IDREF_MON output, a voltage proportional with to average input power can be obtained.

The RSSI monitoring is implemented by measuring the voltage over the 290 Ω bias resistor. This method is preferred over a simple current mirror because at small photo currents the voltage drop over the resistor is very small. This gives a higher bias voltage yielding better performance of the photodiode.

For maximum freedom on bonding location, 2 pads are available for IDREF_MON (pads 5 and 16). These pads are internally connected. Both pads can be used if necessary. If only one is used, the other can be left open.

TZA3036_1

Product data sheet

Rev. 01 — 24 March 2006

7 of 15

8. Limiting values

Table 3. Limiting values
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		−0.5	+3.8	V
V_n	voltage on any other pin	pad			
		IPHOTO	−0.5	+2.0	V
		OUT, OUTQ	−0.5	V_{CC} + 0.5	V
		AGC, IDREF_MON	−0.5	V_{CC} + 0.5	V
		DREF	−0.5	V_{CC} + 0.5	V
I_n	current on any other pin	pad			
		IPHOTO	−1	+2.5	mA
		OUT, OUTQ	−10	+10	mA
		AGC, IDREF_MON	−0.2	+0.2	mA
		DREF	−4.0	+4.0	mA
P_{tot}	total power dissipation		-	300	mW
T_{amb}	ambient temperature		−40	+85	°C
T_j	junction temperature		-	150	°C
T_{stg}	storage temperature		−65	+150	°C

9. Characteristics

Table 4. Characteristics
Typical values at T_j = 25 °C and V_{CC} = 3.3 V; minimum and maximum values are valid over the entire ambient temperature range and supply voltage range; all voltages are measured with respect to ground; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		2.9	3.3	3.6	V
I_{CC}	supply current	AC-coupled; $R_{L(dif)}$ = 100 Ω; excluding I_{DREF} and I_{IDREF_MON}	-	20	24	mA
P_{tot}	total power dissipation		-	66	87	mW
T_j	junction temperature		−40	-	+125	°C
T_{amb}	ambient temperature		−40	+25	+85	°C
R_{tr}	small-signal transresistance	measured differentially; AC-coupled, $R_{L(dif)}$ = 100 Ω	46	69	98	kΩ
$f_{-3dB(h)}$	high frequency −3 dB point	C_{PIN} = 0.7 pF	110	160	-	MHz
$I_{n(rms)(itg)(tot)}$	total integrated RMS noise current over bandwidth	referenced to input; C_{PIN} = 0.7 pF; $f_{-3dB(min)}$ = 110 MHz third-order Bessel filter [1]	-	12	16	nA
Automatic gain control loop: pad AGC						
t_{att}	attack time	AGC pad unconnected	-	10	-	µs
t_{decay}	decay time	AGC pad unconnected	-	40	-	µs
$V_{th(AGC)(p-p)}$	peak-to-peak AGC threshold voltage	referenced to output; measured differentially	-	125	-	mV

Table 4.   Characteristics …continued
Typical values at T_j = 25 °C and V_{CC} = 3.3 V; minimum and maximum values are valid over the entire ambient temperature range and supply voltage range; all voltages are measured with respect to ground; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Bias voltage: pad DREF						
$R_{(DREF-VCC)}$	resistance between pin DREF and pin V_{CC}	tested at DC level; T_{amb} = 25 °C	240	290	330	Ω
TC_{RDREF}	temperature coefficient of R_{DREF}		-	0.33	-	Ω/°C
Input: pad IPHOTO						
$I_{IPHOTO(p-p)}$	peak-to-peak current on pad IPHOTO		[2] −1000	-	+1500	µA
$V_{bias(i)}$	input bias voltage		-	-	900	mV
Monitor: pad IDREF_MON						
V_{mon}	monitor voltage		[1] 0	-	V_{CC} − 0.4	V
I_{IDREF_MON}/I_{DREF}	monitor current ratio	ratio I_{IDREF_MON} / I_{DREF}	19.5	20	20.5	%
$I_{offset(mon)}$	monitor offset current	T_{amb} = 25 °C	0	10	20	µA
$TC_{I(offset)mon}$	temperature coefficient of monitor offset current		-	30	-	nA/°C
Data outputs: pads OUT and OUTQ						
$V_{O(cm)}$	common mode output voltage	AC-coupled; $R_{L(dif)}$ = 100 Ω	-	V_{CC} − 1.2	-	V
$V_{o(dif)(p-p)}$	peak-to-peak differential output voltage	AC-coupled; $R_{L(dif)}$ = 100 Ω				
		I_{PIN} = 0.18 µA (p-p) × R_{tr}	8	12	-	mV
		I_{PIN} = 20 µA (p-p)	-	125	-	mV
		I_{PIN} = 1100 µA (p-p)	-	250	500	mV
$R_{O(dif)}$	differential output resistance	tested at DC level	-	100	-	Ω
t_r	rise time	20 % to 80 %; I_{PIN} = 100 µA (p-p)	-	800	-	ps
t_f	fall time	80 % to 20 %; I_{PIN} = 100 µA (p-p)	-	1000	-	ps

[1]   Guaranteed by design.

[2]   The input current range is determined by the allowed Pulse Width Distortion (PWD), which is < 5 % over the whole input current range.

The PWD is defined as: $PWD = \left(\dfrac{pulse\ width}{T} - (0.5)\right) \times 100$ % , where T is the clock period.

10. Application information

For maximum freedom on bonding location, 2 outputs are available for OUT and OUTQ. The outputs should be used in pairs: pad 14 with pad 7 or pad 8 with pad 13. Pad 8 is internally connected with pad 14, pad 7 is internally connected with pad 13. The device is guaranteed with only one pair used. The other pair should be left open. Two examples of the bonding possibilities are shown in Figure 8.
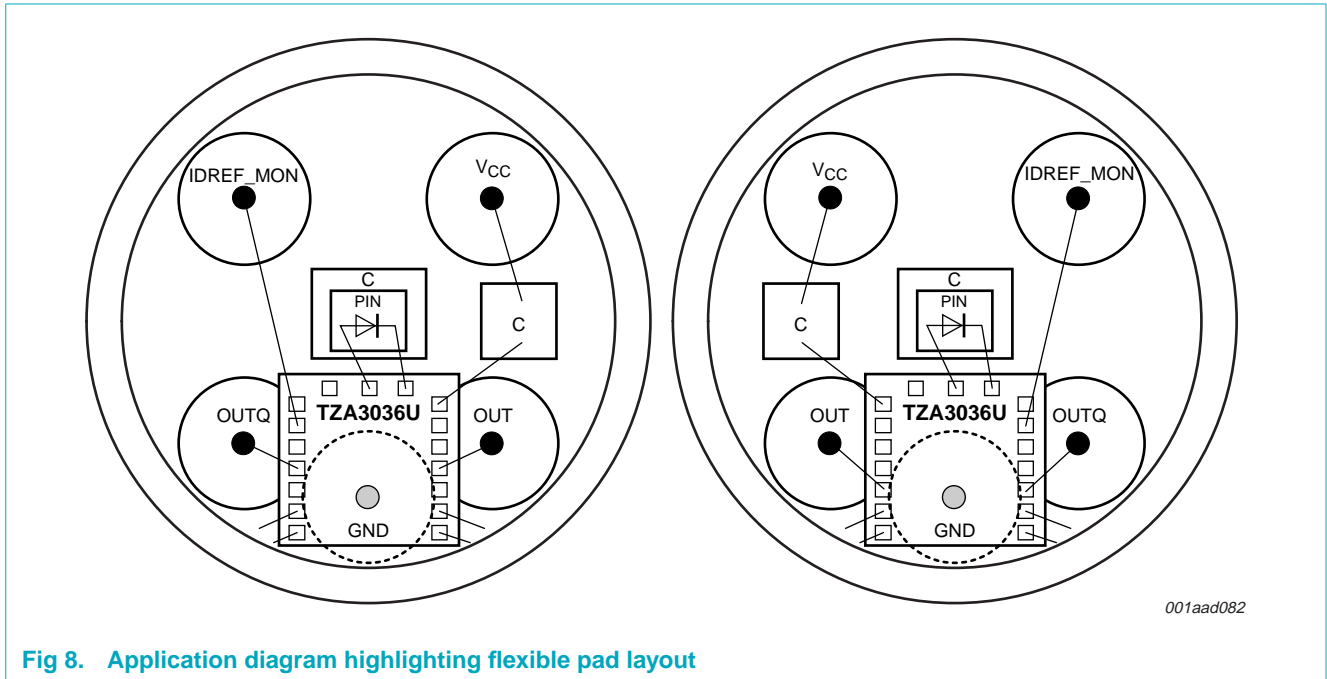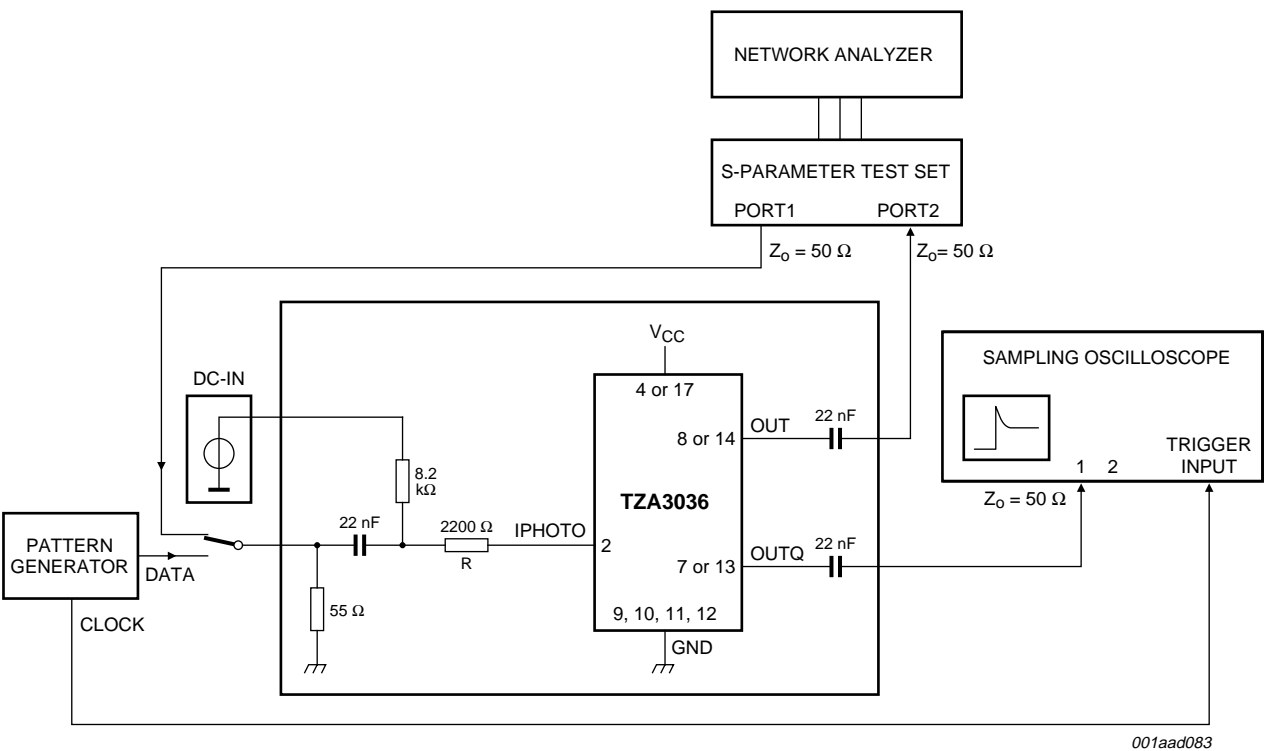

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Fig 8. Application diagram highlighting flexible pad layout

11. Test information

NETWORK ANALYZER

S-PARAMETER TEST SET

PORT1   PORT2

$Z_o = 50\ \Omega$ $Z_o = 50\ \Omega$

V_{CC}

SAMPLING OSCILLOSCOPE

DC-IN

4 or 17

8 or 14   OUT   22 nF

TRIGGER
INPUT

1   2

$Z_o = 50\ \Omega$

8.2
kΩ

PATTERN
GENERATOR

22 nF   2200 Ω   IPHOTO

TZA3036

DATA

R   2

7 or 13   OUTQ   22 nF

55 Ω

9, 10, 11, 12

CLOCK

GND

001aad083

Total impedance of the test circuit ($Z_{tot(tc)}$) is calculated by the equation $Z_{tot(tc)} = s_{21} \times (R + Z_i) \times 2$, where s_{21} is the insertion loss of ports 1 and 2.

Typical values: R = 2200 Ω, Z_i = 300 Ω.
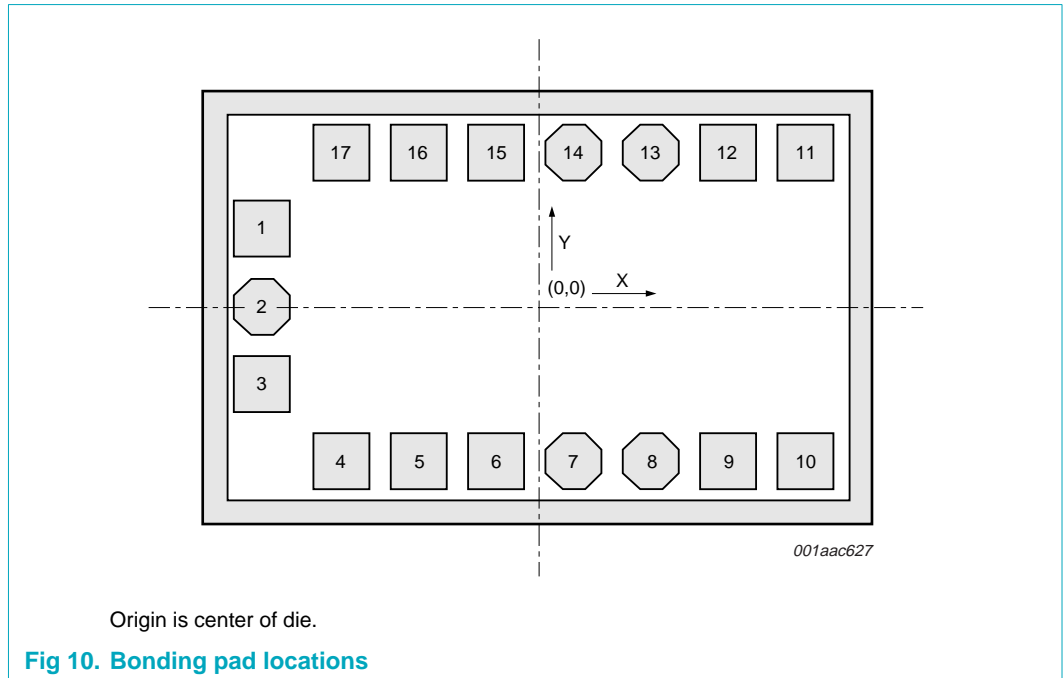
Fig 9.   Test circuit

12. Bare die information

Origin is center of die.

Fig 10. Bonding pad locations

Table 5.   Physical characteristics of the bare die

Parameter	Value
Glass passivation	0.3 μm PSG (PhosphoSilicate Glass) on top of 0.8 μm silicon nitride
Bonding pad dimension	minimum dimension of exposed metallization is 90 μm $\times$ 90 μm (pad size = 100 μm $\times$ 100 μm) except pads 2 and 3 which have exposed metallization of 80 μm $\times$ 80 μm (pad size = 90 μm $\times$ 90 μm)
Metallization	2.8 μm AlCu
Thickness	380 μm nominal
Die dimension	820 μm $\times$ 1300 μm ($\pm$ 20 μm^2)
Backing	silicon; electrically connected to GND potential through substrate contacts
Attach temperature	< 440 $^\circ$C; recommended die attach is glue
Attach time	< 15 s

13. Package outline

Not applicable.

14. Handling information

14.1 General

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be completely safe you must take normal precautions appropriate to handling MOS devices; see *JESD625-A and/or IEC61340-5*.

14.2 Additional information

Pad IPHOTO has limited protection to ensure good RF performance. This pad should be handled with extreme care.

15. Abbreviations

Table 6.   Abbreviations

Acronym	Description
SDH	Synchronous Digital Hierarchy
SONET	Synchronous Optical NETwork
RSSI	Received Signal Strength Indicator
FTTx	Fiber To The "x"
STM1	Synchronous Transport Mode 1 (155.52 Mbit/s)
OC3	Optical Carrier level 3 (155.52 Mbit/s)
PIN	Positive Intrinsic Negative
PSRR	Power Supply Rejection Ratio

16. Revision history

Table 7.   Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
TZA3036_1	20060324	Product data sheet	-	-

TZA3036_1

Product data sheet   Rev. 01 — 24 March 2006   13 of 15

17. Legal information

17.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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TZA3036_1

Product data sheet   **Rev. 01 — 24 March 2006**   **14 of 15**

19. Contents