# Product Preview **Dual Transistor - Power Management** NPN/PNP Dual (Complimentary)

- Low  $V_{CE(SAT)}$ , < 0.5 V
- This is a Pb–Free Device

### MAXIMUM RATINGS

Q1

Rating	Symbol	Value	Unit
Collector-Base Voltage	V <sub>CBO</sub>	50	Vdc
Collector-Emitter Voltage	V <sub>CEO</sub>	50	Vdc
Collector Current	۱ <sub>C</sub>	100	mAdc

Q2

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V <sub>CEO</sub>	-60	V
Collector-Base Voltage	V <sub>CBO</sub>	-50	V
Emitter-Base Voltage	V <sub>EBO</sub>	-6.0	V
Collector Current – Continuous	Ι <sub>C</sub>	-100	mAdc

#### THERMAL CHARACTERISTICS

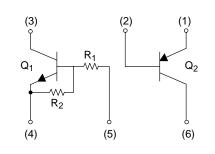
Characteristic (One Junction Heated)	Symbol	Мах	Unit
Total Device Dissipation $T_A = 25^{\circ}C$	PD	357	mW
Derate above 25°C		(Note 1) 2.9 (Note 1)	mW/°C
Thermal Resistance, Junction-to-Ambient	$R_{\thetaJA}$	350 (Note 1)	°C/W
Characteristic			
(Both Junctions Heated)	Symbol	Max	Unit
(Both Junctions Heated) Total Device Dissipation $T_A = 25^{\circ}C$	Symbol P <sub>D</sub>	500	Unit mW
Total Device Dissipation $T_A = 25^{\circ}C$	-	500 (Note 1)	mW
, ,	-	500	•
Total Device Dissipation $T_A = 25^{\circ}C$	-	500 (Note 1) 4.0	mW
Total Device Dissipation $T_A = 25^{\circ}C$ Derate above $25^{\circ}C$ Thermal Resistance,	PD	500 (Note 1) 4.0 (Note 1) 250	mW mW/°C

1. FR-4 @ Minimum Pad.



# ON Semiconductor®

http://onsemi.com





CASE 463A PLASTIC

### MARKING DIAGRAM



UW = Specific Device Code D = Date Code

#### **ORDERING INFORMATION**

Device	Package	Shipping†
EMF23XV6T5	SOT-563	2 mm Pitch 8000/Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

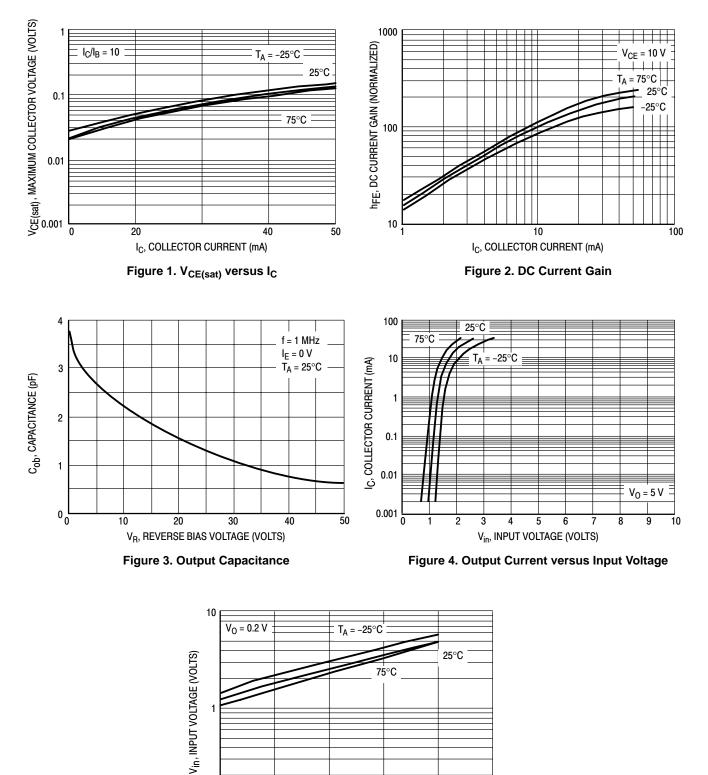
This document contains information on a product under development. ON Semiconductor reserves the right to change or discontinue this product without notice.

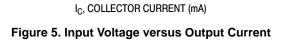
# **ELECTRICAL CHARACTERISTICS** (T<sub>A</sub> = $25^{\circ}$ C)

Characteristic	Symbol	Min	Тур	Max	Unit
Q1: NPN					
Collector-Base Cutoff Current ( $V_{CB} = 50 \text{ V}, I_E = 0$ )	I <sub>CBO</sub>	_	-	100	nAdc
Collector-Emitter Cutoff Current ( $V_{CE} = 50 \text{ V}, I_B = 0$ )	I <sub>CEO</sub>	_	-	500	nAdc
Emitter-Base Cutoff Current (V <sub>EB</sub> = 6.0 V, $I_C$ = 0)	I <sub>EBO</sub>	-	-	0.5	mAdc
Collector-Base Breakdown Voltage ( $I_C = 10 \ \mu A$ , $I_E = 0$ )	V <sub>(BR)CBO</sub>	50	-	-	Vdc
Collector-Emitter Breakdown Voltage (Note 3) (I <sub>C</sub> = 2.0 mA, I <sub>B</sub> = 0)	V <sub>(BR)CEO</sub>	50	-	-	Vdc
DC Current Gain ( $V_{CE}$ = 10 V, $I_C$ = 5.0 mA)	h <sub>FE</sub>	35	60	-	-
Collector-Emitter Saturation Voltage ( $I_C = 10 \text{ mA}, I_B = 0.3 \text{ mA}$ )	V <sub>CE(sat)</sub>	-	-	0.25	Vdc
Output Voltage (on) (V_{CC} = 5.0 V, V_B = 2.5 V, R_L = 1.0 k\Omega)	V <sub>OL</sub>	-	-	0.2	Vdc
Output Voltage (off) (V_{CC} = 5.0 V, V_B = 0.5 V, R_L = 1.0 k\Omega)	V <sub>OH</sub>	4.9	-	-	Vdc
Input Resistor	R1	7.0	10	13	kΩ
Resistor Ratio	R1/R2	0.8	1.0	1.2	-
Q2: PNP					
Collector–Base Breakdown Voltage ( $I_C = -50 \ \mu Adc$ , $I_E = 0$ )	V <sub>(BR)CBO</sub>	-60	-	-	Vdc
Collector–Emitter Breakdown Voltage ( $I_C = -1.0$ mAdc, $I_B = 0$ )	V <sub>(BR)CEO</sub>	-50	-	-	Vdc
Emitter–Base Breakdown Voltage (I <sub>E</sub> = $-50 \ \mu$ Adc, I <sub>E</sub> = 0)	V <sub>(BR)EBO</sub>	-6.0	-	-	Vdc
Collector–Base Cutoff Current ( $V_{CB} = -30$ Vdc, $I_E = 0$ )	I <sub>CBO</sub>	_	-	-0.5	nA
Emitter–Base Cutoff Current ( $V_{EB} = -5.0 \text{ Vdc}, I_B = 0$ )	I <sub>EBO</sub>	_	-	-0.5	μΑ
Collector–Emitter Saturation Voltage (Note 3) ( $I_C = -50$ mAdc, $I_B = -5.0$ mAdc)	V <sub>CE(sat)</sub>	_	-	-0.5	Vdc
DC Current Gain (Note 3) ( $V_{CE} = -6.0$ Vdc, $I_C = -1.0$ mAdc)	h <sub>FE</sub>	120	-	560	-
Transition Frequency (V <sub>CE</sub> = $-12$ Vdc, I <sub>C</sub> = $-2.0$ mAdc, f = $30$ MHz)	f <sub>T</sub>	_	140	-	MHz
Output Capacitance ( $V_{CB} = -12$ Vdc, $I_E = 0$ Adc, $f = 1.0$ MHz)	C <sub>OB</sub>	-	3.5	-	pF

2. Device mounted on a FR-4 glass epoxy printed circuit board using the minimum recommended footprint. 3. Pulse Test: Pulse Width  $\leq$  300 µs, D.C.  $\leq$  2%.

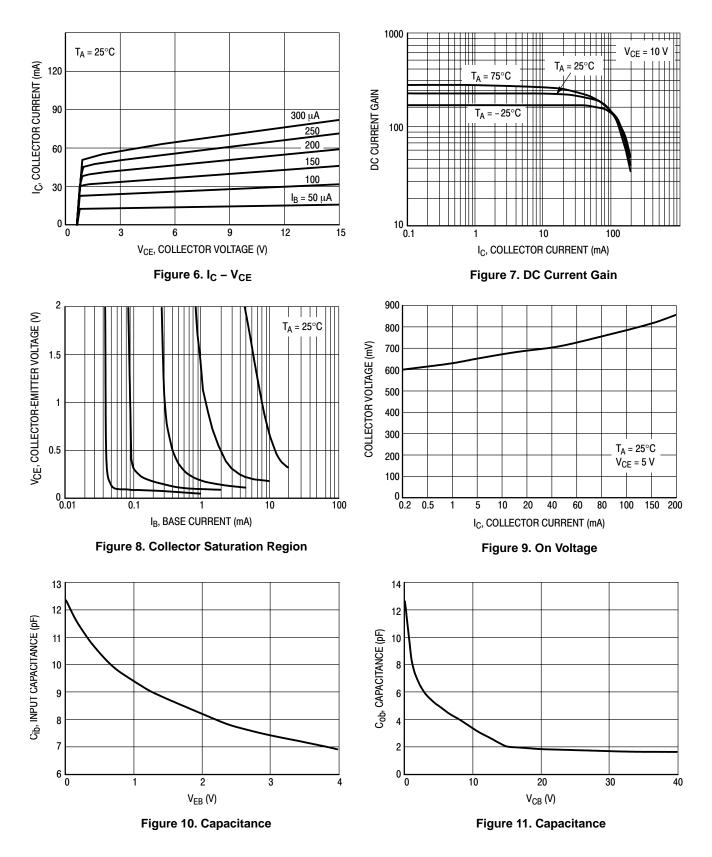
## **TYPICAL ELECTRICAL CHARACTERISTICS — Q1, NPN**





0.1 ∟ 

## **TYPICAL ELECTRICAL CHARACTERISTICS – Q2, PNP**



#### PACKAGE DIMENSIONS

SOT-563, 6 LEAD CASE 463A-01 **ISSUE A** 

Α С -X-Κ 5 4 6 B S -Y-01 2 3 世 > D 6 PL → G 🖛 ⊕ 0.08 (0.003) M X Y

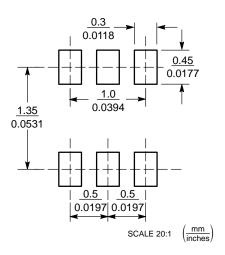
NOTES:

NOTES: 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982. 2. CONTROLLING DIMENSION: MILLIMETERS 3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.

	MILLIMETERS		INC	HES
DIM	MIN	MAX	MIN	MAX
Α	1.50	1.70	0.059	0.067
в	1.10	1.30	0.043	0.051
c	0.50	0.60	0.020	0.024
D	0.17	0.27	0.007	0.011
G	0.50 BSC		0.020	BSC
J	0.08	0.18	0.003	0.007
κ	0.10	0.30	0.004	0.012
S	1.50	1.70	0.059	0.067



#### **SOLDERING FOOTPRINT\***



#### SOT-563

\*For additional information on our Pb–Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

ON Semiconductor and are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any provided in SCILLC data sheets and/or specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and o vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer applications by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other application in which the FSCILLC product caude the SCILLC product caude cause may used user. Should Buyer purchase or uses SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

#### PUBLICATION ORDERING INFORMATION

#### LITERATURE FULFILLMENT:

Literature Distribution Center for ON Semiconductor P.O. Box 5163, Denver, Colorado 80217 USA Phone: 303–675–2175 or 800–344–3860 Toll Free USA/Canada Fax: 303–675–2176 or 800–344–3867 Toll Free USA/Canada Email: orderlit@onsemi.com

N. American Technical Support: 800–282–9855 Toll Free USA/Canada

Japan: ON Semiconductor, Japan Customer Focus Center 2–9–1 Kamimeguro, Meguro–ku, Tokyo, Japan 153–0051 Phone: 81–3–5773–3850 ON Semiconductor Website: http://onsemi.com

Order Literature: http://www.onsemi.com/litorder

For additional information, please contact your local Sales Representative.