HAT3010R

Silicon N/P Channel Power MOS FET
High Speed Power Switching

HITACHI

ADE-208-1402F (Z)

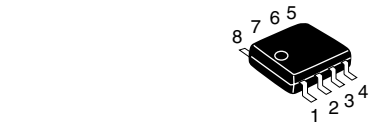
7th. Edition
Feb. 2002

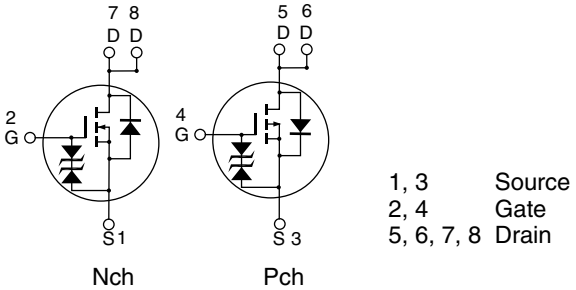
Features

- Low on-resistance
- Capable of 4.5 V gate drive
- High density mounting

Outline

SOP-8





1, 3	Source
2, 4	Gate
5, 6, 7, 8	Drain

Hitachi semiconductor

Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings		Unit
		Nch	Pch	
Drain to source voltage	V_{DSS}	60	–60	V
Gate to source voltage	V_{GSS}	±20	±20	V
Drain current	I_D	6	–5	A
Drain peak current	$I_{D(pulse)}$ Note1	48	–40	A
Body-drain diode reverse drain current	I_{DR}	6	–5	A
Channel dissipation	Pch Note2	2	2	W
Channel dissipation	Pch Note3	3	3	W
Channel temperature	Tch	150	150	°C
Storage temperature	Tstg	–55 to +150	–55 to +150	°C

Notes: 1. PW ≤ 10µs, duty cycle ≤ 1 %
2. 1 Drive operation; When using the glass epoxy board (FR4 40 x 40 x 1.6 mm), PW ≤ 10s
3. 2 Drive operation; When using the glass epoxy board (FR4 40 x 40 x 1.6 mm), PW ≤ 10s

Electrical Characteristics (Ta = 25°C)

• N Channel

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	60	—	—	V	I_D = 10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±20	—	—	V	I_G = ±100 µA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	±10	µA	V_{GS} = ±16 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	1	µA	V_{DS} = 60 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	1.0	—	2.5	V	V_{DS} = 10 V, I_D = 1 mA
Static drain to source on state resistance	$R_{DS(on)}$	—	30	38	mΩ	I_D = 3 A, V_{GS} = 10 V [Note4]
	$R_{DS(on)}$	—	40	60	mΩ	I_D = 3 A, V_{GS} = 4.5 V [Note4]
Forward transfer admittance	$\|y_{fs}\|$	7	11	—	S	I_D = 3 A, V_{DS} = 10 V [Note4]
Input capacitance	Ciss	—	1050	—	pF	V_{DS} = 10 V
Output capacitance	Coss	—	150	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	90	—	pF	f = 1 MHz
Turn-on delay time	$t_{d(on)}$	—	15	—	ns	V_{GS} = 10 V, I_D = 3 A
Rise time	t_r	—	15	—	ns	V_{DD} ≈ 30 V
Turn-off delay time	$t_{d(off)}$	—	55	—	ns	R_L = 10 Ω
Fall time	t_f	—	10	—	ns	R_g = 4.7 Ω
Body–drain diode forward voltage	V_{DF}	—	0.85	1.10	V	IF = 6 A, V_{GS} = 0 [Note4]
Body–drain diode reverse recovery time	t_{rr}	—	50	—	ns	IF = 6 A, V_{GS} = 0 diF/ dt = 100 A/µs

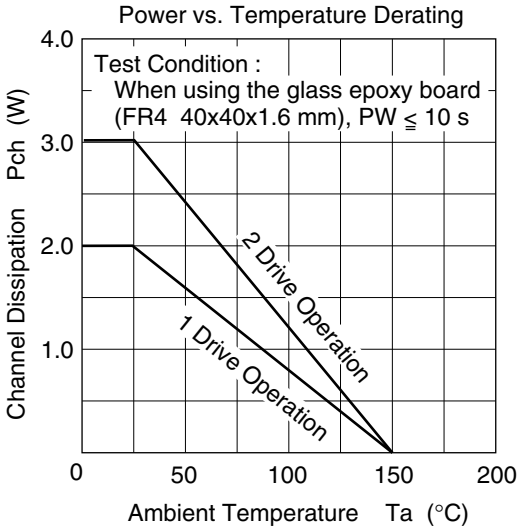
Notes: 5. Pulse test

• P Channel

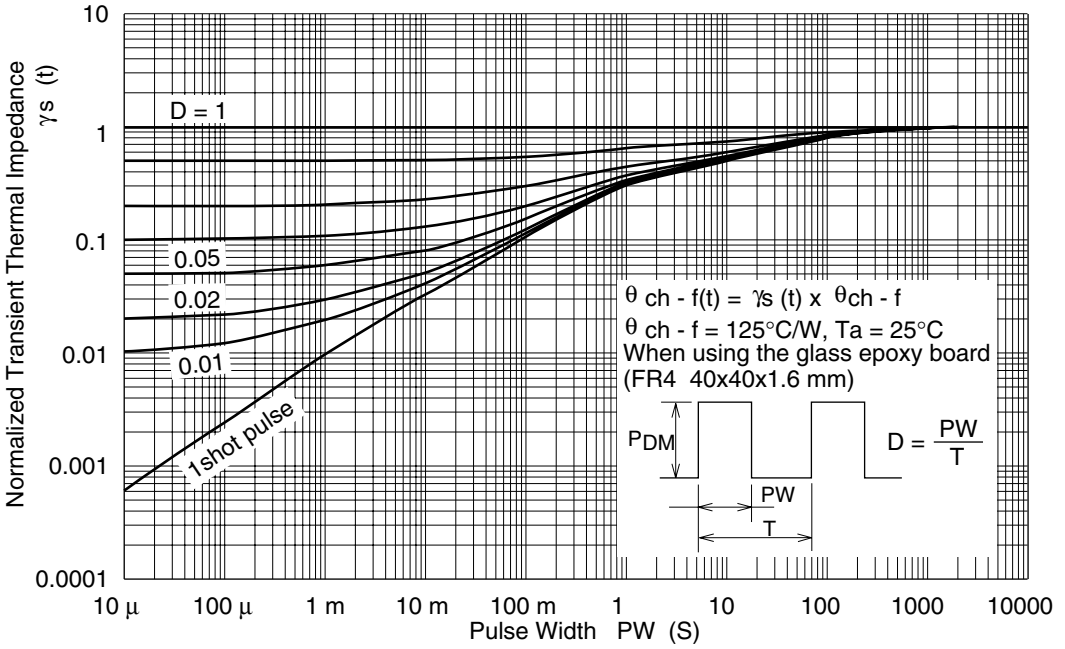
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	–60	—	—	V	I_D = –10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±20	—	—	V	I_G = ±100 µA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	±10	µA	V_{GS} = ±16 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	–1	µA	V_{DS} = –60 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	–1.0	—	–2.5	V	V_{DS} = –10 V, I_D = –1 mA
Static drain to source on state resistance	$R_{DS(on)}$	—	60	76	mΩ	I_D = –2.5 A, V_{GS} = –10 V [Note4]
	$R_{DS(on)}$	—	90	130	mΩ	I_D = –2.5 A, V_{GS} = –4.5 V [Note4]
Forward transfer admittance	$\|y_{fs}\|$	3	5	—	S	I_D = –2.5 A, V_{DS} = –10 V [Note4]
Input capacitance	Ciss	—	1350	—	pF	V_{DS} = –10 V
Output capacitance	Coss	—	135	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	85	—	pF	f = 1 MHz
Turn-on delay time	$t_{d(on)}$	—	20	—	ns	V_{GS} = –10 V, I_D = –2.5 A
Rise time	t_r	—	15	—	ns	$V_{DD} \approx$ –30 V
Turn-off delay time	$t_{d(off)}$	—	55	—	ns	R_L = 12 Ω
Fall time	t_f	—	10	—	ns	R_g = 4.7 Ω
Body–drain diode forward voltage	V_{DF}	—	-0.85	-1.10	V	IF = –5 A, V_{GS} = 0 [Note4]
Body–drain diode reverse recovery time	t_{rr}	—	50	—	ns	IF = –5 A, V_{GS} = 0 diF/ dt = 100 A/µs

Notes: 5. Pulse test

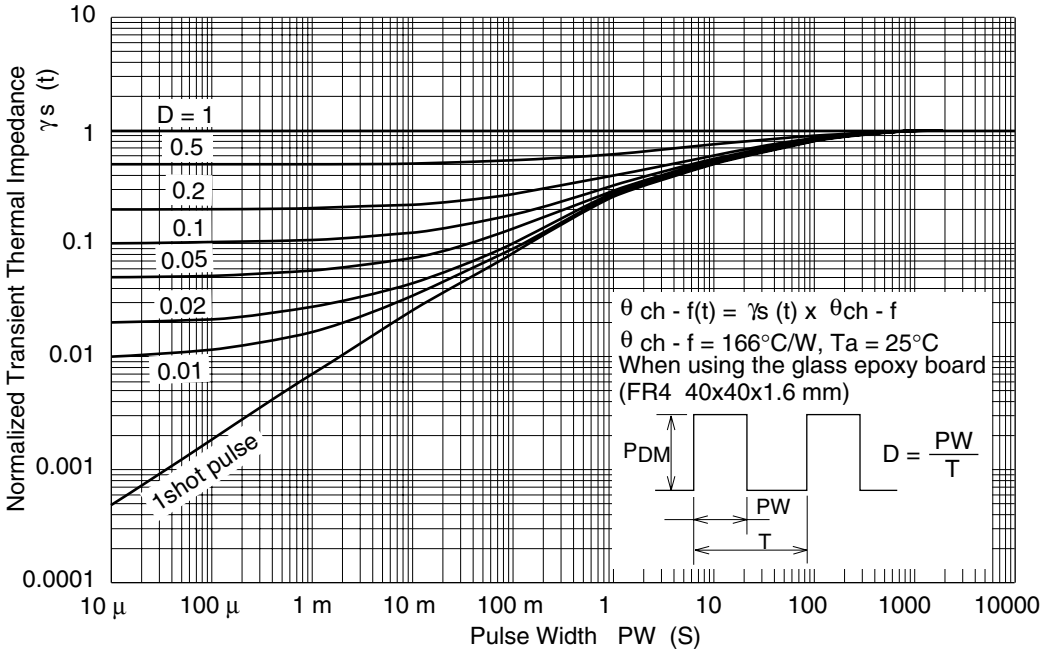
Main Characteristics



Normalized Transient Thermal Impedance vs. Pulse Width (1 Drive Operation)

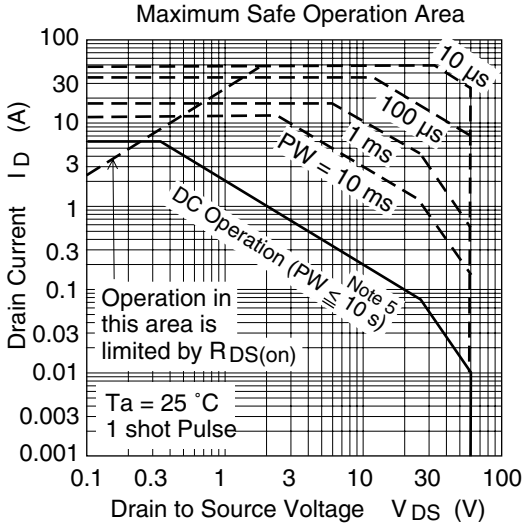


Normalized Transient Thermal Impedance vs. Pulse Width (2 Drive Operation)

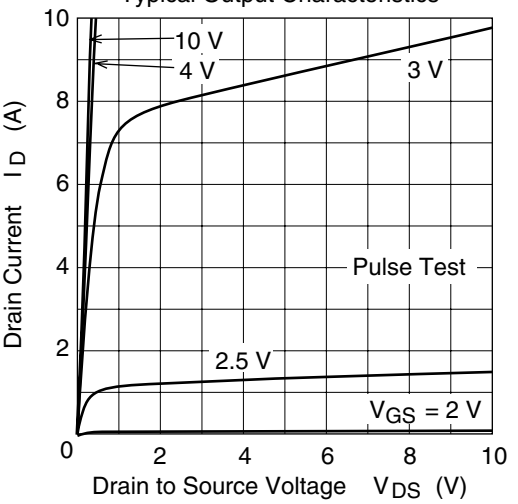


• **N Channel**

Maximum Safe Operation Area

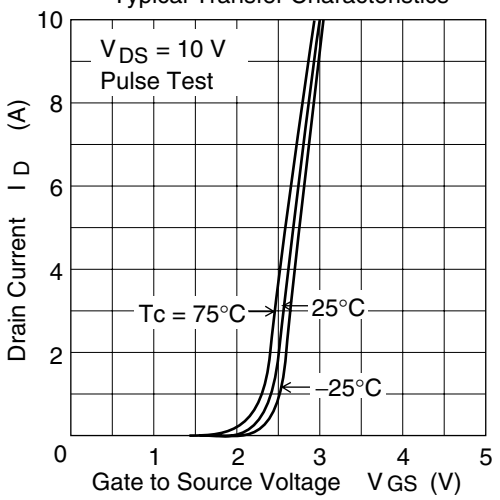


Typical Output Characteristics

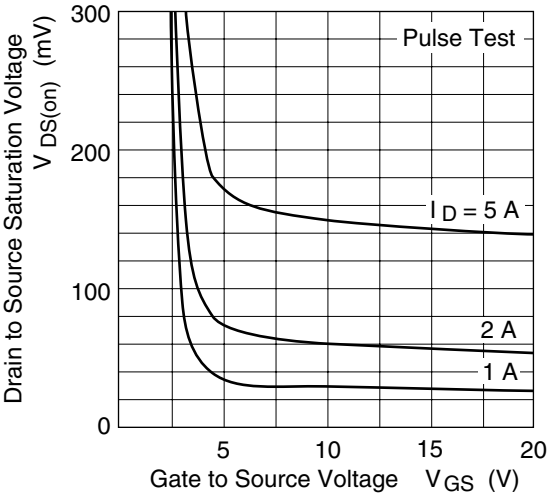


Note 5 :
When using the glass epoxy board
(FR4 40x40x1.6 mm)

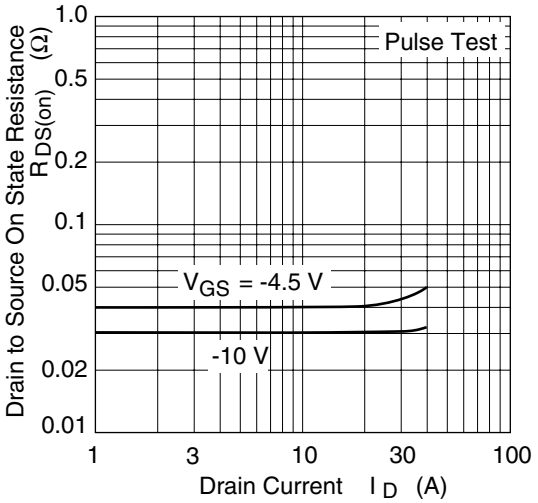
Typical Transfer Characteristics



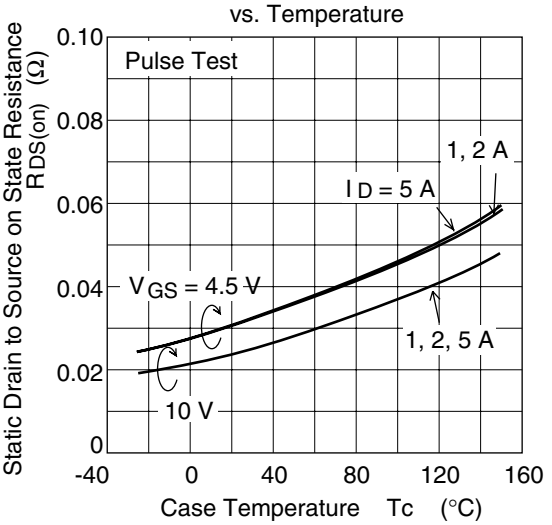
Drain to Source Saturation Voltage vs.
Gate to Source Voltage



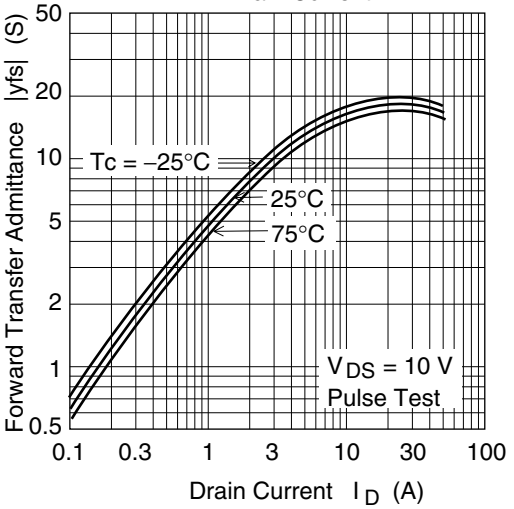
Static Drain to Source on State Resistance vs. Drain Current



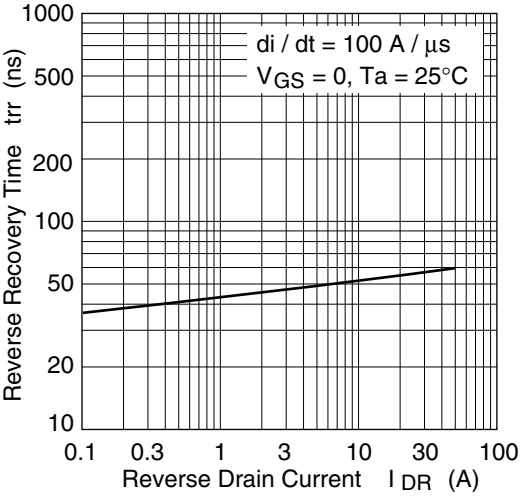
Static Drain to Source on State Resistance vs. Temperature



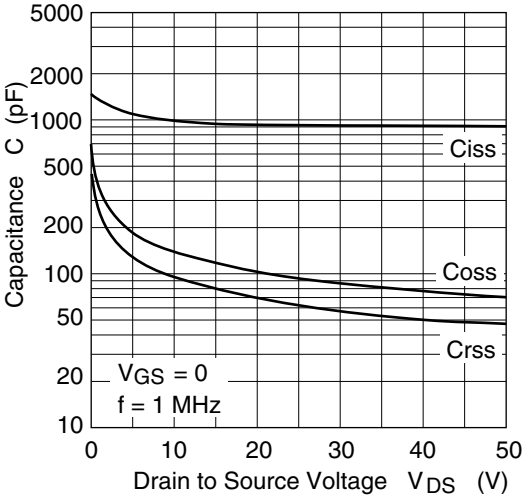
Forward Transfer Admittance vs. Drain Current



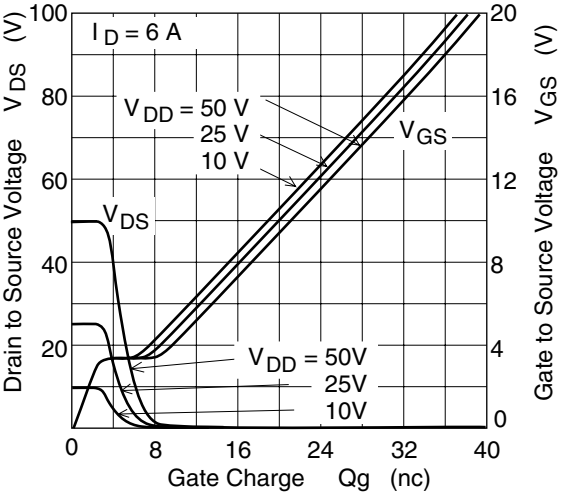
Body-Drain Diode Reverse Recovery Time



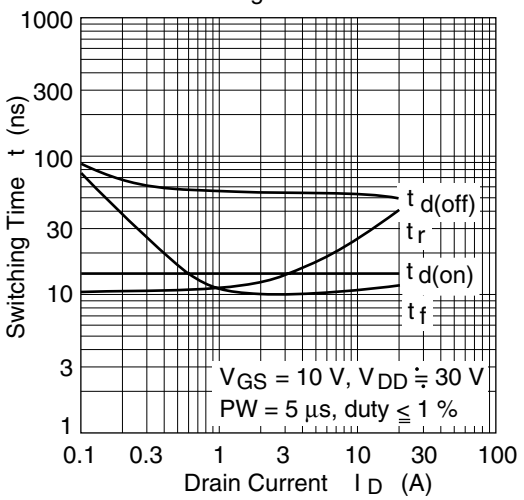
Typical Capacitance vs.
Drain to Source Voltage



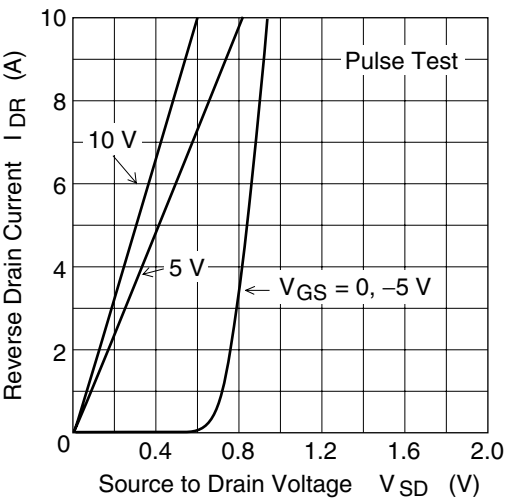
Dynamic Input Characteristics



Switching Characteristics

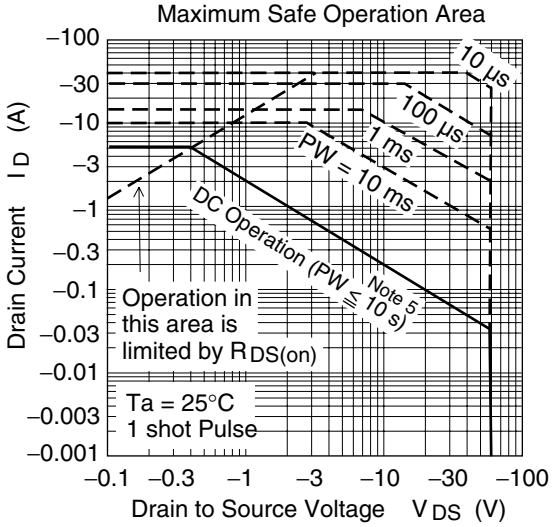


Reverse Drain Current vs.
Souece to Drain Voltage

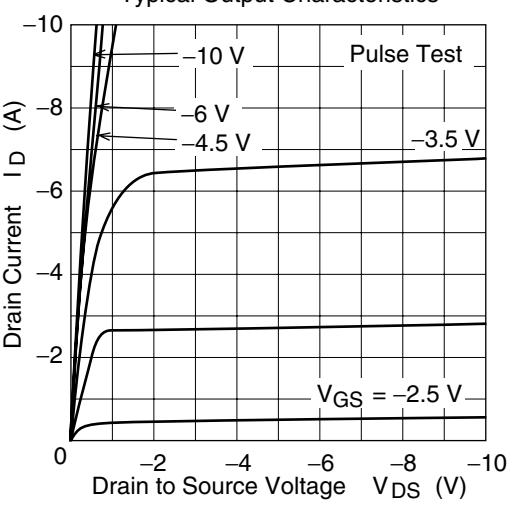


• **P Channel**

Maximum Safe Operation Area

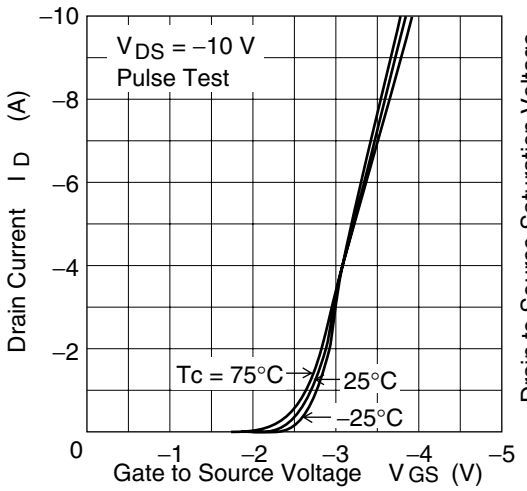


Typical Output Characteristics

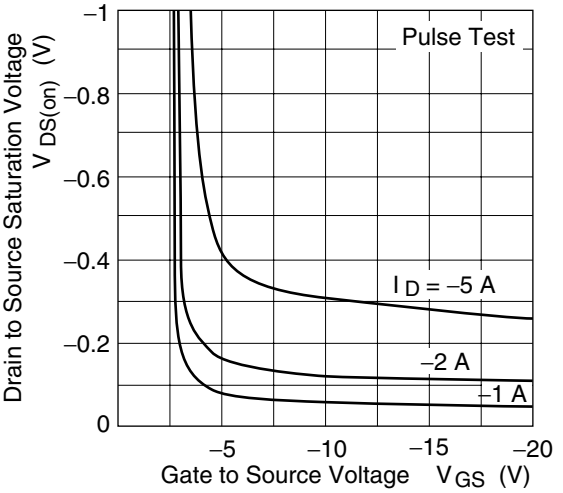


Note 5 :
When using the glass epoxy board
(FR4 40x40x1.6 mm)

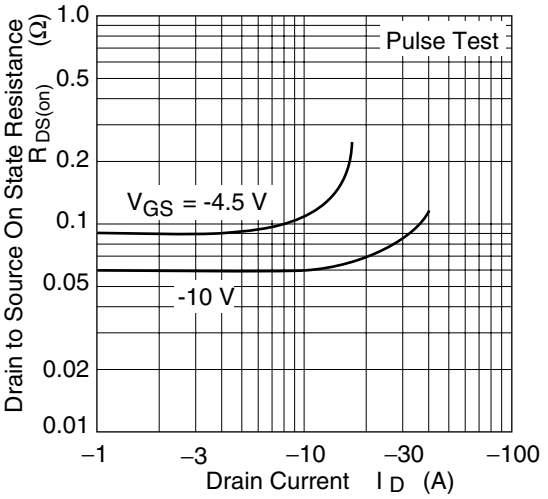
Typical Transfer Characteristics



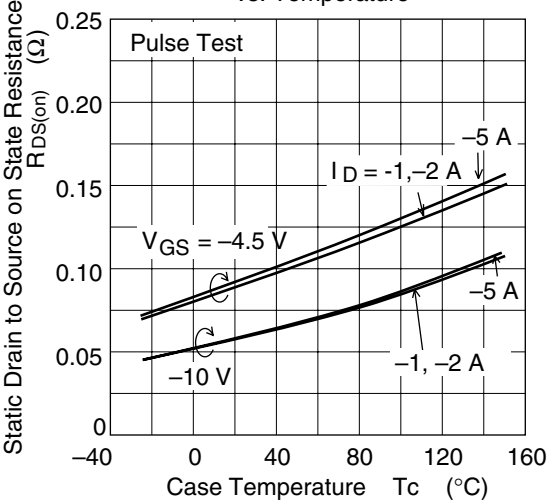
Drain to Source Saturation Voltage vs. Gate to Source Voltage



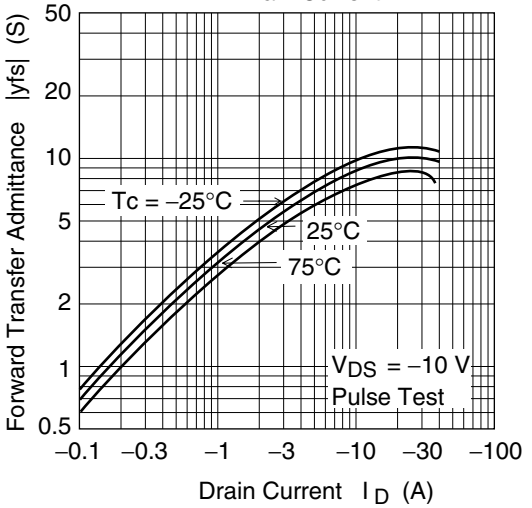
Static Drain to Source on State Resistance vs. Drain Current



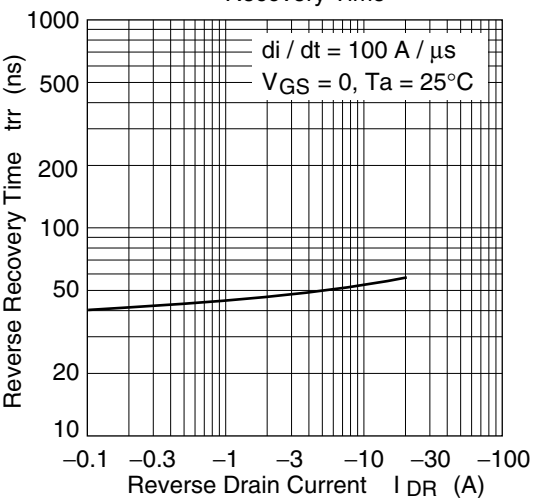
Static Drain to Source on State Resistance vs. Temperature



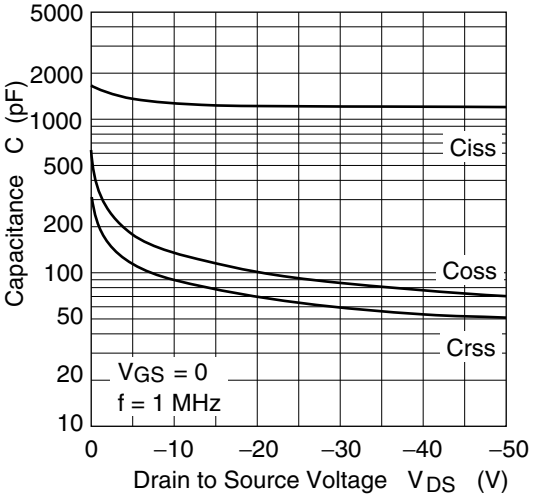
Forward Transfer Admittance vs. Drain Current



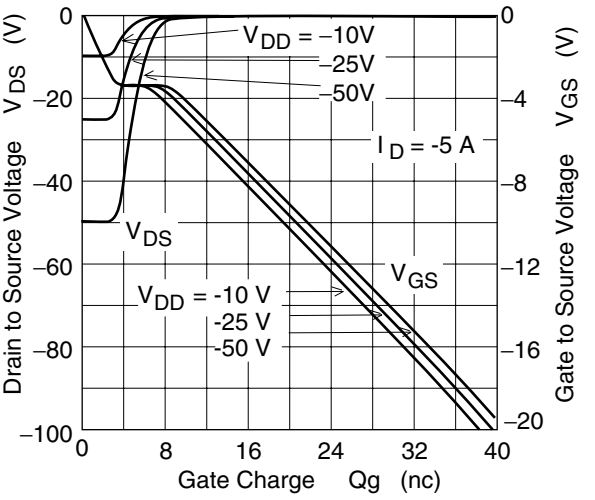
Body-Drain Diode Reverse Recovery Time



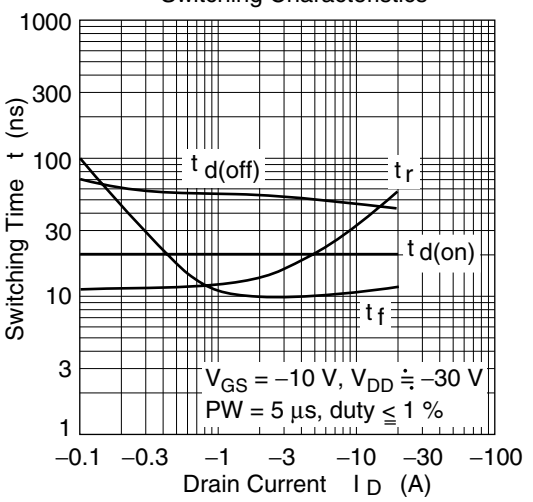
Typical Capacitance vs.
Drain to Source Voltage



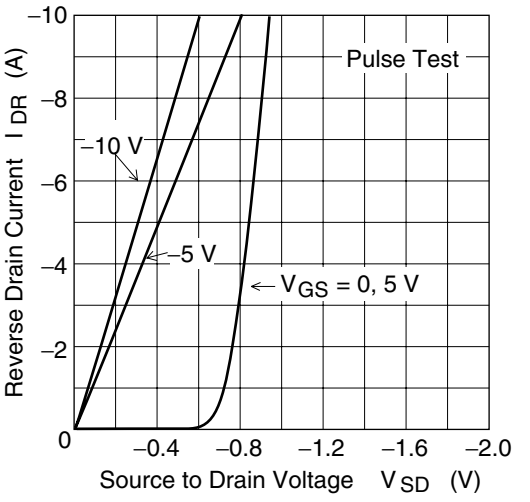
Dynamic Input Characteristics



Switching Characteristics



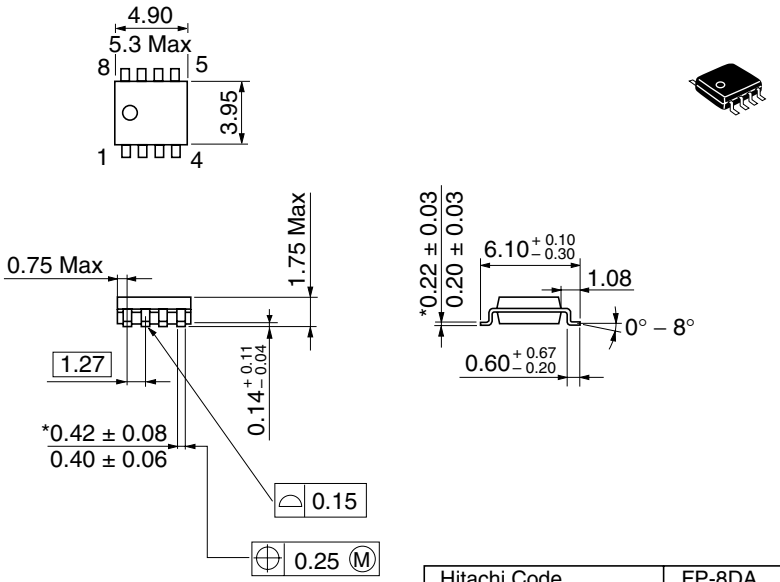
Reverse Drain Current vs.
Souece to Drain Voltage



Package Dimensions

As of July, 2001

Unit: mm



*Dimension including the plating thickness
Base material dimension

Hitachi Code	FP-8DA
JEDEC	Conforms
JEITA	—
Mass (reference value)	0.085 g

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Hitachi, Ltd.
Semiconductor & Integrated Circuits
Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan
Tel: (03) 3270-2111 Fax: (03) 3270-5109

URL http://www.hitachisemiconductor.com/

For further information write to:

Hitachi Semiconductor
(America) Inc.
179 East Tasman Drive
San Jose,CA 95134
Tel: <1> (408) 433-1990
Fax: <1>(408) 433-0223

Hitachi Europe Ltd.
Electronic Components Group
Whitebrook Park
Lower Cookham Road
Maidenhead
Berkshire SL6 8YA, United Kingdom
Tel: <44> (1628) 585000
Fax: <44> (1628) 585200

Hitachi Europe GmbH
Electronic Components Group
Dornacher Straße 3
D-85622 Feldkirchen
Postfach 201, D-85619 Feldkirchen
Germany
Tel: <49> (89) 9 9180-0
Fax: <49> (89) 9 29 30 00

Hitachi Asia Ltd.
Hitachi Tower
16 Collyer Quay #20-00
Singapore 049318
Tel : <65>-538-6533/538-8577
Fax : <65>-538-6933/538-3877
URL : http://semiconductor.hitachi.com.sg

Hitachi Asia Ltd.
(Taipei Branch Office)
4/F, No. 167, Tun Hwa North Road
Hung-Kuo Building
Taipei (105), Taiwan
Tel : <886>-(2)-2718-3666
Fax : <886>-(2)-2718-8180
Telex : 23222 HAS-TP
URL : http://www.hitachi.com.tw

Hitachi Asia (Hong Kong) Ltd.
Group III (Electronic Components)
7/F., North Tower
World Finance Centre,
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Tsim Sha Tsui, Kowloon Hong Kong
Tel : <852>-(2)-735-9218
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