October 2000 File Number 4147.3

3 REN Ringing SLIC For ISDN Modem/TA and WLL

The HC5517 is a ringing SLIC designed to accommodate a wide variety of local loop applications. The various applications include, basic POTS lines with answering machines and fax capabilities, ISDN networks, wireless local loop, and hybrid fiber coax (HFC) terminals. The HC5517 provides a high degree of flexibility with open circuit tip to ring DC voltages, user defined ringing waveforms (sinusoidal to square wave), ring trip detection thresholds and loop current limits that can be tailored for many applications. Additional features of the HC5517 are complex impedance matching, pulse metering and transhybrid balance. The HC5517 is designed for use in systems where a separate ring generator is not economically feasible.

The device is manufactured in a high voltage Dielectric Isolation (DI) process with an operating voltage range from -16V, for off-hook operation and -80V for ring signal injection. The DI process provides substrate latch up immunity, resulting in a robust system design. Together with a secondary protection diode bridge and “feed” resistors, the device will withstand 1000V lightning induced surges, in a plastic package.

A thermal shutdown with an alarm output and line fault protection are also included for operation in harsh environments.

Part Number Information

PART NUMBER	TEMP. RANGE (^oC)	PACKAGE	PKG. NO.
HC5517IM	-40 to 85	28 Ld PLCC	N28.45
HC5517CM	0 to 75	28 Ld PLCC	N28.45
HC5517IB	-40 to 85	28 SOIC	M28.3
HC5517CB	0 to 75	28 SOIC	M28.3

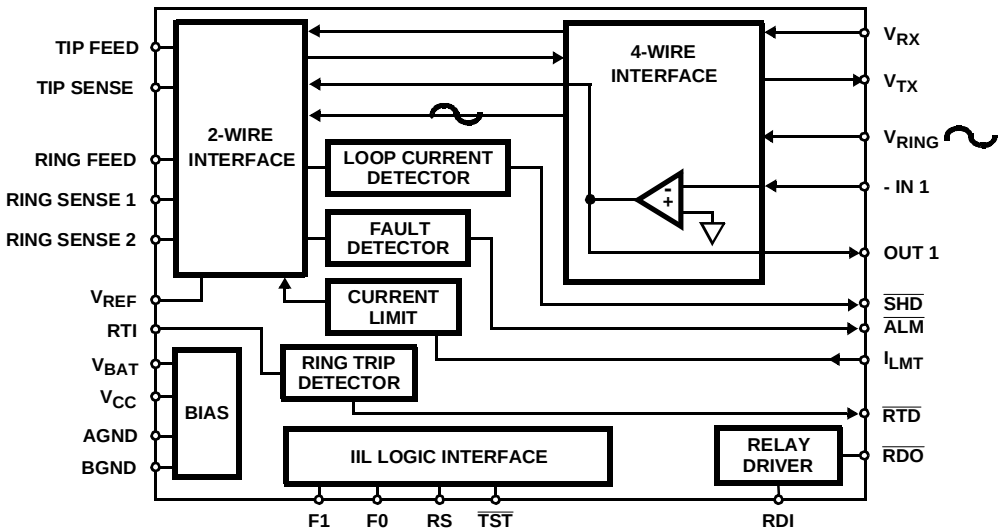
Features

- Thru-SLIC Open Circuit Ringing Voltage up to $77V_{PEAK}/54V_{RMS}$, 3 REN Capability at $44V_{RMS}$
- Sinusoidal Ringing Capability
- DI Process Provides Substrate Latch Up Immunity when Driving Inductive Ringers
- Adjustable On-Hook Voltage for Fax and Answering Machine Compatibility
- Resistive and Complex Impedance Matching
- Programmable Loop Current Limit
- Switch Hook and Adjustable Ring Trip Detection
- Pulse Metering Capability
- Single Low Voltage Positive Supply (+5V)

Applications

- Solid State Line Interface Circuit for Wireless Local Loop, Hybrid Fiber Coax, Set Top Box, Voice/Data Modems
- Related Literature
  - AN9606, Operation of the HC5517 Evaluation Board
  - AN9607, Impedance Matching Design Equations
  - AN9628, AC Voltage Gain
  - AN9608, Implementing Pulse Metering
  - AN9636, Implementing an Analog Port for ISDN Using the HC5517
  - AN549, The HC-5502S/4X Telephone Subscriber Line Interface Circuits (SLIC)

Block Diagram



Absolute Maximum Ratings $T_A = 25^oC$

Maximum Supply Voltages
- (V_{CC}) . . . . . -0.5V to +7V
- (V_{CC})-(V_{BAT}) 90V

Relay Drivers . . . . . -0.5V to +15V

Operating Conditions

Operating Temperature Range
- HC5517IM, HC5517IB . . . . . -40^oC to 85^oC
- HC5517CM, HC5517CB . . . . . 0^oC to 75^oC

Relay Drivers . . . . . +5V to +12V
Positive Power Supply (V_{CC}) . . . . . +5V ±5%
Negative Power Supply (V_{BAT}) . . . . . -16V to -80V

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} ($^oC/W$)
PLCC	55
SOIC	70

Maximum Junction Temperature Plastic . . . . . 150^oC
Maximum Storage Temperature Range . . . . . -65^oC to 150^oC
Maximum Lead Temperature (Soldering 10s) . . . . . 300^oC
(SOIC, PLCC - Lead Tips Only)

Die Characteristics

Transistor Count 224
Diode Count 28
Die Dimensions . . . . . 174 x 120
Substrate Potential . . . . . V_{BAT}
Process . . . . . Bipolar-DI
ESD (Human Body Model) 500V

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.
2. All grounds (AGND, BGND) must be applied before V_{CC} or V_{BAT}. Failure to do so may result in premature failure of the part. If a user wishes to run separate grounds off a line card, the AG must be applied first.

Electrical Specifications

Unless Otherwise Specified, Typical Parameters are at $T_A = 25^oC$, Min-Max Parameters are over Operating Temperature Range, V_{BAT} = -24V, V_{CC} = +5V, AGND = BGND = 0V. All AC Parameters are specified at 600Ω 2-Wire terminating impedance.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
RINGING TRANSMISSION PARAMETERS					
V_{RING} Input Impedance	(Note 3)	-	5.4	-	kΩ
4-Wire to 2-Wire Gain	V_{RING} to Vt-r (Note 3)	-	40	-	V/V
AC TRANSMISSION PARAMETERS					
RX Input Impedance	300Hz to 3.4kHz (Note 3)	-	108	-	kΩ
TX Output Impedance	300Hz to 3.4kHz (Note 3)	-	-	20	Ω
4-Wire Input Overload Level	300Hz to 3.4kHz R_L = 1200Ω, 600Ω Reference (Note 3)	+1.0	-	-	V_{PEAK}
2-Wire Return Loss	Matched for 600Ω (Note 3)				
SRL LO		26	35	-	dB
ERL		30	40	-	dB
SRL HI		30	40	-	dB
2-Wire Longitudinal to Metallic Balance Off Hook	Per ANSI/IEEE STD 455-1976 (Note 3) 300Hz to 3400Hz	58	63	-	dB
4-Wire Longitudinal Balance Off Hook	300Hz to 3400Hz (Note 3)	50	55	-	dB
Low Frequency Longitudinal Balance	I_{LINE} = 40mA $T_A = 25^oC$ (Note 3)	-	10	23	dBrnC
Longitudinal Current Capability	I_{LINE} = 40mA $T_A = 25^oC$ (Note 3)	-	-	40	mA_{RMS}
Insertion Loss	0dBm at 1kHz, Referenced 600Ω				
2-Wire/4-Wire (Includes external transhybrid amplifier with a gain of 3)		-	±0.05	±0.2	dB
4-Wire/2-Wire		-	±0.05	±0.2	dB
4-Wire/4-Wire (Includes external transhybrid amplifier with a gain of 3)		-	-	±0.25	dB

Electrical Specifications Unless Otherwise Specified, Typical Parameters are at $T_A = 25^oC$, Min-Max Parameters are over Operating Temperature Range, $V_{BAT} = -24V$, $V_{CC} = +5V$, AGND = BGND = 0V. All AC Parameters are specified at 600Ω 2-Wire terminating impedance. **(Continued)**

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Frequency Response	300Hz to 3400Hz (Note 3) Referenced to Absolute Level at 1kHz, 0dBm Referenced 600Ω	-	±0.02	±0.06	dB
Level Linearity	Referenced to -10dBm (Note 3)				
2-Wire to 4-Wire and 4-Wire to 2-Wire	+3 to -40dBm	-	-	±0.08	dB
	-40 to -50dBm	-	-	±0.12	dB
	-50 to -55dBm	-	-	±0.3	dB
Absolute Delay	(Note 3)				
2-Wire/4-Wire	300Hz to 3400Hz	-	-	1.0	µs
4-Wire/2-Wire	300Hz to 3400Hz	-	-	1.0	µs
4-Wire/4-Wire	300Hz to 3400Hz	-	0.95	1.5	µs
Transhybrid Loss	$V_{IN} = 1V_{P-P}$ at 1kH (Notes 3, 4)	30	40		dB
Total Harmonic Distortion 2-Wire/4-Wire, 4-Wire/2-Wire, 4-Wire/4-Wire	Reference Level 0dBm at 600Ω 300Hz to 3400Hz (Note 3)	-	-	-50	dB
Idle Channel Noise 2-Wire and 4-Wire	(Note 3) C-Message	-	3	-	dBrnC
	Psophometric (Note 3)	-	-87	-	dBmp
Power Supply Rejection Ratio	(Note 3)				
V_{CC} to 2-Wire	30Hz to 200Hz, $R_L = 600Ω$	20	40	-	dB
V_{CC} to 4-Wire		20	40	-	dB
V_{BAT} to 2-Wire		20	40	-	dB
V_{BAT} to 4-Wire		20	50	-	dB
V_{CC} to 2-Wire	(Note 3)	30	40	-	dB
V_{CC} to 4-Wire	200Hz to 16kHz, $R_L = 600Ω$	20	28	-	dB
V_{BAT} to 2-Wire		20	50	-	dB
V_{BAT} to 4-Wire		20	50	-	dB
DC PARAMETERS					
Loop Current Programming					
Limit Range		20 (Note 5)	-	60	mA
Accuracy		10	-	-	%
Loop Current During Power Denial	$R_L = 200Ω$	-	±4	±7	mA
Fault Currents					
TIP to Ground (Note 3)		-	30	-	mA
RING to Ground		-	120	-	mA
TIP and RING to Ground (Note 3)		-	150	-	mA
Switch Hook Detection Threshold		-	12	15	mA
Ring Trip Comparator Voltage Threshold		-0.28	-0.24	-0.22	V
Thermal $\overline{ALARM}$ Output (Note 3)	Safe Operating Die Temperature Exceeded	140	-	160	^oC

Electrical Specifications Unless Otherwise Specified, Typical Parameters are at $T_A = 25^oC$, Min-Max Parameters are over Operating Temperature Range, $V_{BAT} = -24V$, $V_{CC} = +5V$, AGND = BGND = 0V. All AC Parameters are specified at 600Ω 2-Wire terminating impedance. **(Continued)**

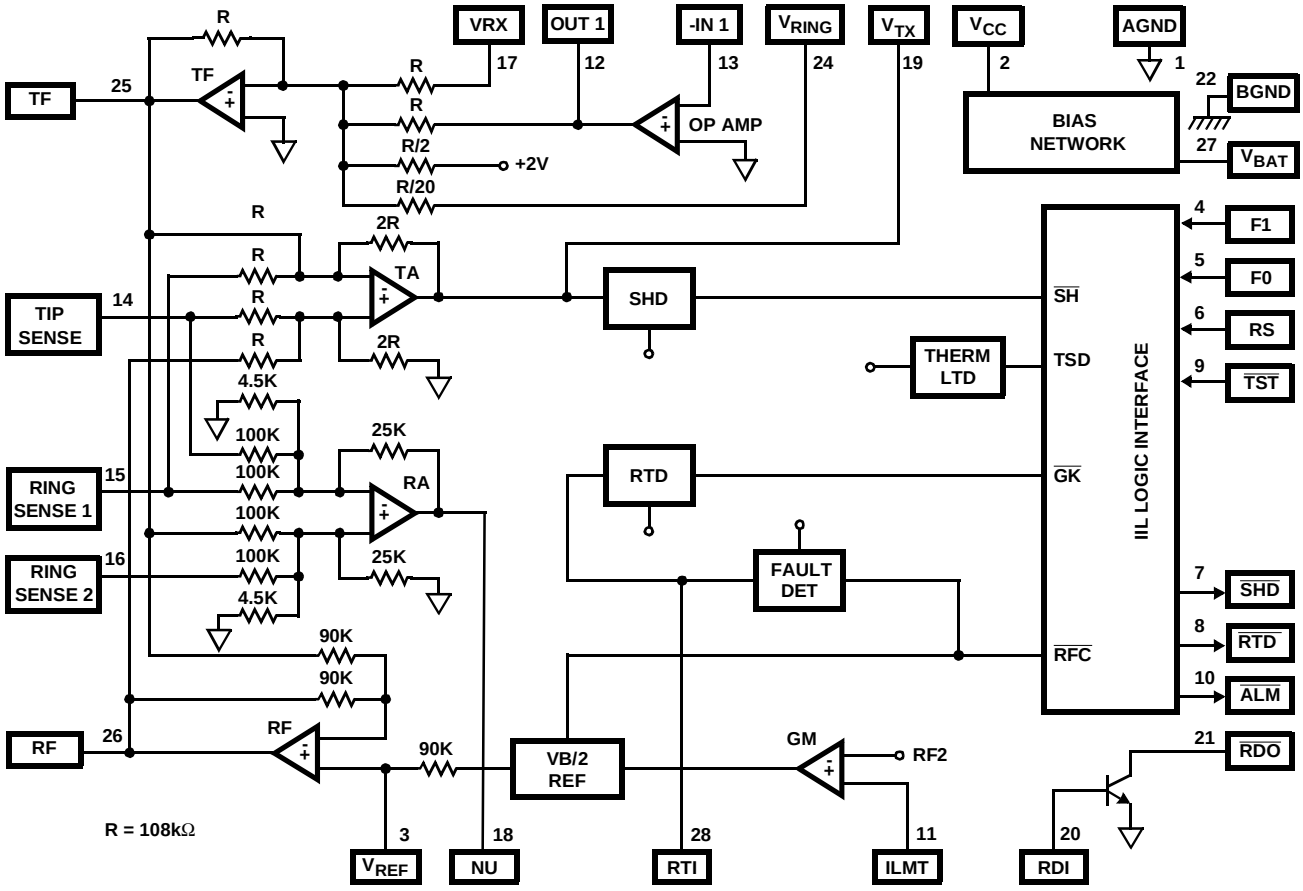
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Dial Pulse Distortion (Note 3)		-	0.1	0.5	ms
Uncommitted Relay Driver					
On Voltage V_{OL}	I_{OL} ($\overline{RDO}$) = 30mA	-	0.2	0.5	V
Off Leakage Current		-	±10	±100	µA
TTL/CMOS Logic Inputs (F0, F1, RS, $\overline{TST}$, RDI)					
Logic '0' V_{IL}		0	-	0.8	V
Logic '1' V_{IH}		2.0	-	5.5	V
Input Current (F0, F1, RS, $\overline{TST}$, RDI)	IIH, $0V \le V_{IN} \le 5V$	-	-	-1	µA
Input Current (F0, F1, RS, $\overline{TST}$, RDI)	IIL, $0V \le V_{IN} \le 5V$	-	-	-100	µA
Logic Outputs					
Logic '0' V_{OL}	I_{LOAD} = 800µA	-	0.1	0.5	V
Logic '1' V_{OH}	I_{LOAD} = 40µA	2.7	-	-	V
Power Dissipation On Hook	V_{CC} = +5V, V_{BAT} = -80V, $R_{LOOP} = \infty$	-	300	-	mW
	V_{CC} = +5V, V_{BAT} = -48V, $R_{LOOP} = \infty$	-	150	-	mW
Power Dissipation Off Hook	V_{CC} = +5V, V_{BAT} = -24V, R_{LOOP} = 600Ω, I_L = 25mA	-	280	-	mW
I_{CC}	V_{CC} = +5V, V_{BAT} = -80V, $R_{LOOP} = \infty$	-	3	6	mA
	V_{CC} = +5V, V_{BAT} = -48V, $R_{LOOP} = \infty$	-	2	5	mA
	V_{CC} = +5V, V_{BAT} = -24V, $R_{LOOP} = \infty$	-	1.9	4	mA
I_{BAT}	V_{CC} = +5V, V_{B-} = -80V, $R_{LOOP} = \infty$	-	3.6	7	mA
	V_{CC} = +5V, V_{B-} = -48V, $R_{LOOP} = \infty$	-	2.6	6	mA
	V_{CC} = +5V, V_{B-} = -24V, $R_{LOOP} = \infty$	-	1.8	4	mA
UNCOMMITTED OP AMP PARAMETERS					
Input Offset Voltage		-	±5	-	mV
Input Offset Current		-	±10	-	nA
Differential Input Resistance (Note 3)		-	1	-	MΩ
Output Voltage Swing (Note 3)	R_L = 10kΩ	-	±3	-	V_{P-P}
Small Signal GBW (Note 3)		-	1	-	MHz

NOTES:

3. These parameters are controlled by design or process parameters and are not directly tested. These parameters are characterized upon initial design release, upon design changes which would affect these characteristics, and at intervals to assure product quality and specification compliance.
4. For transhybrid circuit as shown in Figure 10.
5. Application limitation based on maximum switch hook detect limit and metallic currents. Not a part limitation.

Functional Diagram

PLCC/SOIC



HC5517 TRUTH TABLE

F1	F0	ACTION
0	0	Loop power Denial Active
0	1	Power Down Latch RESET
0	1	Power on RESET
1	0	$\overline{RD}$ Active
1	1	Normal Loop feed

Over Voltage Protection and Longitudinal Current Protection

The SLIC device, in conjunction with an external protection bridge, will withstand high voltage lightning surges and power line crosses.

High voltage surge conditions are as specified in Table 1.

The SLIC will withstand longitudinal currents up to a maximum or $30mA_{RMS}$, $15mA_{RMS}$ per leg, without any performance degradation

TABLE 1.

PARAMETER	TEST CONDITION	PERFORMANCE (MAX)	UNITS
Longitudinal Surge	10µs Rise/ 1000µs Fall	±1000 (Plastic)	V_{PEAK}
Metallic Surge	10µs Rise/ 1000µs Fall	±1000 (Plastic)	V_{PEAK}
T/GND R/GND	10µs Rise/ 1000µs Fall	±1000 (Plastic)	V_{PEAK}
50/60Hz Current T/GND R/GND	 11 Cycles Limited to $10A_{RMS}$	700 (Plastic)	V_{RMS}

Circuit Operation and Design Information

The HC5517 is a voltage feed current sense **S**ubscriber **L**ine **I**nterface **C**ircuit (SLIC). This means that for long loop applications the SLIC provides a constant voltage to the tip and ring terminals while sensing the tip to ring current. For short loops, where the loop current limit is exceeded, the tip to ring voltage decreases as a function of loop resistance.

The following discussion separates the SLIC's operation into its DC and AC path, then follows up with additional circuit design and application information.

DC Operation of Tip and Ring Amplifiers

SLIC in the Active Mode

The tip and ring amplifiers are voltage feedback op amps that are connected to generate a differential output (e.g. if tip sources 20mA then ring sinks 20mA). Figure 1 shows the connection of the tip and ring amplifiers. The tip DC voltage is set by an internal +2V reference, resulting in -4V at the output. The ring DC voltage is set by the tip DC output voltage and an internal $V_{BAT}/2$ reference, resulting in V_{BAT} +4V at the output. (See Equation 1, Equation 2 and Equation 3.)

$$V_{TIPFEED} = V_C = -2V\left(\frac{R}{R/2}\right) = -4V \quad \text{(EQ. 1)}$$

$$V_{RINGFEED} = V_D = \frac{V_{BAT}}{2}\left(1+\frac{R}{R}\right) - V_{TIPFEED}\left(\frac{R}{R}\right) \quad \text{(EQ. 2)}$$

$$V_{RINGFEED} = V_D = V_{BAT} + 4 \quad \text{(EQ. 3)}$$

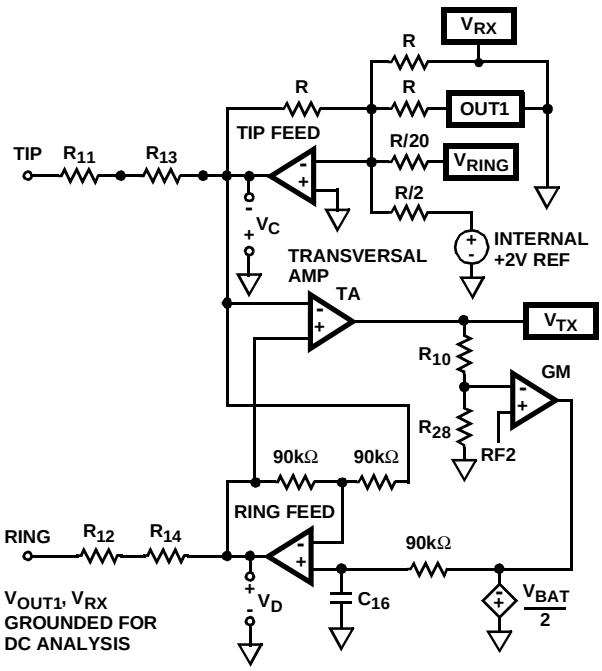


FIGURE 1. OPERATION OF THE TIP AND RING AMPLIFIERS

Current Limit

The tip feed to ring feed voltage (Equation 1 minus Equation 3) is equal to the battery voltage minus 8V. Thus, with a 48 (24) volt battery and a 600Ω loop resistance, including the feed resistors, the loop current is 66.6mA (26.6mA). On short loops the line resistance often approaches zero and the need exists to control the maximum DC loop current.

Current limiting is achieved by a feedback network (Figure 1) that modifies the ring feed voltage (V_D) as a function of the loop current. The output of the Transversal Amplifier (TA) has a DC voltage that is directly proportional to the loop current. This voltage is scaled by R_{10} and R_{28}. The scaled voltage is the input to a transconductance amplifier (GM) that compares it to an internal reference level. When the scaled voltage exceeds the internal reference level, the transconductance amplifier sources current. This current charges C_{16} in the positive direction causing the ring feed voltage (V_D) to approach the tip feed voltage (V_C). This effectively reduces the tip feed to ring feed voltage (V_{T-R}), and holds the maximum loop current constant.

The maximum loop current is programed by resistors R_{10} and R_{28} as shown in Equation 4 (Note: R_{10} is typically 100kΩ).

$$I_{LIMIT} = \frac{(0.6)(R_{10}+R_{28})}{(200xR_{28})} \quad \text{(EQ. 4)}$$

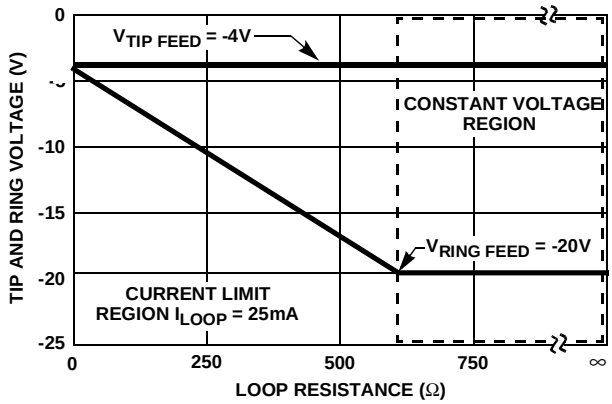


FIGURE 2. V_{T-R} vs R_L (V_{BAT} = -24V, I_{LIMIT} = 25mA)

Figure 2 illustrates the relationship between V_{T-R} and the loop resistance. The conditions are shown for a battery voltage of -24V and the loop current limit set to 25mA. For a infinite loop resistance both tip feed and ring feed are at -4V and -20V respectively. When the loop resistance decreases from infinity to about 640Ω the loop current (obeying Ohm's Law) increases from 0mA to the set loop current limit. As the loop resistance continues to decrease, the ring feed voltage approaches the tip feed voltage as a function of the programed loop current limit (Equation 4).

AC Voltage Gain Design Equations

The HC5517 uses feedback to synthesize the impedance at the 2-wire tip and ring terminals. This feedback network defines the AC voltage gains for the SLIC.

The 4-wire to 2-wire voltage gain (V_{RX} to V_{TR}) is set by the feedback loop shown in Figure 3. The feedback loop senses the loop current through resistors R_{13} and R_{14}, sums their voltage drop and multiplies it by 2 to produce an output voltage at the V_{TX} pin equal to $+4R_S\Delta I_L$. The V_{TX} voltage is then fed into the -IN1 input of the SLIC's internal op amp. This signal is multiplied by the ratio R_8/R_9 and fed into the tip current summing node via the OUT1 pin. (Note: the internal $V_{BAT}/2$ reference (ring feed amplifier) and the internal +2V reference (tip feed amplifier) are grounded for the AC analysis.)

The current into the OUT1 pin is equal to:

$$I_{OUT1} = -\frac{4R_S\Delta I_L}{R}\left(\frac{R_8}{R_9}\right) \quad \text{(EQ. 5)}$$

Equation 6 is the node equation for the tip amplifier summing node. The current in the tip feedback resistor (I_R) is given in Equation 7.

$$-I_R - \frac{4R_S\Delta I_L}{R}\left(\frac{R_8}{R_9}\right) + \frac{V_{RX}}{R} = 0 \quad \text{(EQ. 6)}$$

$$I_R = -\frac{4R_S\Delta I_L}{R}\left(\frac{R_8}{R_9}\right) + \frac{V_{RX}}{R} \quad \text{(EQ. 7)}$$

The AC voltage at V_C is then equal to:

$$V_C = (I_R)(R) \quad \text{(EQ. 8)}$$

$$V_C = -4R_S\Delta I_L\left(\frac{R_8}{R_9}\right) + V_{RX} \quad \text{(EQ. 9)}$$

and the AC voltage at V_D is:

$$V_D = 4R_S\Delta I_L\left(\frac{R_8}{R_9}\right) - V_{RX} \quad \text{(EQ. 10)}$$

The values for R_8 and R_9 are selected to match the impedance requirements on tip and ring, for more information reference AN9607 “Impedance Matching Design Equations for the HC5509 Series of SLICs”. The following loop current calculations will assume the proper R_8 and R_9 values for matching a 600Ω load.

The loop current (ΔI_L) with respect to the feedback network, is calculated in Equations 11 through 14. Where R_8 = 40kΩ, R_9 = 40kΩ, R_L = 600Ω, $R_{11} = R_{12} = R_{13} = R_{14}$ = 50Ω.

$$\Delta I_L = \frac{V_C - V_D}{R_L + R_{11} + R_{12} + R_{13} + R_{14}} \quad \text{(EQ. 11)}$$

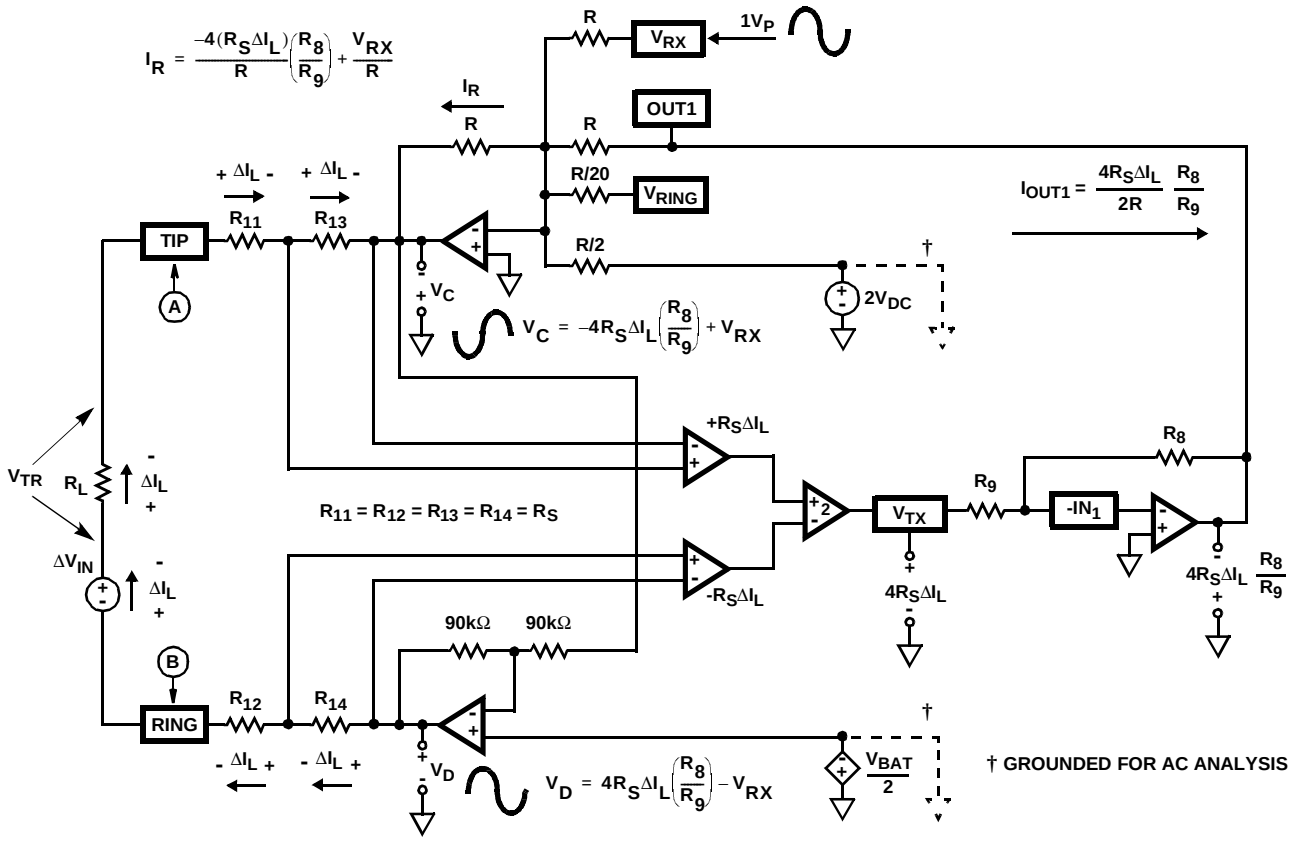


FIGURE 3. AC VOLTAGE GAIN AND IMPEDANCE MATCHING

Substituting the expressions for V_C and V_D:

$$\Delta I_L = \frac{2 \times \left(-4R_S\Delta I_L\left(\frac{R_8}{R_9}\right) + V_{RX}\right)}{R_L + R_{11} + R_{12} + R_{13} + R_{14}} \quad \text{(EQ. 12)}$$

Equation 12 simplifies to:

$$\Delta I_L = \frac{2V_{RX} - 400\Delta I_L}{800} \quad \text{(EQ. 13)}$$

Solving for ΔI_L results in:

$$\Delta I_L = \frac{V_{RX}}{600} \quad \text{(EQ. 14)}$$

Equation 14 is the loop current with respect to the feedback network. From this, the 4-wire to 2-wire and the 2-wire to 4-wire AC voltage gains are calculated. Equation 15 shows the 4-wire to 2-wire AC voltage gain is equal to one.

$$A_{4W-2W} = \frac{V_{TR}}{V_{RX}} = \frac{\Delta I_L(R_L)}{V_{RX}} = \frac{\frac{V_{RX}}{600}(600)}{V_{RX}} = 1 \quad \text{(EQ. 15)}$$

Equation 16 shows the 2-wire to 4-wire AC voltage gain is equal to negative one-third.

$$A_{2W-4W} = \frac{V_{OUT1}}{V_{TR}} = \frac{-4R_S\Delta I_L\left(\frac{R_8}{R_9}\right)}{\Delta I_L(R_L)} = \frac{-200\frac{V_{RX}}{600}(1)}{\frac{V_{RX}}{600}(600)} = -\frac{1}{3} \quad \text{(EQ. 16)}$$

Impedance Matching

The feedback network, described above, is capable of synthesizing both resistive and complex loads. Matching the SLIC's 2-wire impedance to the load is important to maximize power transfer and minimize the 2-wire return loss. The 2-wire return loss is a measure of the similarity of the impedance of a transmission line (tip and ring) and the impedance at it's termination. It is a ratio, expressed in decibels, of the power of the outgoing signal to the power of the signal reflected back from an impedance discontinuity.

Requirements for Impedance Matching

Impedance matching of the HC5517 application circuit to the transmission line requires that the impedance be matched to points "A" and "B" in Figure 3. To do this, the sense resistors R_{11}, R_{12}, R_{13} and R_{14} must be accounted for by the feedback network to make it appear as if the output of the tip and ring amplifiers are at points "A" and "B". The feedback network takes a voltage that is equal to the voltage drop across the sense resistors and feeds it into the summing node of the tip amplifier. The effect of this is to cause the tip feed voltage to become more negative by a value that is proportional to the voltage drop across the sense resistors R_{11} and R_{13}. At the same time the ring amplifier becomes more positive by the same amount to account for resistors R_{12} and R_{14}.

The net effect cancels out the voltage drop across the feed resistors. By nullifying the effects of the feed resistors the feedback circuitry becomes relatively easy to match the impedance at points "A" and "B".

IMPEDANCE MATCHING DESIGN EQUATIONS

Matching the impedance of the SLIC to the load is accomplished by writing a loop equation starting at V_D and going around the loop to V_C. The loop equation to match the impedance of any load is as follows (Note: V_{RX} = 0 for this analysis):

$$-4R_S\Delta I_L\left(\frac{R_8}{R_9}\right) + 2R_S\Delta I_L - \Delta V_{IN} +$$

$$R_L\Delta I_L + 2R_S\Delta I_L - 4R_S\Delta I_L\left(\frac{R_8}{R_9}\right) = 0 \quad \text{(EQ. 17)}$$

$$\Delta V_{IN} = -8R_S\Delta I_L\left(\frac{R_8}{R_9}\right) + 4R_S\Delta I_L + R_L\Delta I_L \quad \text{(EQ. 18)}$$

$$\Delta V_{IN} = \Delta I_L\left[-8R_S\left(\frac{R_8}{R_9}\right) + 4R_S + R_L\right] \quad \text{(EQ. 19)}$$

Equation 19 can be separated into two terms, the feedback ($-8R_S(R_8/R_9)$) and the loop impedance ($+4R_S+R_L$).

$$\frac{\Delta V_{IN}}{\Delta I_L} = -8R_S\left(\frac{R_8}{R_9}\right) + 4R_S + R_L \quad \text{(EQ. 20)}$$

The result is shown in Equation 20. Figure 4 is a schematic representation of Equation 15.

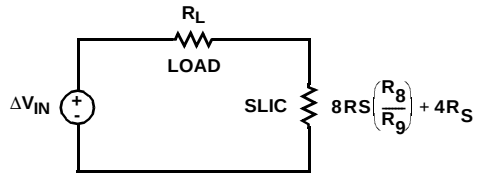


FIGURE 4. SCHEMATIC REPRESENTATION OF EQUATION 20

To match the impedance of the SLIC to the impedance of the load, set:

$$R_L = 8R_S\left(\frac{R_8}{R_9}\right) + 4R_S \quad \text{(EQ. 21)}$$

If R_9 is made to equal $8R_S$ then:

$$R_L = R_8 + 4R_S \quad \text{(EQ. 22)}$$

Therefore to match the HC5517, with R_S equal to 50Ω, to a 600Ω load:

$$R_9 = 8R_S = 8(50\Omega) = 400\Omega \quad \text{(EQ. 23)}$$

and:

$$R_8 = R_L - 4R_S = 600\Omega - 200\Omega = 400\Omega \quad \text{(EQ. 24)}$$

To prevent loading of the V_{TX} output, the value of R_8 and R_9 are typically scaled by a factor of 100:

$$KR_8 = 40k\Omega \qquad KR_9 = 40k\Omega \tag{EQ. 25}$$

Since the impedance matching is a function of the voltage gain, scaling of the resistors to achieve a standard value is recommended.

For complex impedances the above analysis is the same.

$$KR_9 = 40k\Omega \qquad KR_8 = 100(Resistive - 200) + \frac{Reactive}{100} \tag{EQ. 26}$$

Reference application note AN9607 (“Impedance Matching Design Equations for the HC5509 Series of SLICs”) for the values of KR_9 and KR_8 for several worldwide Typical line impedances.

Tip-to-Ring Open-Circuit Voltage

The tip-to-ring open-circuit voltage, V_{OC}, of the HC5517 is programmable to meet a variety of applications. The design of the HC5517 defaults the value of V_{OC} to:

$$V_{OC} \cong |V_{BAT}| - 8$$

The HC5517 application circuit overrides the default V_{OC} operation when operating from a -80V battery. While operating from a -80V battery, the SLIC will be in either the ringing mode or on-hook standby mode. In the ringing mode, V_{OC} is designed to switch from 0V (centering voltage) to -47V (Maintenance Termination Unit voltage). The centering voltage is active during the ringing portion of the ringing waveform and the Maintenance Termination Unit (MTU) voltage is active during the silent portion of the ringing signal. In the on-hook standby mode, the application circuit is designed to maintain V_{OC} at the MTU voltage.

Centering Voltage Application Circuit Overview

The centering voltage is used during ringing to center the DC outputs of the tip feed and ring feed amplifiers. Centering the amplifier outputs allows for the maximum undistorted voltage swing of the ringing signal. Without centering, the output of each amplifier would saturate at ground or V_{BAT}, minimizing the ringing capability of the HC5517. The required centering voltage, V_C, is $+1.8V_{DC}$ when operating from a -80V battery.

Centering Voltage Application Circuit Operation

The circuit used to generate the centering voltage is shown in Figure 5.

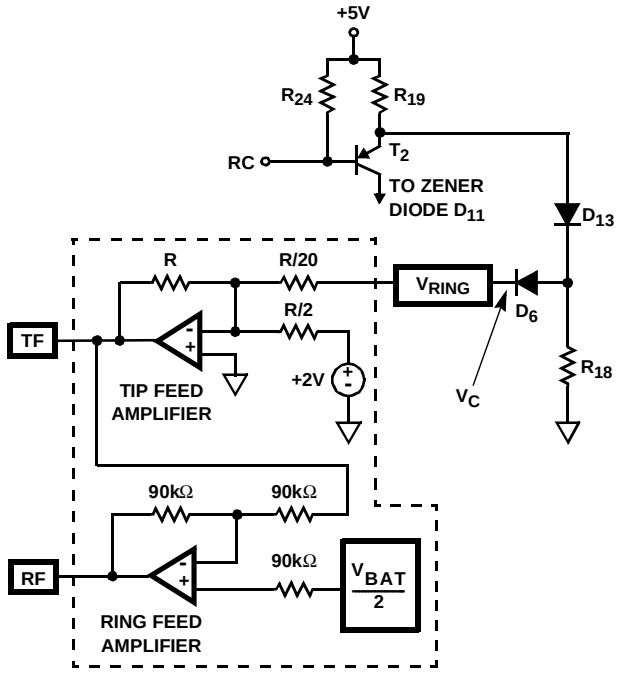


FIGURE 5. CENTERING VOLTAGE APPLICATION CIRCUIT

The circuitry within the dotted lines is internal to the HC5517. The value of the resistor designated as R is 108kΩ and the resistor R/20 is 5.4kΩ. The tip amplifier gain of 20V/V amplifies the $+1.8V_{DC}$ at V_C to $+36V_{DC}$ and adds it to the internal $4V_{DC}$ offset, generating $-40V_{DC}$ at the tip amplifier output. The $-40V_{DC}$ offset also sums into the ring amplifier, adding to the battery voltage, achieving -40V at the ring amplifier output.

Centering Voltage Design Equations

The centering voltage (V_C) is dependent on the battery voltage. A battery voltage of -80V requires a $+1.8V_{DC}$ centering voltage. The equation used to calculate the centering voltage is shown below.

$$V_C = \left(\left|\frac{V_{BAT}}{2}\right| - 4\right)/20 \tag{EQ. 27}$$

The DC voltage at the outputs of the centered tip and ring amplifiers can be calculated from Equation 28 and Equation 29.

$$V_{TC} = -(20V_C + 4) \tag{EQ. 28}$$

$$V_{RC} = V_{BAT} + (20V_C + 4) \tag{EQ. 29}$$

The shunt resistor of the divider network, R_{18}, is not determined from a design equation. It is selected based on the trade-off of power dissipation in the voltage divider (low value of R_{18}) and loading affects of the internal R/20 resistor (high value of R_{18}). The suggested range of R_{18} is between 1.0kΩ and 2.0kΩ. The application circuit design equation used to calculate the value of R_{19} of the divider network is as follows:

$$R_{19} = \frac{(V_{CC} - V_{D13} - V_{D6} - V_C)(R_{18} \bullet R_{IN})}{(V_C + V_{D6})R_{IN} + V_C R_{18}} \quad \text{(EQ. 30)}$$

where: V_{D13} forward drop of D_{13}, 0.63V.

V_{D6} forward drop of D_6, 0.54V.

R_{18} is the shunt resistor of the divider, 1.1kΩ.

R_{IN} is the input impedance of V_{RING}, 5.4kΩ.

V_C is the required centering voltage, 1.8V, V_{BAT} = -80V.

V_{CC} is the +5V supply.

Centering Voltage Logic Control

The pnp transistor T_2 is used to defeat the voltage divider formed by R_{19}, R_{18}, D_{13} and D_6. When T_2 is off (RC is logic high), +5V_{DC} is divided to produce +1.8V_{DC} at the V_{RING} input. When T_2 is on (RC is logic low), its emitter base voltage of +0.9V_{DC} is divided resulting in +0.2V at the anode of D_6, hence reverse biasing the diode (D_6) and floating the V_{RING} pin.

MTU Voltage Application Circuit Overview

According to Bellcore specification TR-NWT-000057, an MTU voltage may be required by some operating companies. The minimum allowable voltage to meet MTU requirements is -42.75V, which is used by measurement equipment to verify an active line. Also, some facsimile and answering machines use the MTU voltage as an indication that the telephone is on-hook or not answered. In addition to the Bellcore specification, FCC Part 68.306 requires that the maximum tip to ground or ring to ground voltage not exceed -56.5V for hazardous voltage limitations. These two requirements have been combined and the resulting range is defined as the MTU voltage. The HC5517 application circuit can be programmed to any voltage within this range using the zener clamping circuit.

MTU Voltage Application Circuit Operation

The circuit used to generate the MTU voltage is shown in Figure 6.

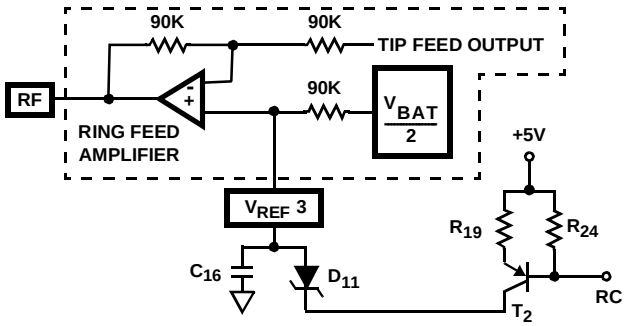


FIGURE 6. RING FEED AMPLIFIER CIRCUIT CONNECTIONS

The ring feed amplifier DC output voltage, V_{RDC}, is a function of the internal $V_{BAT}/2$ reference and external zener diode D_{11}. When the magnitude of $V_{BAT}/2$ is less than the zener voltage, the zener is off and the input to the ring feed amplifier is $V_{BAT}/2$. When the magnitude of $V_{BAT}/2$ is greater than the zener voltage, the zener conducts and clamps the noninverting terminal of the ring amplifier to the zener voltage.

Internal to the HC5517 are connections to the tip feed amplifier output and $V_{BAT}/2$ reference. The DC voltage at the tip feed output, V_{TDC}, is a constant -4V during on-hook standby.

MTU Voltage Design Equations

The following equations are used to predict the DC output of the ring feed amplifier, V_{RDC}.

$$\left|\frac{V_{BAT}}{2}\right| < V_Z \qquad V_{RDC} = 2\left(\frac{V_{BAT}}{2}\right) + 4 \quad \text{(EQ. 31)}$$

$$\left|\frac{V_{BAT}}{2}\right| \geq V_Z \qquad V_{RDC} = 2(-V_Z + (V_{CE} - V_{BE})) + 4 \quad \text{(EQ. 32)}$$

Where V_Z is the zener diode voltage of D_{11} and V_{CE} and V_{BE} are the saturation voltages of T_2. Using Equations 31 and 32, the tip-to-ring open-circuit voltage can be calculated for any value of zener diode and battery voltage.

$$\left|\frac{V_{BAT}}{2}\right| < V_Z \qquad V_{OC} = V_{TDC} - 2\left(\frac{V_{BAT}}{2}\right) - 4 \quad \text{(EQ. 33)}$$

$$\left|\frac{V_{BAT}}{2}\right| \geq V_Z \qquad V_{OC} = V_{TDC} - 2(-V_Z + (V_{CE} - V_{BE})) - 4 \quad \text{(EQ. 34)}$$

Figure 7 plots V_{OC} as a function of battery voltage. The graph illustrates the clamping function of the zener circuitry.

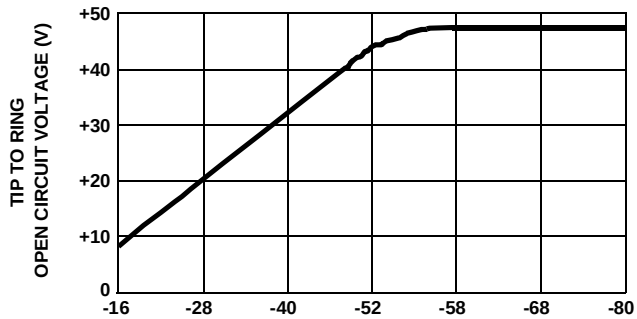


FIGURE 7. V_{OC} AS A FUNCTION OF BATTERY VOLTAGE

MTU Voltage Logic Control

The same pnp transistor, T_2, that is used to control the centering voltage is also used to control the MTU voltage. The application circuit uses T_2 to ground or float the anode of the zener diode D_{11}. When RC is a logic low (T_2 on) the anode of D_{11} is referenced to ground through the collector base junction of the transistor. Current then flows through the zener, allowing the ring amplifier input to be clamped. When RC is a logic high (T_2 off) the anode of D_{11} floats, inhibiting the clamping action of the zener.

HC5517 Modes of Operation

The four modes of operation of the HC5517 Ringing SLIC are ringing, on-hook standby, off-hook active and power denial. Three control signals select the operating mode of the SLIC. The signals are Battery Switch, F1 and Ring Cadence (RC). The active application circuit and active supervisory function are different for each mode, as shown in the Table 2.

Mode Control Signals

The Battery Switch selects between the -80V and -24V supplies. The Battery Switch circuitry is described in the "Operation of the Battery Switch" section. A system alternative to the battery switch signal is to use a buffered version of the $\overline{SHD}$ output to select the battery voltage. Another alternative is to control the output of a programmable battery supply, removing the battery switch entirely from the application circuit. F1 is used to put the SLIC in the power denial mode. RC drives the base of T_2, which is the transistor used to control the centering voltage and MTU voltage. The three control signals can be driven from a TTL logic source or an open collector output.

Ringing Mode

The ringing state, as the name indicates, is used to ring the telephone with a -80V battery supply. The SLIC is designed for balanced ringing with a differential gain of 40V/V across tip and ring. Voltage feed amplifiers operating in the linear mode are used to amplify the ringing signal. The linear amplifier approach allows the system designer to define the shape and amplitude of the ringing waveform. Both supervisory function outputs, $\overline{SHD}$ and $\overline{RTD}$, are active during ringing.

Spectral Content of the Ringing Signal

The shape of the waveform can range from sinusoidal to trapezoidal. Sinusoidal waveforms are spectrally cleaner than trapezoidal waveforms, although the latter does result in lower power dissipation across the SLIC for a given RMS amplitude. Systems where the ringing signal will be in proximity to digital data lines will benefit from the sinusoidal ringing capability of the HC5517. The slow edge rates of a sinusoid will minimize coupling of the large amplitude ringing signal. The linear amplifier architecture of the HC5517 allows the system designer to optimize the design for power dissipation and spectral purity.

Amplitude of the Ringing Signal

Amplitude control is another benefit of the linear amplifier architecture. Systems that require less ringing amplitude are able to do so by driving the HC5517 with a lower level ringing waveform. Solutions that use saturated amplifiers can only vary the amplitude of the ringing signal by changing the negative battery voltage to the SLIC.

HC5517 Through SLIC Ringing

The HC5517 is designed with a high gain input, V_{RING}, that the system drives while ringing the phone. V_{RING} is one of many signals summed at the inverting input to the tip feed amplifier. The gain of the V_{RING} signal through the tip feed amplifier is set to 20V/V. The output of the tip feed amplifier is summed at the inverting input of the ring feed amplifier, configured for unity gain. The result is a differential gain of 40V/V across tip and ring of the ringing signal.

The ringing function requires an input ringing waveform and a centering voltage. The ringing waveform is the signal from the 4-wire side that is amplified by the SLIC to ring the telephone. The centering voltage, as previously discussed, is a positive DC offset that is applied to the V_{RING} input along with the ringing waveform. The HC5517 application circuit provides the centering voltage, simplifying the system interface to an AC coupled ringing waveform.

Ringer Equivalence Number

Before any further discussion, the Ringer Equivalence Number or REN must be discussed. Based on FCC Part 68.313 a single REN can be defined as 5kΩ, 7kΩ or 8kΩ of AC impedance at the ringing frequency. The ringing frequency is based on the ringing types listed in Table 1 of the FCC specification. The impedance of multiple REN is the paralleling of a single REN. Therefore 5 REN can either be 1kΩ, 1.4kΩ or 1.6kΩ. The 7kΩ model of a single REN will be used throughout the remainder of the data sheet.

Ringing Waveform

An amplitude of $1.2V_{RMS}$ will deliver approximately $46V_{RMS}$ to a 1 REN load, and $42V_{RMS}$ to a 3 REN load. The amplitude is REN dependent and is slightly attenuated by the feedback scheme used for impedance matching. The ringing waveform is cadenced, alternating between a 20Hz burst and a silent portion between bursts. Bellcore specification TR-NWT-000057 defines seven distinct ringing waveforms or alerting (ringing) patterns. The following table lists each type.

TABLE 2. DISTINCTIVE ALERTING PATTERNS

	INTERVAL DURATION IN SECONDS					
PATTERN	RINGING	SILENT	RINGING	SILENT	RINGING	SILENT
A	0.4	0.2	0.4	0.2	0.8	4.0
B	0.2	0.1	0.2	0.1	0.6	4.0
C	0.8	0.4	0.8	0.4		
D	0.4	0.2	0.6	4.0		
E	1.2	4.0				
F	1 ± 0.2	3 ± 0.3				
G	0.3	0.2	1.0	0.2	0.3	4.0

Figure 8 shows the relationship of the cadenced ringing waveform and the Battery Switch and RC control signals. Also shown are the states of the MTU voltage and the centering voltage.

The state of Battery Switch is indicated by the desired battery voltage to the SLIC. The RC signal is used to enable and disable the centering voltage and MTU voltage. RC follows the ring signal in that it is high during the 20Hz burst and low during the static part of the waveform.

Open Circuit Voltage During the Ringing Mode

The mutually exclusive relationship of the centering voltage and MTU implies that both functions will not exist at the same time. During the silent portion of the ringing waveform the HC5517 application circuit meets the hazardous voltage requirements of FCC Part 68.306 by forcing the MTU voltage. Without the zener clamping solution, a

programmable power supply would have to be designed. The intervals listed in Table 1 would require the power supply to switch voltages and settle to stable operation well within 100ms. The design of such a power supply may prove quite a challenge. The zener solution provides a cost effective, low impact to meeting a wide variety of tip to ring open circuit voltages.

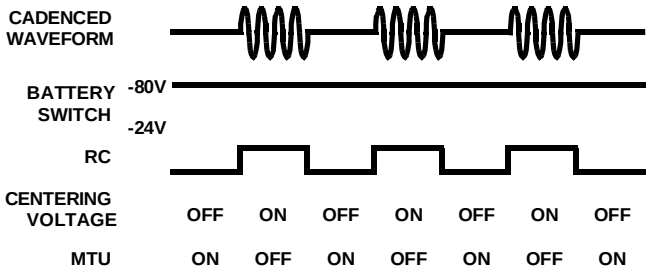


FIGURE 8. RINGING WAVEFORM AND CONTROL SIGNALS

Ringing Design Equations

The differential tip to ring voltage during ringing, as a function of REN, can be approximated from Equation 35.

$$V_{TR}(R_L) \cong 2 \times \left[\frac{V_{RING}}{5.4e3} - \frac{(0.702)(200)V_{TRO}}{(108e3)R_L}\right] \bullet 108e3 \quad \text{(EQ. 35)}$$

The voltage V_{RING} is defined as the RMS amplitude of the input ringing signal. V_{TRO} is the open circuit tip to ring differential output voltage, calculated as V_{RING} multiplied by the differential gain of 40V/V. The REN impedance is shown as R_L. Figure 9 shows the relationship of REN load to maximum differential tip to ring RMS voltage during ringing. The maximum ringing signal amplitude herein assumes an infinite source and sink capability of the tip feed and ring feed amplifiers. Due to the amplifier output design, the HC5517 is limited to 3 REN ringing capability for this reason.

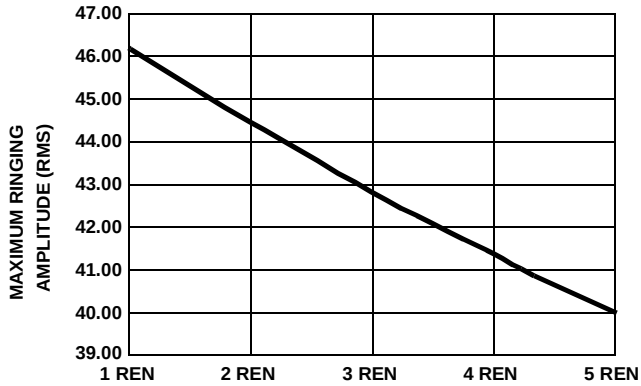


FIGURE 9. MAXIMUM RINGING OUTPUT VOLTAGE ($V_{RING} = 1.2V_{RMS}$)

ON-Hook Standby Mode

On-hook standby mode is with the phone on-hook (i.e., not answered) and ready to accept an incoming voice signal or electronic data. The HC5517 application circuit is designed to maintain the MTU voltage during this mode of operation. During this mode, the $\overline{SHD}$ output is valid and the $\overline{RTD}$ output is invalid.

Off-Hook Active Mode

Off-hook active accommodates voice and data communications, including pulse metering, with a battery voltage of -24V. The MTU voltage during this mode is defeated by the zener clamp design regardless of the state of RC. It is important to have RC low to disable the ringing voltage. Only the $\overline{SHD}$ output is valid during this mode.

Power Denial Mode

The HC5517 will enter the power denial mode whenever F1 is a logic low. During power denial, the tip and ring amplifiers are active. The DC voltages of both amplifiers are near ground, resulting in a maximum loop current of 7mA. Both the $\overline{SHD}$ and the $\overline{RTD}$ detector output are invalid.

Table 2 summarizes the operating modes of the HC5517 application circuit. The table indicates the valid detectors in each mode as well as valid application circuit operation.

TABLE 3. HC5517 APPLICATION CIRCUIT OPERATING MODES SUMMARY

BATTERY SWITCH	F1	RC	MODE	DETECTORS VALID		APPLICATION CIRCUIT VALID	
				$\overline{SHD}$	$\overline{RTD}$	MTU	CENTERING
-24V	0	0	Power Denial				
-24V	0	1	Invalid				
-24V	1	0	Off-Hook Active	√			
-24V	1	1	Invalid				
-80V	0	0	Power Denial			√	
-80V	0	1	Invalid				
-80V	1	0	On-Hook Standby	√		√	
-80V	1	1	Ringing	(Note)	√		√

NOTE: During Ringing, the $\overline{SHD}$ output will be active for both on-hook and off-hook conditions. The AC current, for the on-hook condition, exceeds the $\overline{SHD}$ threshold of 12mA. Valid off-hook detection during ringing is provided by the $\overline{RTD}$ output only.

Operation of the Battery Switch

The battery switch is used to select between the off-hook battery of -24V and the ringing/standby battery of -80V. When T_1 is off (battery switch is logic low) the MOSFET T_3 is off and the -24V battery is supplied to the SLIC through D_{10}. When T_1 is on (battery switch is logic high) current flows through the collector of T_1 turning on the zener D_9. When D_9 turns on, the gate of the MOSFET is positive with respect to the drain (-80V) and T_3 turns on. Turning T_3 on connects the -80V battery to the SLIC through D_7. This in turn reverse biases D_{10}, isolating the two supplies.

Transhybrid Balance (Voice Signal)

The purpose of the transhybrid circuit is to remove the receive signal (V-REC) from the transmit signal (V-XMIT), thereby preventing an echo on the transmit side. This is accomplished by using an external op amp (usually part of the CODEC) and by the inversion of the signal from the SLIC's 4-wire receive port (V_{RX}) to the SLIC's 4-wire transmit port (OUT1).

The external transhybrid circuit is shown in Figure 10. The effects of capacitors C_5, C_7 and C_8 are negligible and therefore omitted from the analysis. The input signal (V-REC) will be subtracted from the output signal (V-XMIT) if I_1 equals I_2 are equal and opposite in phase. A node analysis yields the following equation:

$$\frac{V\text{–}REC}{R_2} + \frac{OUT1}{R_3} = 0 \qquad \text{(EQ. 36)}$$

The value of R_2 is then:

$$R_2 = -R_3 \bullet \frac{V\text{–}REC}{OUT1} \qquad \text{(EQ. 37)}$$

Given that OUT1 is equal to -1/3 of V-REC (Equation 16) and V-REC is equal to VTR ($A_{4\text{-Wire-2-Wire}}$ = 1, Equation 15), then $R_2 = 3R_3$. A transhybrid balance greater than 30dB can be achieved by using 1% resistors values.

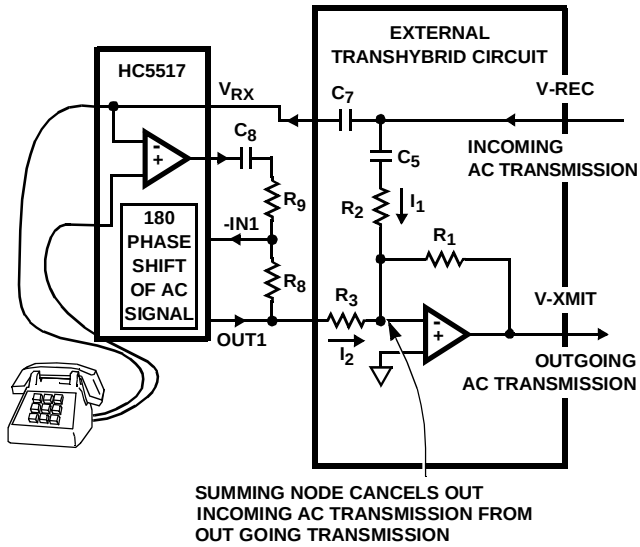


FIGURE 10. TRANSHYBRID CIRCUIT (VOICE SIGNAL)

Transhybrid Balance (Pulse Metering)

Transhybrid balance of the pulse metering signal is accomplished in 2 stages. The first stage uses the SLIC's internal op amp to invert the phase of the pulse metering signal. The second stage sums the inverted pulse metering signal with the incoming signal for cancellation in the transhybrid amplifier. A third network can be added to offset both tip and ring by the peak amplitude of the pulse metering signal. This will allow both the maximum voice and pulse metering signals to occur at the same time with no distortion.

Pulse Metering

Pulse metering or Teletax is used outside the United States for billing purposes at pay phones. A 12kHz or 16kHz burst is injected into the 4-wire side of the SLIC and transmitted across the tip and ring lines from the central office to the pay phone. For more information about pulse metering than covered here reference application note AN9608 "Implementing Pulse Metering for the HC5509 Series of SLICs".

Inverting Amplifier (A1)

The pulse metering signal is injected in the -IN1 pin of the SLIC. This pin is the inverting input of the internal amplifier (A_1) that is used to invert the pulse metering signal for later cancellation. The components required for pulse metering are C_6 and R_5, are shown in Figure 11. The pulse metering signal is AC coupled to prevent a DC offset on the input of the internal amplifier. The value of C_6 should be 10µF. The expression for the voltage at OUT1 is given in Equation 38

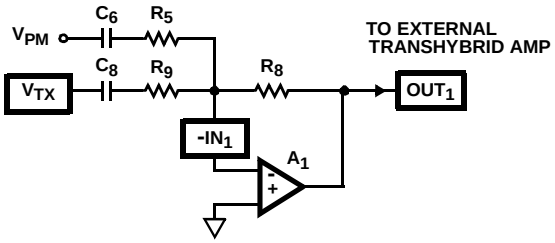


FIGURE 11. PULSE METERING PHASE SHIFT AMPLIFIER DESIGN

$$V_{OUT1} = -V_{TX} \bullet \frac{R_8}{R_9} - V_{PM} \bullet \frac{R_8}{R_5} \quad \text{(EQ. 38)}$$

The first term is the gain of the feedback voltage from the 2-wire side and the second term is the gain of the injected pulse metering signal. The effects of C_6 and C_8 are negligible and therefore omitted from the analysis.

The injected pulse metering output term of Equation 38 is shown below in Equation 39 and rearranged to solve for R_5 in Equation 40.

$$V_{OUT1(injected)} = V_{PM} \bullet \frac{R_8}{R_5} = 1 \quad \text{(EQ. 39)}$$

$$R_5 = R_8 \quad \text{(EQ. 40)}$$

The ratio of R_8 to R_5 is set equal to one and results in unity gain of the pulse metering signal from 4-wire side to 2-wire side. The value of R_8 is considered to be a constant since it is selected based on impedance matching requirements.

Cancellation of the Pulse Metering Signal

The transhybrid cancellation technique that is used for the voice signal is also implemented for pulse metering. The technique is to drive the transhybrid amplifier with the signal that is injected on the 4-wire side, then adjust its level to match the amplitude of the feedback signal, and cancel the signals at the summing node of an amplifier.

NOTE: The CA741C operational amplifier is used in the application as a “stand in” for the operational amplifier that is traditionally located in the CODEC, where transhybrid cancellation is performed.

Referring to Figure 3, V_{TX} is the 2-wire feedback used to drive the internal amplifier (A1) which in turn drives the OUT1 pin of the SLIC. The voltage measured at V_{TX} is related to the loop impedance as follows:

$$V_{TX} = \frac{-200}{R_L} \bullet V_{PM} \bullet G_{PM} \quad \text{(EQ. 41)}$$

For a 600Ω termination and a pulse metering gain (G_{PM}) of 1, the feedback voltage (V_{TX}) is equal to one third the injected pulse metering signal of the 4-wire side. Note, depending upon the line impedance characteristics and the degree of impedance matching, the pulse metering gain may differ from the voice gain. The pulse metering gain (G_{PM}) must be accounted for in the transhybrid balance circuit.

The polarity of the signal at OUT1 (Equation 38) is opposite of V_{PM} allowing the circuit of Figure 12 to perform the final stage of transhybrid cancellation.

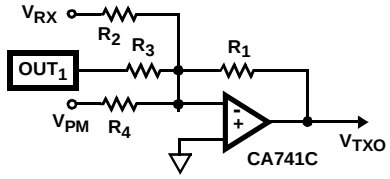


FIGURE 12. CANCELLATION OF THE PULSE METERING SIGNAL

The following equations do not require much discussion. They are based on inverting amplifier design theory. The voice path V_{RX} signal has been omitted for clarity. All reference designators refer to components of Figures 11 and 12.

$$V_{TXO} = -R_8 \bullet \left(-\frac{V_{TX}}{R_9} - \frac{V_{PM}}{R_5} \right) \bullet \frac{R_1}{R_3} - \left(V_{PM} \bullet \frac{R_1}{R_4} \right) \quad \text{(EQ. 42)}$$

The first term refers to the signal at OUT1 and the second term refers to the 4-wire side pulse metering signal. Since ideal transhybrid cancellation implies V_{TXO} equals zero when a signal is injected on the 4-wire side, V_{TXO} is set to zero and the resulting equation is shown below.

$$0 = R_8 \bullet \left(\frac{V_{TX}}{R_9} + \frac{V_{PM}}{R_5} \right) \bullet \frac{R_1}{R_3} - \left(V_{PM} \bullet \frac{R_1}{R_4} \right) \quad \text{(EQ. 43)}$$

Rearranging terms of Equation 43 and solving for R_4 results in Equation 44. This is the only value to be calculated for the transhybrid cancellation. All other values either exist in the application circuit or have been calculated in previous sections of this data sheet.

$$R_4 = \left(\frac{R_8}{R_3} \bullet \left(\frac{-200 \bullet G_{PM}}{R_L \bullet R_9} + \frac{1}{R_5} \right) \right)^{-1} \quad \text{(EQ. 44)}$$

The value of R_4 (Figure 12) is 12.37kΩ given the following set of values:

R_8 = 40kΩ
R_9 = 40kΩ
R_L = 600Ω
R_3 = 8.25kΩ
R_5 = 40kΩ
G_{PM} = 1

Substituting the same values into Equation 41 and Equation 42, it can be shown that the signal at OUT_1 is equal to -2/3V_{PM}. This result, along with Equation 44 where R_3 equals to 2/3R4, indicates the signal levels into the transhybrid amplifier are equalized by the amplifier gains and opposite in polarity, thereby achieving transhybrid balance at V_{TXO}.

Additional Tip and Ring Offset Voltage

A DC offset is required to level shift tip and ring from ground and V_{BAT} respectively. By design, the tip amplifier is offset 4V below ground and the ring amplifier is offset 4V above V_{BAT}. The 4V offset was designed so that the peak voice signal could pass through the SLIC without distortion. Therefore, to maintain distortion free transmission of pulse metering and voice, an additional offset equal to the peak of the pulse metering signal is required.

The tip and ring voltages are offset by a voltage divider network on the V_{RX} pin. The V_{RX} pin is a unity gain input designed as the 4-wire side voice input for the SLIC. Figure 13 details the circuit used to generate the additional offset voltage.

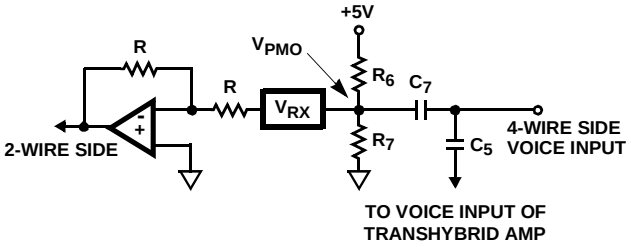


FIGURE 13. PULSE METERING OFFSET GENERATION

The amplifier shown is the tip amplifier. Other signals are connected to the summing node of the amplifier but only those components used for the offset generation are shown. The offset generated at the output of the tip amplifier is summed at the ring amplifier inverting input to provide a positive offset from the battery voltage. The connection to the ring amplifier was omitted from Figure 13 for clarity, refer to Figure 3 for details.

The term V_{PMO} is defined to be the offset required for the pulse metering signal. The value of the offset voltage is calculated as the peak value of the pulse metering signal. Equation 45 assumes the amplitude of the pulse metering signal is expressed as an RMS voltage.

$$V_{PMO} = \sqrt{2} \bullet V_{PM} \quad \text{(EQ. 45)}$$

The value of R_6 can be calculated from the following equation:

$$R_6 = \left(\frac{R_7 R}{R_7 + R}\right)\left(\frac{5 - V_{PMO}}{V_{PMO}}\right) \quad \text{(EQ. 46)}$$

The component labeled R is the internal summing resistor of the tip amplifier and has a typical value of 108kΩ. The value of R_7 should be selected in the range of 4.99kΩ and 10kΩ. Staying within these limits will minimize the parallel loading effects of the internal resistor R on R_7 as well as minimize the constant power dissipation introduced by the divider.

Solving Equation 45 for $1V_{RMS}$ results in a 1.414V requirement for V_{PMO}. Setting R_7 of Equation 46 to 10kΩ and substituting the values for V_{PMO} and R yields 23.2kΩ for R_6. The value of R_6 can be rounded to the nearest standard value without significantly changing the offset voltage.

Single Low Voltage Supply Operation

The application circuit shown Figure 15 requires 2 low voltage supplies (+5V, -5V). The following application offers away to make use of a 2.5V reference, provided with some CODEC, to operate the transhybrid balance amplifier from a single +5V supply. The implementation is shown in Figure 14. Notice that the three inputs from the SLIC must all be AC coupled to insure the proper DC gain through the CODECs internal op amp. The resistor Ra is not used for gain setting and is only intended to balance the DC offsets generated by the input bias current of the CODEC amplifier. If the DC offsets generated by the input bias currents are negligible, then Ra may be omitted from the circuit. Ca may be required for decoupling of the voltage reference pin and does not contribute to the response of the amplifier.

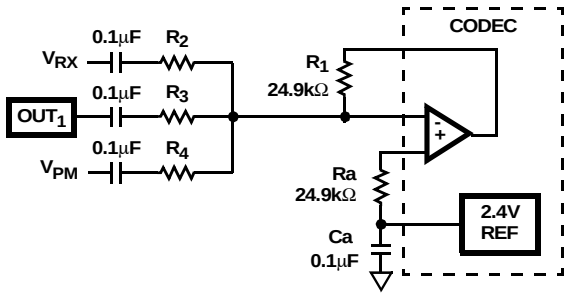


FIGURE 14. SINGLE LOW VOLTAGE SUPPLY OPERATION

Layout Guidelines and Considerations

The printed circuit board trace length to all high impedance nodes should be kept as short as possible. Minimizing length will reduce the risk of noise or other unwanted signal pickup. The short lead length also applies to all high gain inputs. The set of circuit nodes that can be categorized as such are:

- V_{RX} pin 27, the 4-wire voice input.
- -IN1 pin 13, the inverting input of the internal amplifier.
- V_{REF} pin 3, the noninverting input to ring feed amplifier.
- V_{RING} pin 24, the 20V/V input for the ringing signal.
- U1 pin 2, inverting input of external amplifier.

For multi layer boards, the traces connected to tip should not cross the traces connected to ring. Since they will be carrying high voltages, and could be subject to lightning or surge depending on the application, using a larger than minimum trace width is advised.

The 4-wire transmit and receive signal paths should not cross. The receive path is any trace associated with the V_{RX} input and the transmit path is any trace associated with V_{TX} output. The physical distance between the two signal paths should be maximized to reduce crosstalk.

The mode control signals and detector outputs should be routed away from the analog circuitry. Though the digital

signals are nearly static, care should be taken to minimize coupling of the sharp digital edges to the analog signals.

The part has two ground pins, one is labeled AGND and the other BGND. Both pins should be connected together as close as possible to the SLIC. If a ground plane is available, then both AGND and BGND should be connected directly to the ground plane.

A ground plane that provides a low impedance return path for the supply currents should be used. A ground plane provides isolation between analog and digital signals. If the layout density does not accommodate a ground plane, a single point grounding scheme should be used.

Application Pin Descriptions

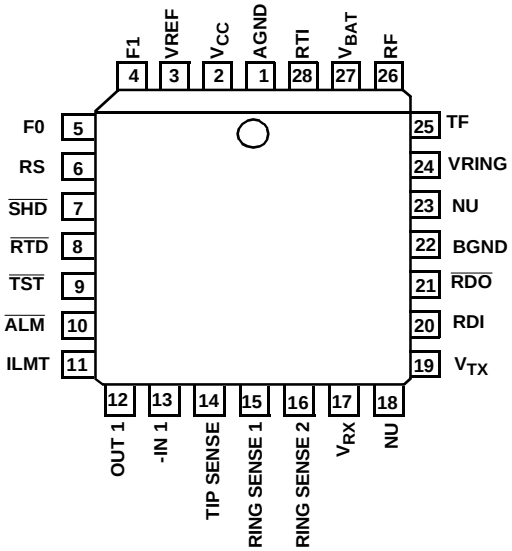
PLCC	SYMBOL	DESCRIPTION
1	AGND	Analog Ground - To be connected to zero potential. Serves as a reference for the transmit output and receive input terminals.
2	V_{CC}	Positive Voltage Source - Most Positive Supply.
3	V_{REF}	Ring amplifier reference override. An external voltage connected to this pin will override the internal $V_{BAT}/2$ reference.
4	F1	Power Denial -A low active TTL compatible logic control input. When enabled, the output of the ring amplifier will ramp close to the output voltage of the tip amplifier.
5	F0	TTL compatible logic control input that must be tied high for proper SLIC operation.
6	RS	TTL compatible logic control input that must be tied high for proper SLIC operation.
7	$\overline{SHD}$	Switch Hook Detection - An active low TTL compatible logic output. Indicates an offhook condition.
8	RTD	Ring Trip Detection - An active low TTL compatible logic output. Indicates an off-hook condition when the phone is ringing.
9	$\overline{TST}$	A TTL logic input. A low on this pin will keep the SLIC in a power down mode. The $\overline{TST}$ pin in conjunction with the $\overline{ALM}$ pin can provide thermal shutdown protection for the SLIC. Thermal shutdown is implemented by a system controller that monitors the $\overline{ALM}$ pin. When the $\overline{ALM}$ pin is active (low) the system controller issues a command to the $\overline{TST}$ pin (low) to power down the SLIC. The timing of the thermal recovery is controlled by the system controller.
10	$\overline{ALM}$	A TTL compatible active low output which responds to the thermal detector circuit when a safe operating die temperature has been exceeded.
11	I_{LMT}	Loop Current Limit - Voltage on this pin sets the short loop current limiting conditions using a resistive voltage divider.
12	OUT1	The analog output of the spare operational amplifier.
13	-IN1	The inverting analog input of the spare operational amplifier. Note that the non-inverting input of the amplifier is internally connected to AGND.
14	TIP SENSE	An analog input connected to the TIP (more positive) side of the subscriber loop through a feed resistor and ring relay contact. Functions with the RING terminal to receive voice signals from the telephone and for loop monitoring purpose.
15	RING SENSE 1	An analog input connected to the RING (more negative) side of the subscriber loop through a feed resistor. Functions with the TIP terminal to receive voice signals from the telephone and for loop monitoring purposes.
16	RING SENSE 2	This is an internal sense mode that must be tied to RING SENSE 1 for proper SLIC operation.
17	V_{RX}	Receive Input, 4-Wire Side - A high impedance analog input. AC signals appearing at this input drive the Tip Feed and Ring Feed amplifiers deferentially.
18	NU	Not used in this application.This pin should be left floating.
19	V_{TX}	Transmit Output, 4-Wire Side - A low impedance analog output which represents the differential voltage across TIP and RING. Since the DC level of this output varies with loop current, capacitive coupling to the next stage is necessary.
20	RDI	TTL compatible input to drive the uncommitted relay driver.
21	$\overline{RDO}$	This is the output of the uncommitted relay driver.
22	BGND	Battery Ground - To be connected to zero potential. All loop current and some quiescent current flows into this terminal.
23	NU	Not used in this application. This pin should be either grounded or left floating.
24	V_{RING}	Ring signal input (0V to $3V_{PEAK}$ at 20Hz).
25	TF	This is the output of the tip amplifier.
26	RF	This is the output of the ring amplifier.
27	V_{BAT}	The negative battery source.

Application Pin Descriptions (Continued)

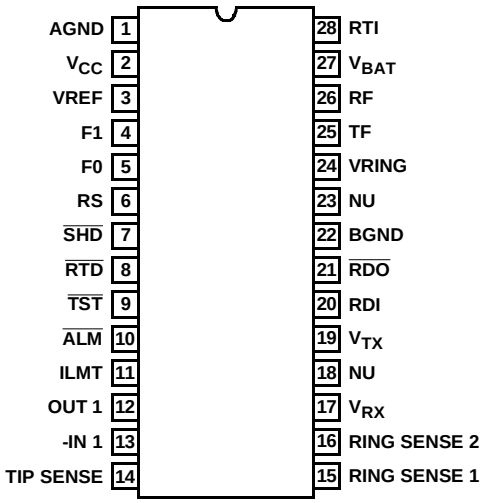
PLCC	SYMBOL	DESCRIPTION
28	RTI	Ring Trip Input - This pin is connected to the external negative peak detector output for ring trip detection.

Pinouts

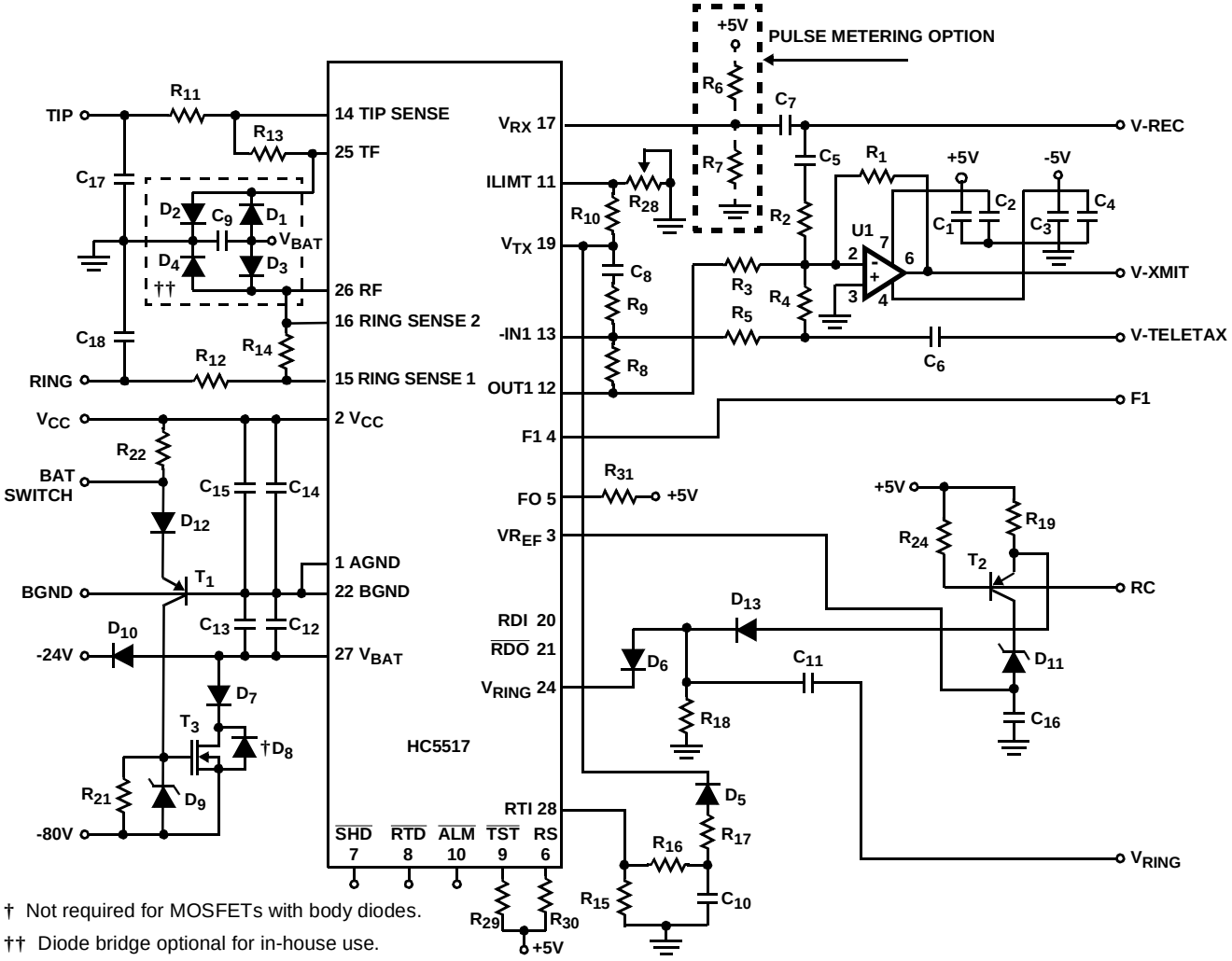
HC5517 (PLCC)
TOP VIEW



HC5517 (SOIC)
TOP VIEW



Applications Circuit



† Not required for MOSFETs with body diodes.

FIGURE 15. APPLICATION CIRCUIT

HC5517EVAL Evaluation Board Parts List

COMPONENT	VALUE	TOLERANCE	RATING	COMPONENT	VALUE	TOLERANCE	RATING
SLIC	HC5517	n/a	n/a	C_2, C_4, C_{15}	0.1µF	20%	50V
R_1, R_2	24.9kΩ	1%	1/4W	C_5, C_7	10µF	20%	20V
R_3	8.25kΩ	1%	1/4W	C_6, C_8	0.47µF	20%	20V
R_4	12.1kΩ	1%	1/4W	C_9, C_{12}	0.01µF	20%	100V
R_5, R_8, R_9	40kΩ	1%	1/4W	C_{10}	1.0µF	20%	50V
R_6 (Not Provided)	23.2kΩ	1%	1/4W	C_{11}	100µF	20%	5V
R_7 (Not Provided)	10kΩ	1%	1/4W	C_{13}	0.1µF	20%	100V
R_{10}	100kΩ	5%	1/4W	C_{16}	0.5µF	20%	50V
R_{11-14}	50Ω	1%	1/4W	C_{17}, C_{18}	3300pF	20%	100V
R_{15}	47kΩ	1%	1/4W	D_{1-4}, D_7, D_8, D_{10}	1N4007		100V, 1A
R_{16}	1.5MΩ	1%	1/4W	D_5, D_6, D_{12}, D_{13}	1N914		100V, 1A
R_{17}	56.2kΩ	1%	1/4W	D_9	1N4744		15V, 1W
R_{18}	1.1kΩ	1%	1/4W	D_{11}	1N5255		28V, 1/2-Wire
R_{19}	825Ω	1%	1/4W	T_1	NTE 383		100V, 1A
R_{22}, R_{29}, R_{30}, R_{31}	10kΩ	5%	1/4W	T_2	2N2907		60V,150mA
R_{24}	47kΩ	5%	1/4W	T_3	RFP2N10 or equivalent		100V, 2A
R_{25-27}	560Ω	5%	1/4W	F1, RC, Battery	SPDT Toggle Switches, Center Off.		
R_{28}	20kΩ Potentiometer		1/4W	U1	CA741C OpAmp		
R_{21}	47kΩ	5%	1/4W	Textool Socket	228-5523		
C_1, C_3, C_{14}	0.01µF	20%	50V				