PRELIMINARY | Data Sheet | March 13, 2006 | FN6222.0

32x32 Video Crosspoint with Differential Inputs

The ISL59533 is a 32x32 integrated video crosspoint switch matrix with input and output buffers and On-Screen Display (OSD) insertion. The ISL59533 is ideal for routing video signals in security and video-on-demand systems. This device operates from a single +5V supply. Any output can be switched to any of the 32 input video signal sources and OSD information through an internal, dedicated fast 2:1 mux (15ns switching times) located before the output buffer. Also, any one input can be broadcast to all 32 outputs.

The ISL59533 offers a -3dB signal bandwidth of 300MHz. The differential gain and phase at 0.01% and 0.03° respectively, along with 0.1dB flatness out to 35MHz, make the ISL59533 suitable for many video applications.

The switch matrix configuration and output buffer gain are programmed through an SPI/QSPI™-compatible, three-wire serial interface. The ISL59533 interface is set up to facilitate both fast updates and initialization. On power-up, all outputs are initialized in the disabled state to avoid output conflicts within the user system.

The ISL59533 is available in a 356-pin BGA package and specified over an extended -40°C to +85°C temperature range.

The ISL59533 has single-supply signal operation. It can accommodate input and output voltages from ground to >3.5V. It also has fully differential inputs. The differential input span is ±1.5V. The output offset is applied via a group reference input.

Features

- 32x32 non-blocking switch with buffered inputs and outputs
- Differential inputs
- Operates from a single +5V supply
- Output gain switchable +1 or +2
- Tri-state output
- -80dB Isolation at 6MHz
- 0.01%/0.03° dG/dP
- Pb-Free plus anneal available (RoHS compliant)

Applications

- Security camera switching
- RGB routing
- HDTV routing

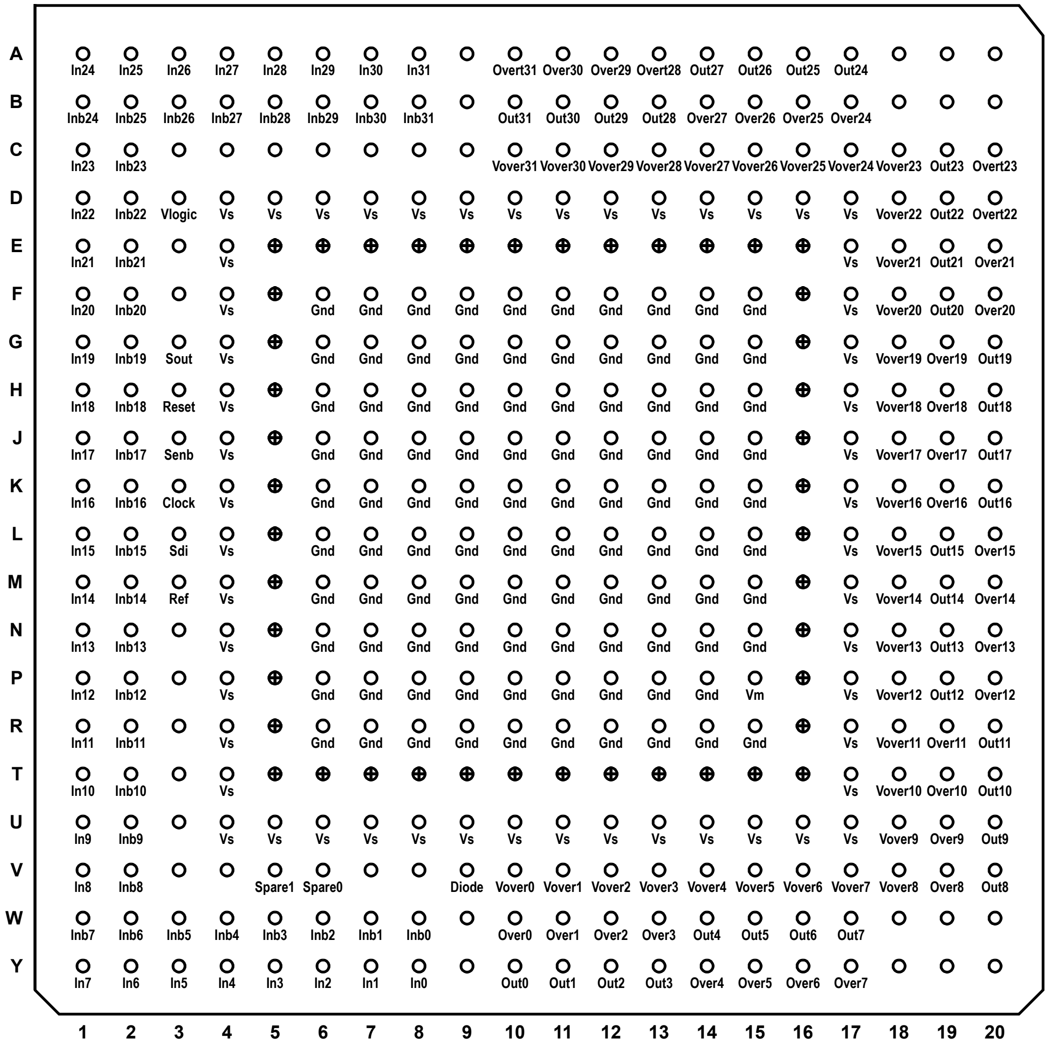
Ordering Information

PART NUMBER	TAPE & REEL	PACKAGE	PKG. DWG. #
ISL59533IKEZ (See Note)	-	356-Pin BGA (Pb-Free)	V356.27x27A

NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Pinout

ISL59533
(356-PIN BGA)
TOP VIEW



	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
A	In24	In25	In26	In27	In28	In29	In30	In31		Overt31	Over30	Over29	Overt28	Out27	Out26	Out25	Out24			
B	Inb24	Inb25	Inb26	Inb27	Inb28	Inb29	Inb30	Inb31		Out31	Out30	Out29	Out28	Over27	Over26	Over25	Over24			
C	In23	Inb23								Vover31	Vover30	Vover29	Vover28	Vover27	Vover26	Vover25	Vover24	Vover23	Out23	Overt23
D	In22	Inb22	Vlogic	Vs	Vs	Vs	Vs	Vs	Vs	Vs	Vs	Vs	Vs	Vs	Vs	Vs	Vs	Vover22	Out22	Overt22
E	In21	Inb21		Vs	⊕	⊕	⊕	⊕	⊕	⊕	⊕	⊕	⊕	⊕	⊕	⊕	Vs	Vover21	Out21	Over21
F	In20	Inb20		Vs	⊕	Gnd	Gnd	Gnd	Gnd	Gnd	Gnd	Gnd	Gnd	Gnd	Gnd	⊕	Vs	Vover20	Out20	Over20
G	In19	Inb19	Sout	Vs	⊕	Gnd	Gnd	Gnd	Gnd	Gnd	Gnd	Gnd	Gnd	Gnd	Gnd	⊕	Vs	Vover19	Over19	Out19
H	In18	Inb18	Reset	Vs	⊕	Gnd	Gnd	Gnd	Gnd	Gnd	Gnd	Gnd	Gnd	Gnd	Gnd	⊕	Vs	Vover18	Over18	Out18
J	In17	Inb17	Senb	Vs	⊕	Gnd	Gnd	Gnd	Gnd	Gnd	Gnd	Gnd	Gnd	Gnd	Gnd	⊕	Vs	Vover17	Over17	Out17
K	In16	Inb16	Clock	Vs	⊕	Gnd	Gnd	Gnd	Gnd	Gnd	Gnd	Gnd	Gnd	Gnd	Gnd	⊕	Vs	Vover16	Over16	Out16
L	In15	Inb15	Sdi	Vs	⊕	Gnd	Gnd	Gnd	Gnd	Gnd	Gnd	Gnd	Gnd	Gnd	Gnd	⊕	Vs	Vover15	Out15	Over15
M	In14	Inb14	Ref	Vs	⊕	Gnd	Gnd	Gnd	Gnd	Gnd	Gnd	Gnd	Gnd	Gnd	Gnd	⊕	Vs	Vover14	Out14	Over14
N	In13	Inb13		Vs	⊕	Gnd	Gnd	Gnd	Gnd	Gnd	Gnd	Gnd	Gnd	Gnd	Gnd	⊕	Vs	Vover13	Out13	Over13
P	In12	Inb12		Vs	⊕	Gnd	Gnd	Gnd	Gnd	Gnd	Gnd	Gnd	Gnd	Gnd	Vm	⊕	Vs	Vover12	Out12	Over12
R	In11	Inb11		Vs	⊕	Gnd	Gnd	Gnd	Gnd	Gnd	Gnd	Gnd	Gnd	Gnd	Gnd	⊕	Vs	Vover11	Over11	Out11
T	In10	Inb10		Vs	⊕	⊕	⊕	⊕	⊕	⊕	⊕	⊕	⊕	⊕	⊕	⊕	Vs	Vover10	Over10	Out10
U	In9	Inb9		Vs	Vs	Vs	Vs	Vs	Vs	Vs	Vs	Vs	Vs	Vs	Vs	Vs	Vs	Vover9	Over9	Out9
V	In8	Inb8			Spare1	Spare0			Diode	Vover0	Vover1	Vover2	Vover3	Vover4	Vover5	Vover6	Vover7	Vover8	Over8	Out8
W	Inb7	Inb6	Inb5	Inb4	Inb3	Inb2	Inb1	Inb0		Over0	Over1	Over2	Over3	Out4	Out5	Out6	Out7			
Y	In7	In6	In5	In4	In3	In2	In1	In0		Out0	Out1	Out2	Out3	Over4	Over5	Over6	Over7			

⊕ = NO BALLS

PAD NAME “GND” IS THE SAME AS PACKAGE OR BALL NAME “GROUND” OR “G”
PAD NAME “VS” IS THE SAME AS PACKAGE OR BALL NAME “POWER” OR “P”
ALL PADS ARE 70µ x 70µ

Absolute Maximum Ratings (T_A = 25°C)

Supply Voltage between V_S and GND 6V
Maximum Continuous Output Current 40mA
Ambient Operating Temperature . . . . -TBD°C to +TBD°C
Maximum Die Temperature . . . .+125°C
Storage Temperature . . . . -TBD°C to +TBD°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typical values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$

DC Electrical Specifications V_S = 5V

PARAMETER	DESCRIPTION	CONDITION	MIN	TYP	MAX	UNIT
V_S	Supply Range		4.5		5.5	V
V_D	Digital Supply	Establishes serial output high level	1.2		5.5	V
G	Gain	G = 1, R_L = 500Ω	0.97	1	1.03	V/V
		G = 2, R_L = 150Ω	1.94	2	2.06	%
GM	Gain Matching (to average of all other outputs)	G = 1	-1.5	1	1.5	%
		G = 2		0.5	1.0	%
V_{IN}	Input Voltage Range	G = 1	0		3.5	V
V_{OUT}	Output Voltage Range	G = 2, R_L = 150Ω	0		4.0	V
I_B	Input Bias Current			7	15	µA
V_{OS}	Output Offset Voltage	A_V = 1	-25	0	25	mV
		A_V = 2	-70	0	70	mV
I_{OUT}	Output Current	Sourcing, R_L = 10Ω to GND	60	100		mA
		Sinking, R_L to 2.5V	25	35		mA
PSRR	Power Supply Rejection Ratio					dB
I_S	Supply Current	Enabled, all outputs enable, no load current		600	700	mA
		Enable, all outputs disable, no load current		245		mA
		Disabled		1.6	2.2	mA
		Supply current per output channel		9.5		mA

AC Electrical Specifications

PARAMETER	DESCRIPTION	CONDITION	MIN	TYP	MAX	UNIT
BW -3dB	3dB Bandwidth	V_{OUT} = 200mV_{P-P}, A_V = 2		320		MHz
BW 0.1dB	0.1dB Bandwidth	V_{OUT} = 200mV_{P-P}, A_V = 2		50		MHz
SR	Slew Rate	V_{OUT} = 2V_{P-P}, A_V = 2	360	470		V/µs
T_S	Settling Time to 0.1%	V_{OUT} = 2V_{P-P}, A_V = 2		12		ns
Glitch	Switching Glitch, Peak	A_V = 1		40		mV
T_{over}	Overlay Delay Time	Beginning of output transition		6		ns
dG/dP	Diff Gain	A_V = 2, R_L = 150Ω		0.01		%
	Diff Phase	A_V = 2, R_L = 150Ω		0.03		%
Xt	Hostile Crosstalk	6MHz		80		dB
V_N	Input Noise Voltage			42		nV/√Hz

Pin Descriptions

NAME	NUMBER	DESCRIPTION
INB4	W4	Complementary input
IN4	Y4	Input
INB5	W3	Complementary input
IN5	Y3	Input
INB6	W2	Complementary input
IN6	Y2	Input
INB7	W1	Complementary input
IN7	Y1	Input
REF	M3	Output reference
GND	GND	Ground
SDI	L3	Serial data input
VS	VS	Power supply
INB8	V2	Complementary input
IN8	V1	Input
INB9	U2	Complementary input
IN9	U1	Input
INB10	T2	Complementary input
IN10	T1	Input
INB11	R2	Complementary input
IN11	R1	Input
VS	VS	Power supply
GND	GND	Ground
INB12	P2	Complementary input
IN12	P1	Input
INB13	N2	Complementary input
IN13	N1	Input
INB14	M2	Complementary input
IN14	M1	Input
INB15	L2	Complementary input
IN15	L1	Input
CLOCK	K3	Serial data clock
VS	VS	Power supply
SENB	J3	Serial enable-inverted
GND	GND	Ground
INB16	K2	Complementary input
IN16	K1	Input
INB17	J2	Complementary input
IN17	J1	Input
INB18	H2	Complementary input

Pin Descriptions (Continued)

NAME	NUMBER	DESCRIPTION
IN18	H1	Input
INB19	G2	Complementary input
IN19	G1	Input
VS	VS	Power supply
GND	GND	Ground
INB20	F2	Complementary input
IN20	F1	Input
INB21	E2	Complementary input
IN21	E1	Input
INB22	D2	Complementary input
IN22	D1	Input
INB23	C2	Complementary input
IN23	C1	Input
RESET	H3	Reset input
VS	VS	Power supply
SOUT	G3	Serial data output
GND	GND	Ground
INB24	B1	Complementary input
IN24	A1	Input
INB25	B2	Complementary input
IN25	A2	Input
INB26	B3	Complementary input
IN26	A3	Input
INB27	B4	Complementary input
IN27	A4	Input
$\overline{\text{INPUTTEST}}$	NONE	Manufacturing test pin - leave open
GND	GND	Ground
GND	GND	Ground
VS	VS	Power supply
VS	VS	Power supply
VLOGIC	D3	Logic power supply for serial output driver
INB28	B5	Complementary input
IN28	A5	Input
INB29	B6	Complementary input
IN29	A6	Input
INB30	B7	Complementary input
IN30	A7	Input
INB31	B8	Complementary input
IN31	A8	Input

Pin Descriptions (Continued)

NAME	NUMBER	DESCRIPTION
VSL	VS	Power supply
VGL	GND	Ground
VS	VS	Power supply
GND	GND	Ground
OVER31	A10	Overlay logic control
VOVER31	C10	Overlay analog input
OUT31	B10	Output
OVER30	A11	Overlay logic control
VOVER30	C11	Overlay analog input
OUT30	B11	Output
OVER29	A12	Overlay logic control
VOVER29	C12	Overlay analog input
OUT29	B12	Output
OVER28	A13	Overlay logic control
VOVER28	C13	Overlay analog input
OUT28	B13	Output
GND	GND	Ground
VS	VS	Power supply
OUT27	A14	Output
VOVER27	C14	Overlay analog input
OVER27	B14	Overlay logic control
OUT26	A15	Output
VOVER26	C15	Overlay analog input
OVER26	B15	Overlay logic control
OUT25	A16	Output
VOVER25	C16	Overlay analog input
OVER25	B16	Overlay logic control
OUT24	A17	Output
VOVER24	C17	Overlay analog input
OVER24	B17	Overlay logic control
GND	GND	Ground
OUTTEST3	NONE	Manufacturing test pin-leave open
VS	VS	Power supply
OVER23	C20	Overlay logic control
VOVER23	C18	Overlay analog input
OUT23	C19	Output
OVER22	D20	Overlay logic control
VOVER22	D18	Overlay analog input
OUT22	D19	Output
OVER21	E20	Overlay logic control

Pin Descriptions (Continued)

NAME	NUMBER	DESCRIPTION
VOVER21	E18	Overlay analog input
OUT21	E19	Output
OVER20	F20	Overlay logic control
VOVER20	F18	Overlay analog input
OUT20	F19	Output
GND	GND	Ground
VS	VS	Power supply
OUT19	G20	Output
VOVER19	G18	Overlay analog input
OVER19	G19	Overlay logic control
OUT18	H20	Output
VOVER18	H18	Overlay analog input
OVER18	H19	Overlay logic control
OUT17	J20	Output
VOVER17	J18	Overlay analog input
OVER17	J19	Overlay logic control
OUT16	K20	Output
VOVER16	K18	Overlay analog input
OVER16	K19	Overlay logic control
OUTTEST2	NONE	Manufacturing test pin-leave open
GND	GND	Ground
VS	VS	Power supply
OVER15	L20	Overlay logic control
VOVER15	L18	Overlay analog input
OUT15	L19	Output
OVER14	M20	Overlay logic control
VOVER14	M18	Overlay analog input
OUT14	M19	Output
OVER13	N20	Overlay logic control
VOVER13	N18	Overlay analog input
OUT13	N19	Output
OVER12	P20	Overlay logic control
VOVER12	P18	Overlay analog input
OUT12	P19	Output
GND	GND	Ground
VS	VS	Power supply
OUT11	R20	Output
VOVER11	R18	Overlay analog input
OVER11	R19	Overlay logic control
OUT10	T20	Output

Pin Descriptions (Continued)

NAME	NUMBER	DESCRIPTION
VOVER10	T18	Overlay analog input
OVER10	T19	Overlay logic control
OUT9	U20	Output
VOVER9	U18	Overlay analog input
OVER9	U19	Overlay logic control
OUT8	V20	Output
VOVER8	V18	Overlay analog input
OVER8	V19	Overlay logic control
VS	VS	Power supply
OUTTEST1	NONE	Manufacturing test pin-leave open
GND	GND	Ground
OVER7	Y17	Overlay logic control
VOVER7	V17	Overlay analog input
OUT7	W17	Output
OVER6	Y16	Overlay logic control
VOVER6	V16	Overlay analog input
OUT6	W16	Output
OVER5	Y15	Overlay logic control
VOVER5	V15	Overlay analog input
OUT5	W15	Output
OVER4	Y14	Overlay logic control
VOVER4	V14	Overlay analog input
OUT4	W14	Output
VS	VS	Power supply
GND	GND	Ground
OUT3	Y13	Output
VOVER3	V13	Overlay analog input
OVER3	W13	Overlay logic control
OUT2	Y12	Output
VOVER2	V12	Overlay analog input
OVER2	W12	Overlay logic control
OUT1	Y11	Output
VOVER1	V11	Overlay analog input
OVER1	W11	Overlay logic control
OUT0	Y10	Output
VOVER0	V10	Overlay analog input
OVER0	W10	Overlay logic control
VS	VS	Power supply
OUTTEST0	NONE	Manufacturing test pin-leave open
GND	GND	Ground

Pin Descriptions (Continued)

NAME	NUMBER	DESCRIPTION
IN0	Y8	Input
INB0	W8	Complementary input
IN1	Y7	Input
INB1	W7	Complementary input
IN2	Y6	Input
INB2	W6	Complementary input
IN3	Y5	Input
INB3	W5	Complementary input
DIODE	V9	Anode of a ground-connected diode: useful for measuring die temperature
VS	VS	Power supply
GND	GND	Ground
VS	VS	Power supply
GND	GND	Ground
SPARE0	V6	Not assigned-do not connect
SPARE1	V5	Not assigned-do not connect
INPUTTEST BUS	NONE	Manufacturing test pin-leave open

Typical Performance Curve

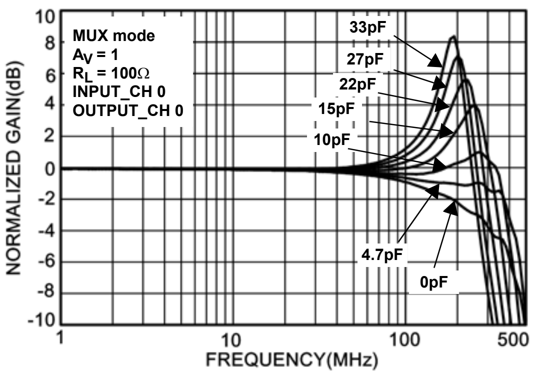


FIGURE 1. FREQUENCY RESPONSE - VARIOUS C_L, A_V = 1, MUX MODE

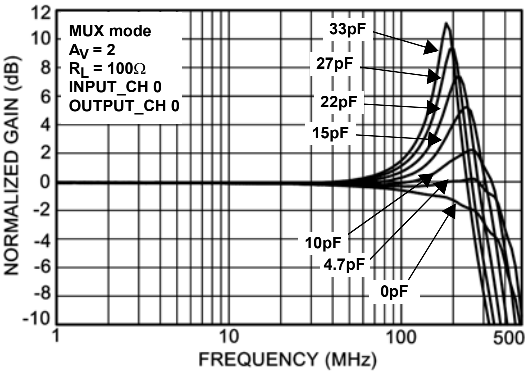


FIGURE 2. FREQUENCY RESPONSE - VARIOUS C_L, A_V = 2, MUX MODE

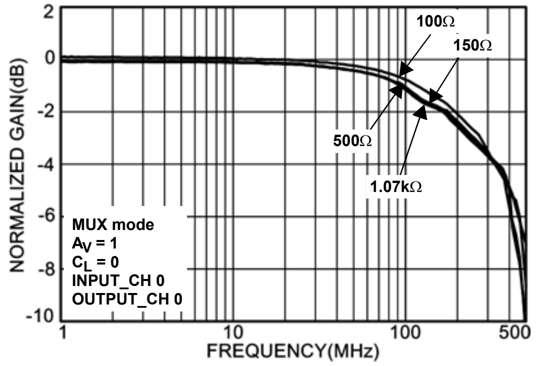


FIGURE 3. FREQUENCY RESPONSE - VARIOUS R_L, A_V = 1, MUX MODE

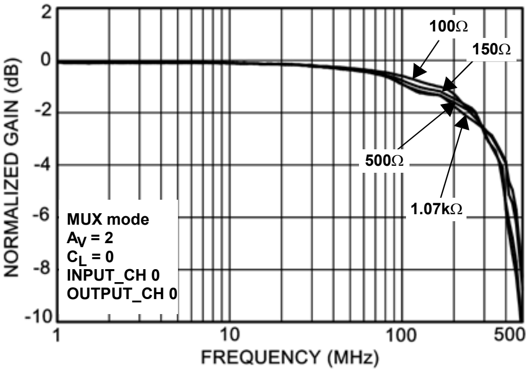


FIGURE 4. FREQUENCY RESPONSE - VARIOUS R_L, A_V = 2, MUX MODE

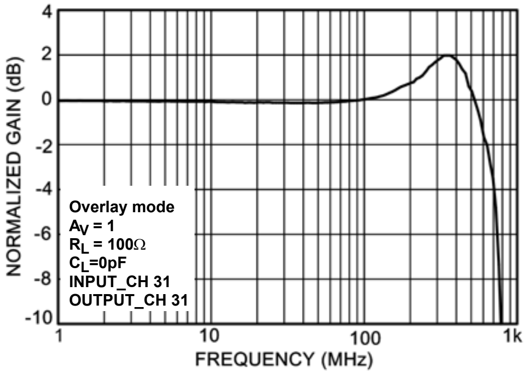


FIGURE 5. FREQUENCY RESPONSE - OVERLAY INPUT, A_V = 1

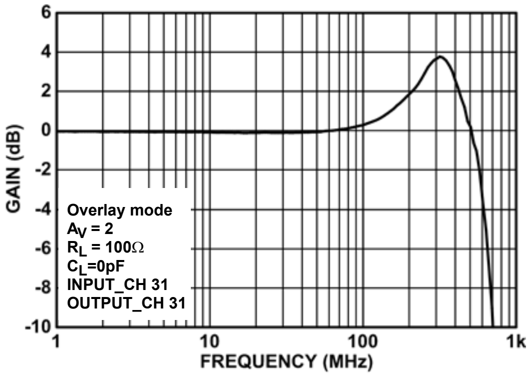


FIGURE 6. FREQUENCY RESPONSE - OVERLAY INPUT, A_V = 2

Typical Performance Curve (Continued)

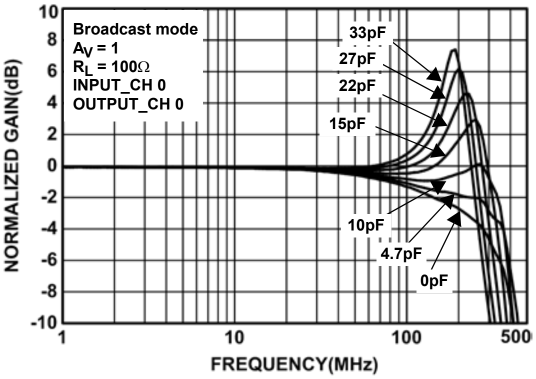


FIGURE 7. FREQUENCY RESPONSE - VARIOUS C_L, $A_V = 1$, BROADCAST MODE

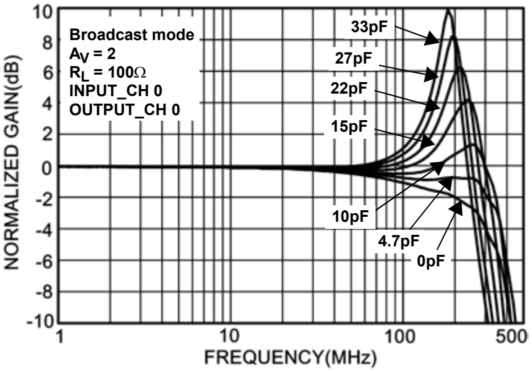


FIGURE 8. FREQUENCY RESPONSE - VARIOUS C_L, $A_V = 2$, BROADCAST MODE

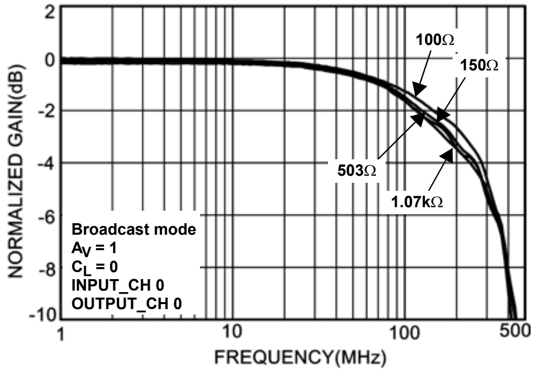


FIGURE 9A. FREQUENCY RESPONSE - VARIOUS R_L, $A_V = 1$, BROADCAST MODE

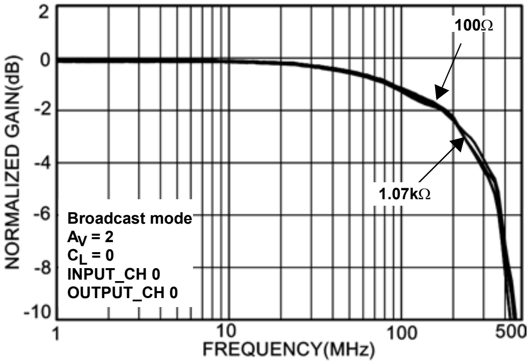


FIGURE 10. FREQUENCY RESPONSE - VARIOUS R_L, $A_V = 2$, BROADCAST MODE

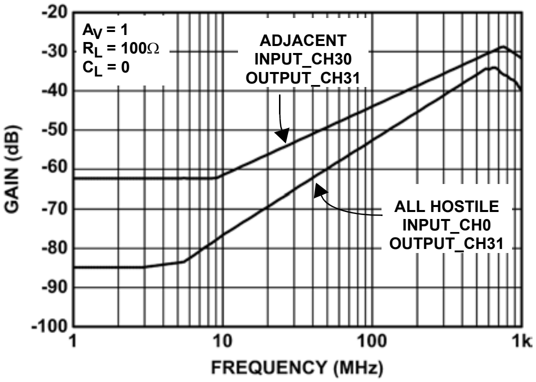


FIGURE 11. CROSSTALK - $A_V = 1$

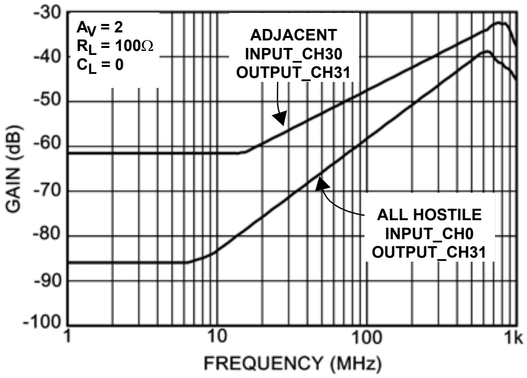


FIGURE 12. CROSSTALK - $A_V = 2$

Typical Performance Curve (Continued)

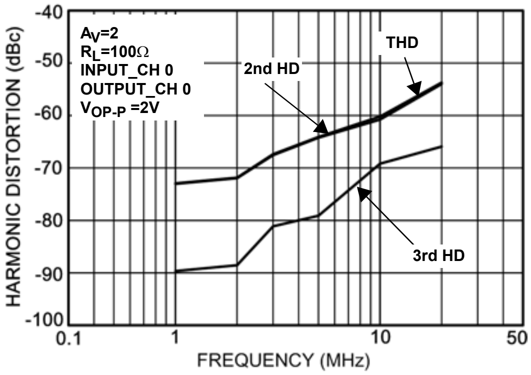


FIGURE 13. HARMONIC DISTORTION vs FREQUENCY

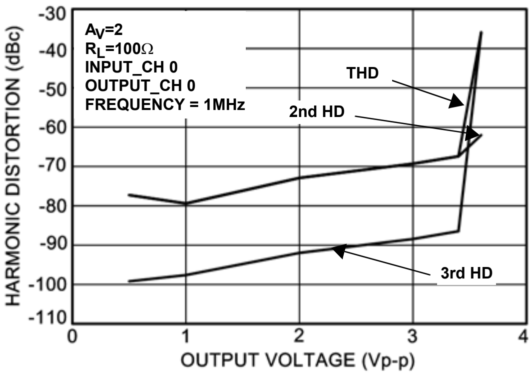


FIGURE 14. HARMONIC DISTORTION vs V_{OUT_P-P}

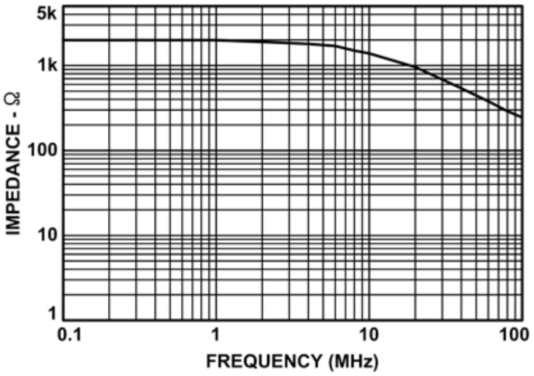


FIGURE 15. DISABLE OUTPUT IMPEDANCE

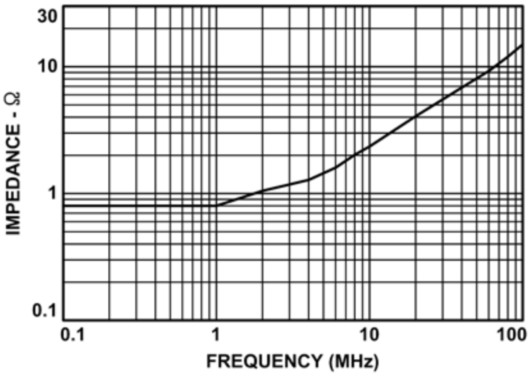


FIGURE 16. ENABLE OUTPUT IMPEDANCE

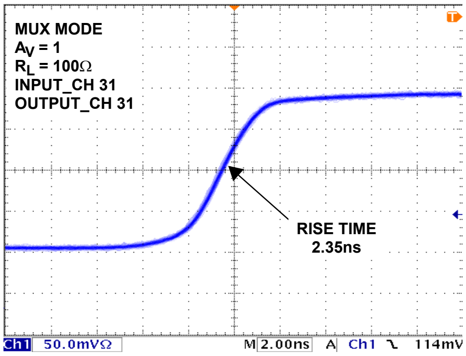


FIGURE 17. RISE TIME - $A_V = 1$

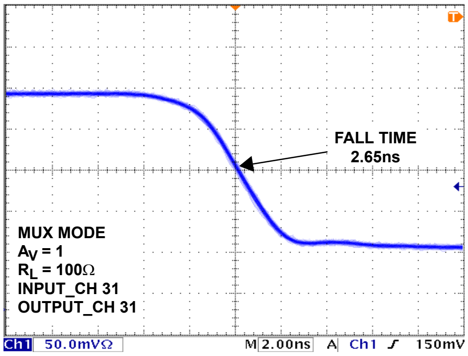


FIGURE 18. FALL TIME - $A_V = 1$

Typical Performance Curve (Continued)

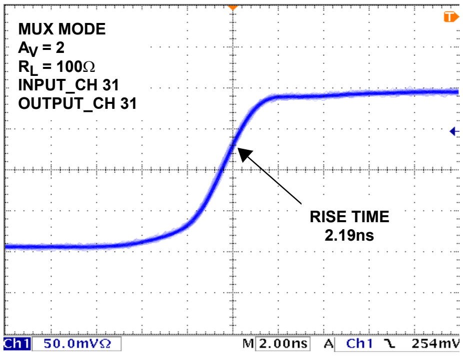


FIGURE 19. RISE TIME - A_V = 2

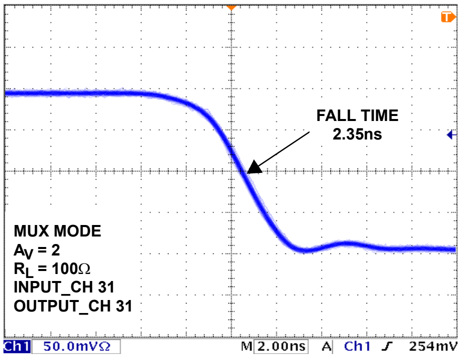


FIGURE 20. FALL TIME - A_V = 2

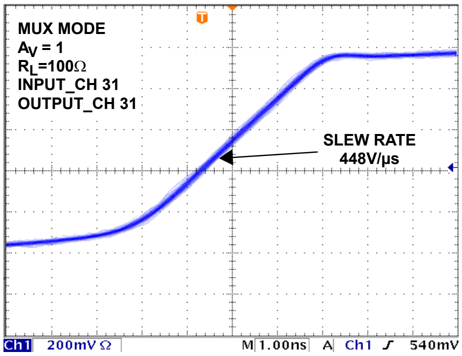


FIGURE 21. RISING SLEW RATE - A_V = 1

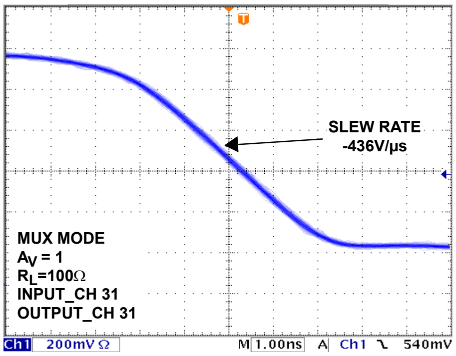


FIGURE 22. FALLING SLEW RATE - A_V = 1

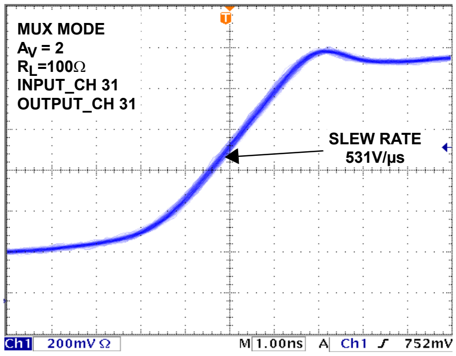


FIGURE 23. RISING SLEW RATE - A_V = 2

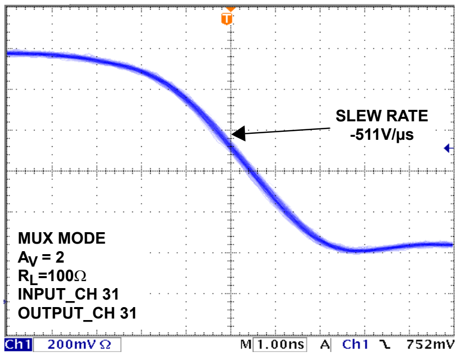


FIGURE 24. FALLING SLEW RATE - A_V = 2

Typical Performance Curve (Continued)

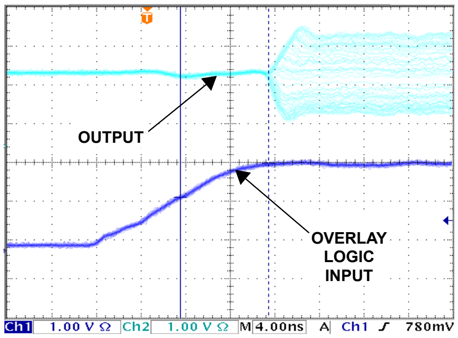


FIGURE 25. OVERLAY SWITCH TURN-ON DELAY TIME

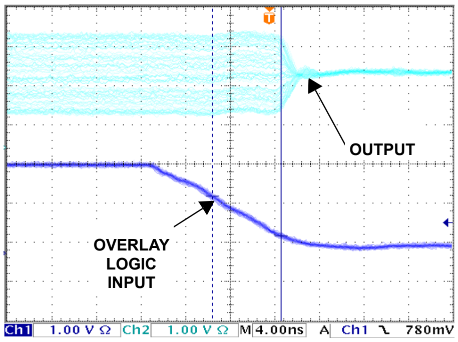


FIGURE 26. OVERLAY SWITCH TURN-OFF DELAY TIME

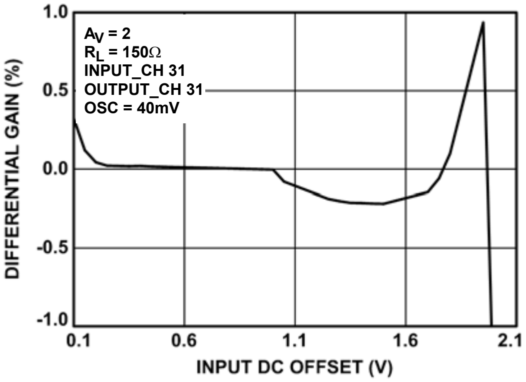


FIGURE 27. DIFFERENTIAL GAIN, A_V = 2

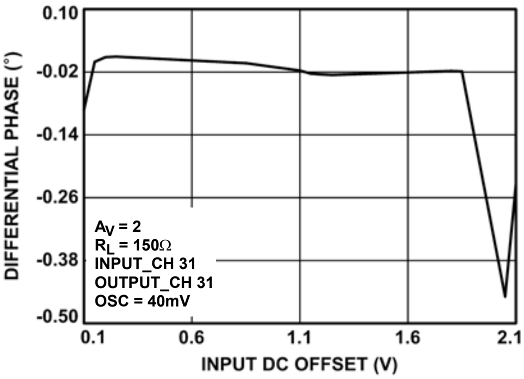


FIGURE 28. DIFFERENTIAL PHASE, A_V = 2

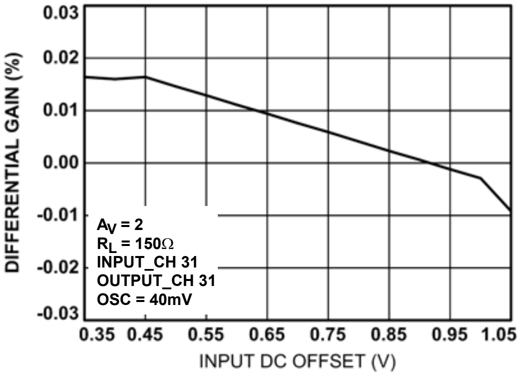


FIGURE 29. DIFFERENTIAL GAIN, A_V = 2

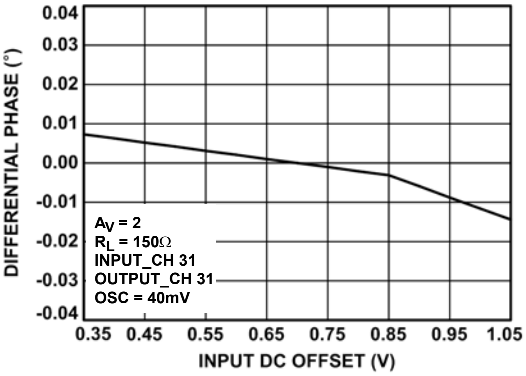


FIGURE 30. DIFFERENTIAL PHASE, A_V = 2

Typical Performance Curve (Continued)

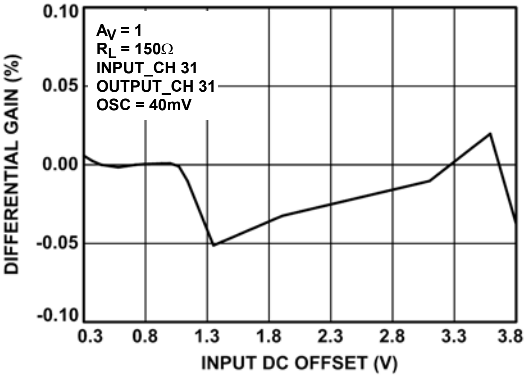


FIGURE 31. DIFFERENTIAL GAIN, $A_V = 1$

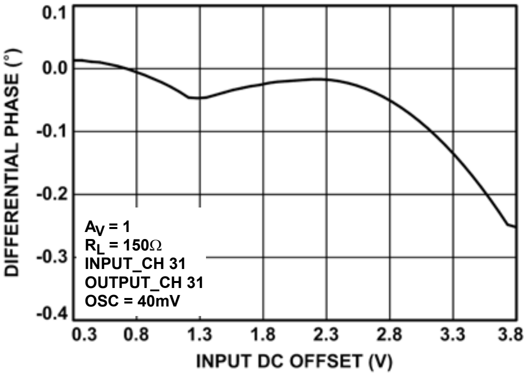


FIGURE 32. DIFFERENTIAL PHASE, $A_V = 1$

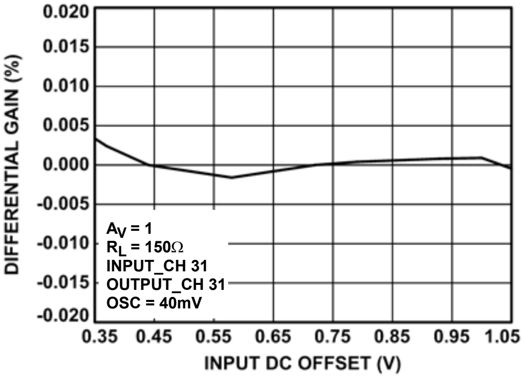


FIGURE 33. DIFFERENTIAL GAIN, $A_V = 1$

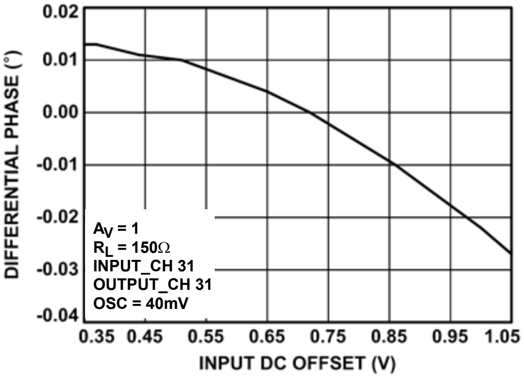


FIGURE 34. DIFFERENTIAL GAIN, $A_V = 1$

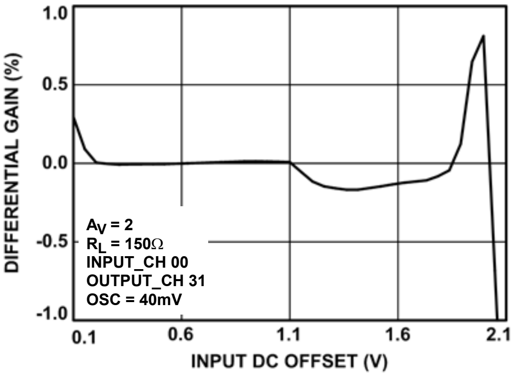


FIGURE 35. DIFFERENTIAL GAIN, $A_V = 2$

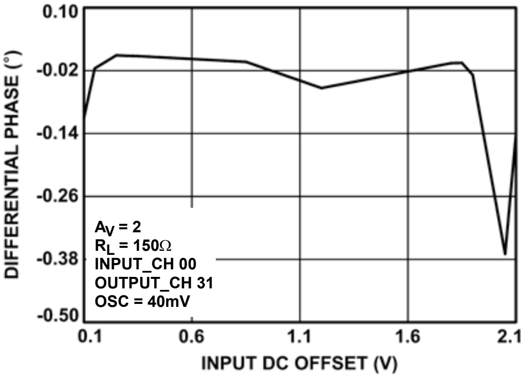


FIGURE 36. DIFFERENTIAL PHASE, $A_V = 2$

Typical Performance Curve (Continued)

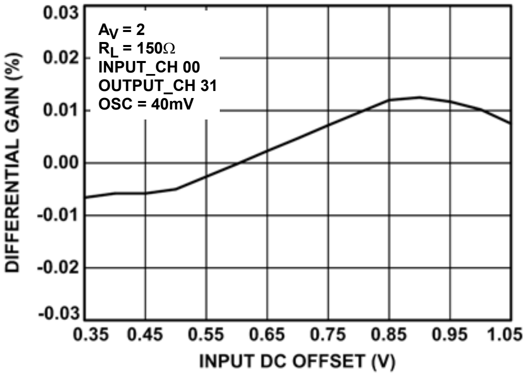


FIGURE 37. DIFFERENTIAL GAIN, $A_V = 2$

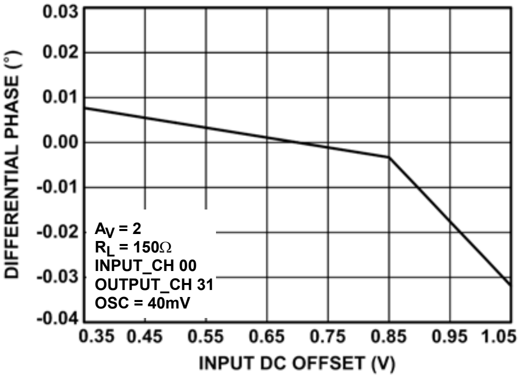


FIGURE 38. DIFFERENTIAL PHASE, $A_V = 2$

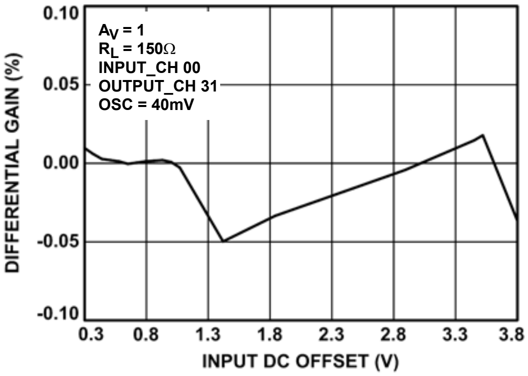


FIGURE 39. DIFFERENTIAL GAIN, $A_V = 1$

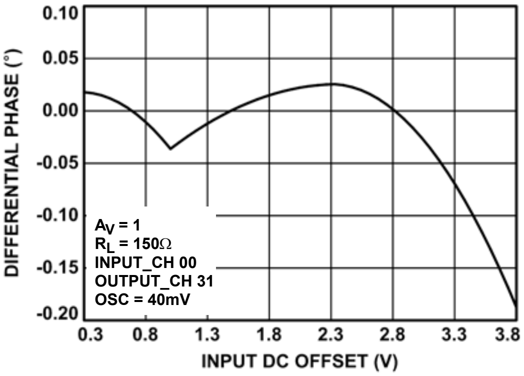


FIGURE 40. DIFFERENTIAL PHASE, $A_V = 1$

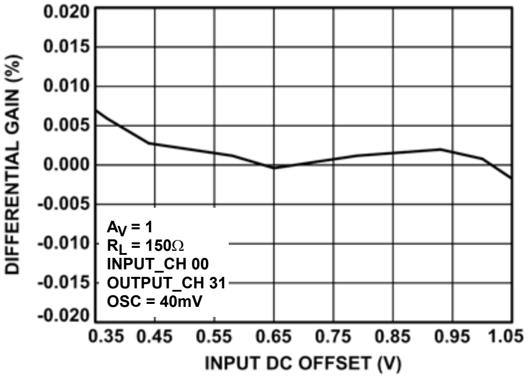


FIGURE 41. DIFFERENTIAL GAIN, $A_V = 1$

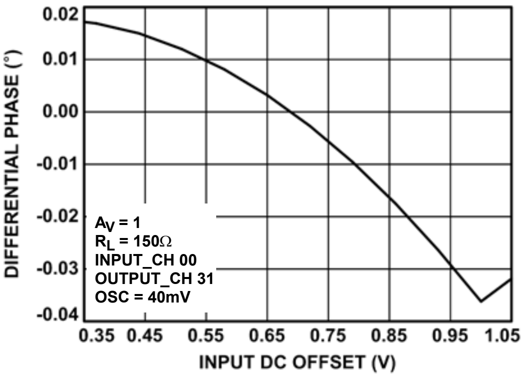


FIGURE 42. DIFFERENTIAL PHASE, $A_V = 1$

Typical Performance Curve (Continued)

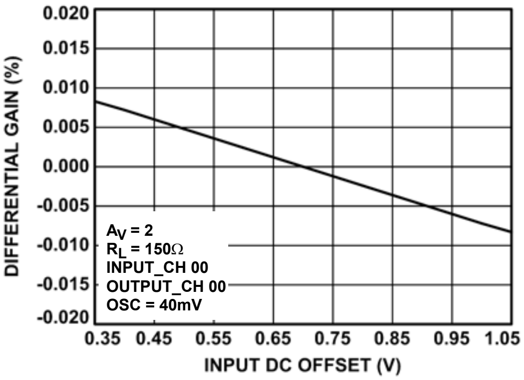


FIGURE 43. DIFFERENTIAL GAIN, OVERLAY, $A_V = 2$

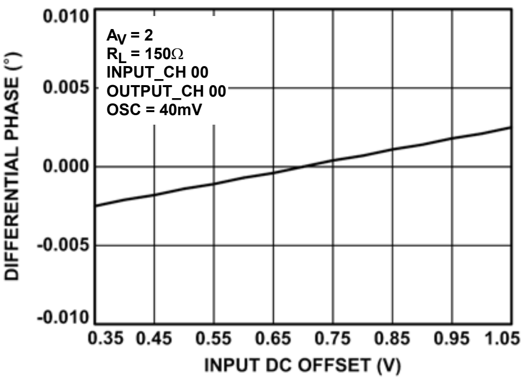


FIGURE 44. DIFFERENTIAL PHASE, OVERLAY, $A_V = 2$

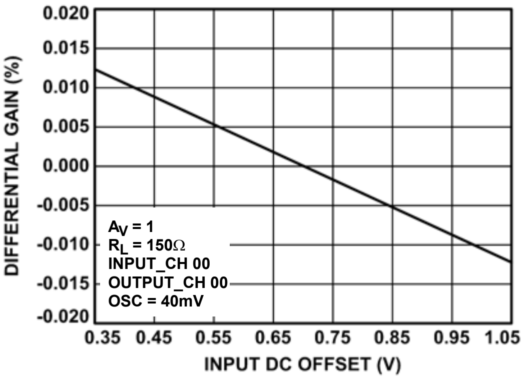


FIGURE 45. DIFFERENTIAL GAIN, OVERLAY, $A_V = 1$

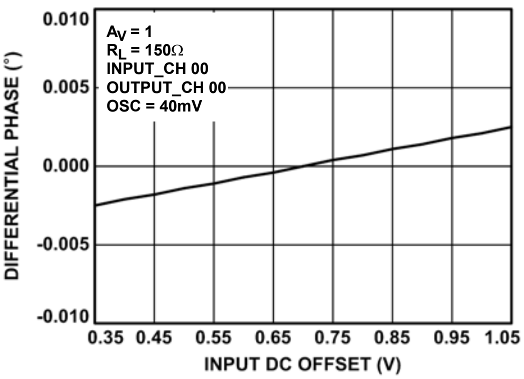


FIGURE 46. DIFFERENTIAL PHASE, OVERLAY, $A_V = 1$

3dB Bandwidth, MUX Mode, $A_V = 1$, $R_L = 100\Omega$ [MHz]

		INPUT CHANNELS																															
		0	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**	**17**	**18**	**19**	**20**	**21**	**22**	**23**	**24**	**25**	**26**	**27**	**28**	**29**	**30**	**31**
OUTPUT CHANNELS	**0**	262					270					268					235					236					235						236
	1		224																													214	
	2			217																											214		
	3				211																									203			
	4					277																							272				
	5	267					268										247											268					259
	6							288																			290						
	7								271																	278							
	8									269															271								
	9										277													275									
	10	273										274					256						272										267
	11												274									272											
	12													255							258												
	13														264					271													
	14															268			274														
	15	298	292	289	290	304	299	307	304	198	309	299	300	292	290	286	283	290	292	299	296	298	308	326	311	221	309	313	311	293	297	294	283
	16																278	286															
	17															268			276														
	18														265					277													
	19													255							264												
	20	281											282				265					288											283
	21											266											275										
	22										285													350									
	23									268															336								
	24								196																	216							
	25	264						271									247										277						272
	26						269																					285					
	27					267																							283				
	28				199																									281			
	29			206																											252		
	30		214																													252	
	31	238					230					238					220					280					287						274

3dB Bandwidth, MUX Mode, $A_V = 2$, $R_L = 100\Omega$ [MHz]

		INPUT CHANNELS																															
		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
OUTPUT CHANNELS	0	262					270					268					235					236					235						236
	1		224																													214	
	2			217																											214		
	3				211																									203			
	4					277																							272				
	5	267					268										247											268					259
	6							288																			290						
	7								271																	278							
	8									269															271								
	9										277													275									
	10	273										274					256						272										267
	11												274									272											
	12													255							258												
	13														264					271													
	14															268			274														
	15	298	292	289	290	304	299	307	304	198	309	299	300	292	290	286	283	290	292	299	296	298	308	326	311	221	309	313	311	293	297	294	283
	16																278	286															
	17															268			276														
	18														265					277													
	19													255							264												
	20	281											282				265					288											283
	21											266											275										
	22										285													350									
	23									268															336								
	24								196																	216							
	25	264						271									247										277						272
	26						269																					285					
	27					267																							283				
	28				199																									281			
	29			206																											252		
	30		214																													252	
	31	238					230					238					220					280					287						274

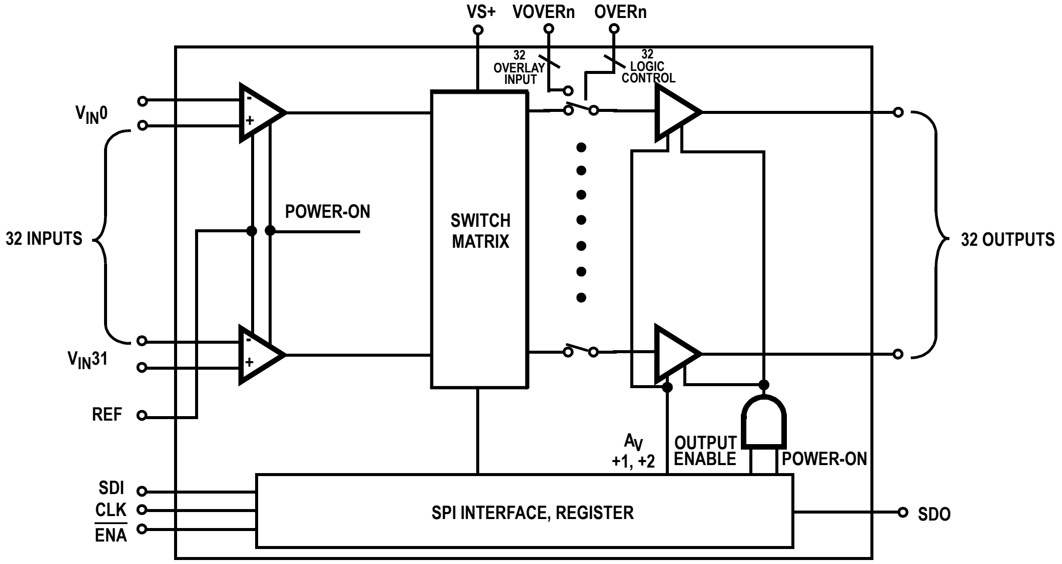
3dB Bandwidth, Broadcast Mode, $A_V = 1$, $R_L = 100\Omega$ [MHz]

		INPUT CHANNELS																															
		0	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**	**17**	**18**	**19**	**20**	**21**	**22**	**23**	**24**	**25**	**26**	**27**	**28**	**29**	**30**	**31**
OUTPUT CHANNELS	**0**	196	204	193	175	154	154	158	161	169	157	155	146	125	121	115	109	81	81	79	80	85	85	86	86	83	82	82	77	80	82	85	86
	1	185	189														104															85	87
	2	172		163													104														85		87
	3	161			138												99													81			87
	4	165				128											99												79				89
	5	160					126										97											82					89
	6	152						123									95										81						89
	7	141							119								91									84							89
	8	133								113							86								82								89
	9	133									113						90							85									90
	10	132										113					91						88										92
	11	130											107				90					90											93
	12	125												94			87				81												92
	13	125													91		88			84													95
	14	127														90	88		85														97
	15	125	129	124	118	109	109	110	112	113	110	107	106	95	93	91	89	88	88	88	88	95	94	96	97	93	92	89	86	91	93	95	98
	16	124															89	88															100
	17	119														85	85		86														100
	18	116													88		84			87													100
	19	113												89			82				88												100
	20	114											97				84					98											102
	21	112										99					82						98										103
	22	108									94						80							100									102
	23	107								96							78								100								104
	24	106							96								79									99							106
	25	107						96									80										99						110
	26	108					96										81											98					114
	27	107				97											81												99				123
	28	104			98												78													105			115
	29	104		102													80														106		119
	30	105	106														80															118	125
	31	107	110	108	103	98	98	98	99	101	99	97	95	87	86	84	81	113	112	112	114	126	126	128	129	124	118	114	111	120	122	129	131

3dB Bandwidth, Broadcast Mode, $A_V = 2$, $R_L = 100\Omega$ [MHz]

		INPUT CHANNELS																															
		0	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**	**17**	**18**	**19**	**20**	**21**	**22**	**23**	**24**	**25**	**26**	**27**	**28**	**29**	**30**	**31**
OUTPUT CHANNELS	**0**	270	277	268	247	213	216	227	244	258	223	208	196	147	142	132	123	85	85	85	86	91	91	92	93	90	88	86	85	89	90	92	94
	1	256	261														117															93	93
	2	240		223													112														88		92
	3	219			189												106													86			92
	4	233				158											108												83				95
	5	225					152										106											86					95
	6	204						146									105										88						95
	7	187							137								99									89							94
	8	172								128							92								85								94
	9	171									128						96							93									96
	10	170										126					97						94										98
	11	167											119				97					96											101
	12	152												103			93				89												99
	13	153													99		93			88													103
	14	155														96	94		89														105
	15	151	155	146	134	123	125	126	126	128	123	123	114	103	99	97	94	94	92	92	93	102	102	102	102	99	99	93	93	98	99	102	104
	16	146															93	94															109
	17	138														91	91		92														109
	18	133													94		90			93													109
	19	127												95			90				94												109
	20	129											106				89					106											113
	21	126										106					86						105										114
	22	119									102						84							107									112
	23	118								105							83								106								114
	24	116							103								83									107							117
	25	118						103									84										107						125
	26	120					103										84											108					135
	27	118				103											85												108				142
	28	113			106												82													113			133
	29	114		110													81														123		143
	30	115	116														82															138	155
	31	117	121	118	112	105	105	106	108	110	107	104	101	93	91	88	85	130	127	127	130	153	150	158	163	149	140	133	126	140	146	161	164

Block Diagram



General Description

The ISL59533 is a 32x32 integrated video crosspoint switch matrix with differential input and output buffers and On-Screen Display (OSD) insertion. This device operates from a single +5V supply. Any output can be switched to any of the 32 input video signal sources and OSD information through an internal, dedicated fast 2:1 mux located before the output buffer. Also, any one input can be broadcast to all 32 outputs.

Each output X is defined as:

Voutx = Avx*(INx-INBx+REF)

Where Avx = 1, or Avx = 2. Note that all REF's are common between channels and must be externally well buffered and/or bypassed.

The ISL59533 offers a -3dB signal bandwidth of 300MHz. The differential gain and phase at 0.01% and 0.03° respectively, along with 0.1dB flatness out to 35MHz. The switch matrix configuration and output buffer gain are programmed through an SPI/QSPI™-compatible, three-wire serial interface. The ISL59533 interface is set up to facilitate both fast updates and initialization. On power-up, all facilities are initialized in the disabled state to avoid output conflicts within the user system.

Digital Interface

The ISL59533 uses a simple 3-wire SPI compliant digital interface to program the outputs. The ISL59533 can support the clock rate up to 5MHz.

Serial Interface

The ISL59533 is programmed through a three-wire serial interface. The start and stop conditions are defined by the $\overline{\text{ENA}}$ signal. While the $\overline{\text{ENA}}$ is low, the data on the SDI (serial data input) pin is shifted into the 16-bit shift register on the positive edge of the SCLK (serial clock) signal. The LSB (bit 0) is loaded first and the MSB (bit 15) is loaded last (see Table 1). After the full 16-bit data has been loaded, the $\overline{\text{ENA}}$ is pulled high and the addressed output channel is updated. The SCLK is disabled internally when the $\overline{\text{ENA}}$ is high. The SCLK must be low before the $\overline{\text{ENA}}$ is pulled low.

The Serial Timing Diagram and parameters table show the timing requirements for three-wire signals.

Serial Timing Diagram

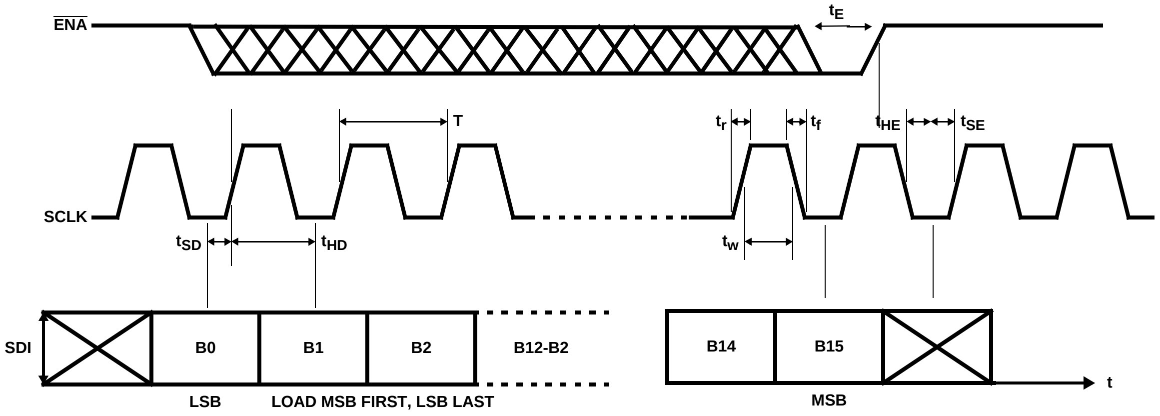


TABLE 1. SERIAL TIMING PARAMETERS

PARAMETER	RECOMMENDED OPERATING RANGE	DESCRIPTION
T	≥200ns	Clock Period
t_{HE}	≥20ns	$\overline{ENA}$ Hold Time
t_{SE}	≥20ns	$\overline{ENA}$ Setup Time
t_{HD}	≥20ns	Data Hold Time
t_{SD}	≥20ns	Data Setup Time
t_W	0.50 * T	Clock Pulse Width

Programming Model

The device has power-on reset that disables outputs, disables test mode, and turns off analog currents. To start up the device the control word is sent:

TABLE 2. CONTROL WORD FORMAT

B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
1	1	1	-	-	-	-	0	0	0	0	0	0	0	Power on	Common output enable

It is important to always program control bits 2-8 as zeros to avoid activating test modes designed for device manufacturing. The clamp bit activates the input clamp and bleed current sink and works only in the single-ended version.

To enable individual outputs, the output enable control word is sent. There are 32 enables to set; this is done with serial words controlling eight at a time. The output enable control word format is:

TABLE 3. OUTPUT ENABLE FORMAT

B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
0	0	1	-	-	-	N1	N0	O_{n+7}	O_{n+6}	O_{n+5}	O_{n+4}	O_{n+3}	O_{n+2}	O_{n+1}	O_n

The O_X bits represent output enables of eight individual registers. The N1N0 bits represent a two bit binary number which is used in setting $n = 2^{N1N0}$. For instance, to access the control bit of the 11th output enable, we send the word:

TABLE 4. OUTPUT ENABLE WORD OF 2ND GROUP OF OUTPUTS

B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
0	0	1	-	-	-	0	1	O_{15}	O_{14}	O_{13}	O_{12}	O_{11}	O_{10}	O_9	O_8

Individual output enables are ended with the control register’s common output enable bit and the power on bit.

Gain Setting

The gain of each output may be set to 1 or 2 using the gain set word. It is in the same format as the output enable control word:

TABLE 5. GAIN SET FORMAT

B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
0	1	0	-	-	-	N1	N0	G_{n+7}	G_{n+6}	G_{n+5}	G_{n+4}	G_{n+3}	G_{n+2}	G_{n+1}	G_n

Input to Output Selection

Individual outputs receive their input selection choice using the input/output control word. Its format is:

TABLE 6. INPUT/OUTPUT WORD

B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
0	0	0	I_4	I_3	I_2	I_1	I_0	-	-	-	O_4	O_3	O_2	O_1	O_0

For a given binarily selected output, as specified by the O's, an input channel is assigned by the binarily selected I's. Thirty-two transmissions of the input/output control words will be required to set up all outputs.

Broadcast Mode

The broadcast mode routs one input to all 32 outputs. It has a memory bit that remembers its state. The configuration of input/output assignments that existed before setting broadcast mode is kept in memory and when broadcast mode is disabled the previous configuration is restored. The broadcast control word format is:

TABLE 7. BROADCAST WORD

B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
0	1	1	I_4	I_3	I_2	I_1	I_0	-	-	-	-	-	-	-	EB

EB sets or resets the broadcast mode memory bit. The I's binarily select the input channel to be broadcast to all outputs.

Note: Going from broadcast mode to normal crosspoint mode can alter the input/output configuration. All input/output selections currently must be re-sent after a broadcast-to-non-broadcast transition.

Bandwidth Considerations

Wide frequency response (high bandwidth) in a video system means better video resolution. Four sets of frequency response curves are shown in Figure 47. Depending on the switch configurations, one can get between 250MHz to 350MHz bandwidth. A short discussion of the trade-offs follows—including matrix configuration, output buffer gain selection, channel selection, and loading.

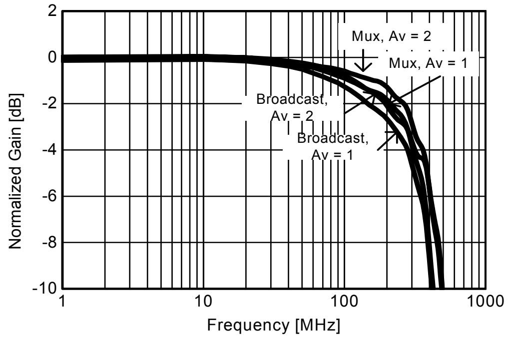


FIGURE 47. FREQUENCY RESPONSE FOR VARIOUS MODES

In multiplexer mode, the input only drives one output channel, while in broadcast mode the same input drives all 32 outputs. The parasitic capacitance of all 32 channels loads down the input and reduces bandwidth in broadcast mode. In addition, output buffer gain of +2 has higher bandwidth than gain of +1 due to internal device compensation. Therefore, the highest bandwidth set-up is multiplexer mode and output buffer gain of +2.

The relative location of the input and output channel also has significant impact on the device bandwidth. Again this is due to the layout of the device. When the input and output channels are further away, there are additional parasitics as a result of the distance and lower bandwidth results.

The bandwidth does not change significantly with resistive loading as shown in Figure 3 in the typical performance curves. However, it does change greatly with capacitance loading, Figure 4 in typical performance curves. This is most significant when laying out the PCB. If the PCB trace between the output of the crosspoint switch and the back termination resistor is not minimized, additional parasitic capacitance severely distorts the frequency response.

To emphasize how critical the PCB layout is to performance, let's compare the two boards presented in Figures 48 and 49. Figure 48 shows a larger engineering evaluation board where the termination resistor is far away from the device because of the use of a socket. The board in Figure 48 is a demoboard without the socket. The parasitic capacitance of the demoboard is about 2.7pF less.

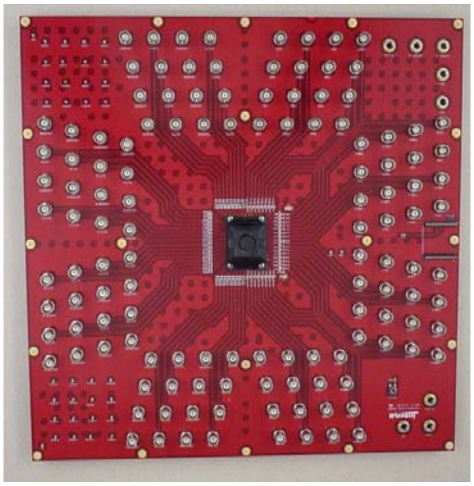


FIGURE 48. ENGINEERING EVALUATION BOARD

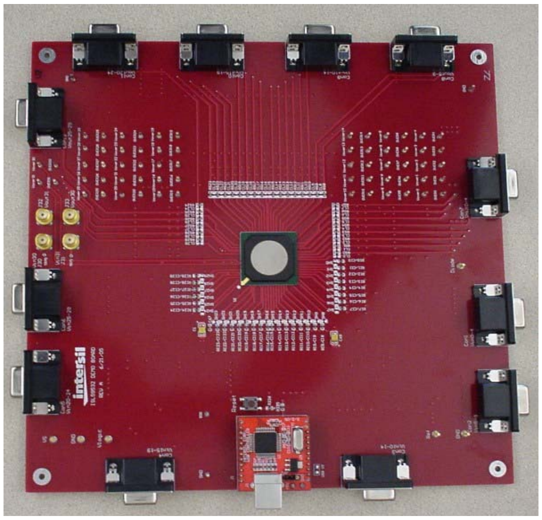


FIGURE 49. CUSTOMER DEMOBOARD

To prove that the parasitic capacitance is the largest contributor to the difference in bandwidth of the two boards, we added 2.7pF at the output of the demoboard. Figure 50 shows the similarity in frequency response of the engineering evaluation board alongside the demoboard piggybacked with 2.7pF.

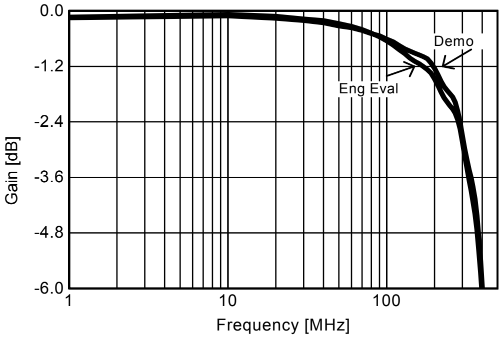


FIGURE 50. FREQUENCY RESPONSE - ENG EVAL BOARD vs DEMO

Linear Operating Region

In addition to bandwidth, one must also be very careful with operating the device at its linear operating region. Figure 51 shows differential gain curve. The ISL59533 is a single supply 5V device with its linear region is between 0.1 and 2V. The signal range is fine for most video signals whose nominal signal amplitude is 1V. Both inputs should be maintained at 0.3V or above for best operation. A DC restore circuit is required to put the video signal within the linear operating region of the crosspoint switch.

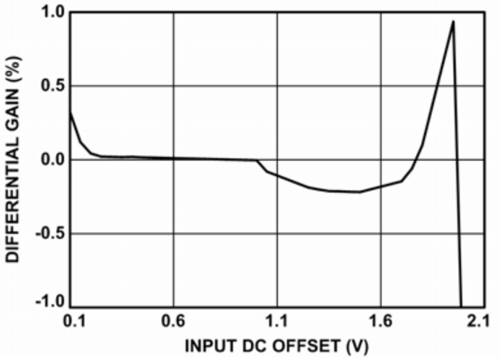


FIGURE 51. DIFFERENTIAL GAIN RESPONSE

Power Dissipation and Thermal Resistance

With a large number of switches, it is possible to exceed the 150°C absolute maximum junction temperature under certain load current conditions. Therefore, it is important to calculate the maximum junction temperature for an application to determine if load conditions or package types need to be modified to assure operation of the crosspoint switch in a safe operating area.

The maximum power dissipation allowed in a package is determined according to:

$$PD_{MAX} = \frac{T_{JMAX} - T_{AMAX}}{\Theta_{JA}}$$

Where:

- T_{JMAX} = Maximum junction temperature = 125°C
- T_{AMAX} = Maximum ambient temperature = 85°C
- θ_{JA} = Thermal resistance of the package

The maximum power dissipation actually produced by an IC is the total quiescent supply current times the total power supply voltage, plus the power in the IC due to the load, or:

$$PD_{MAX} = V_S \times I_{SMAX} + \sum_{i=1}^{n} (V_S - V_{OUTi}) \times \frac{V_{OUTi}}{R_{Li}}$$

Where:

- V_S = Supply voltage = 5V
- I_{SMAX} = Maximum quiescent supply current = 700mA
- V_{OUT} = Maximum output voltage of the application = 2V
- R_{LOAD} = Load resistance tied to ground = 150
- n = 1 to 32 channels

$$PD_{MAX} = V_S \times I_{SMAX} + \sum_{i=1}^{n} (V_S - V_{OUTi}) \times \frac{V_{OUTi}}{R_{Li}} = 4.8W$$

The reqired θ_{JA} to dissipate 4.8W is:

$$\Theta_{JA} = \frac{T_{JMAX} - T_{AMAX}}{PD_{MAX}} = 8.33(°C/W)$$

Table 8 shows θ_{JA} thermal resistance results with a Wakefield heatsink and without heatsink and various airflow. At the thermal resistance equation shows, the required thermal resistance depends on the maximum ambient temperature.

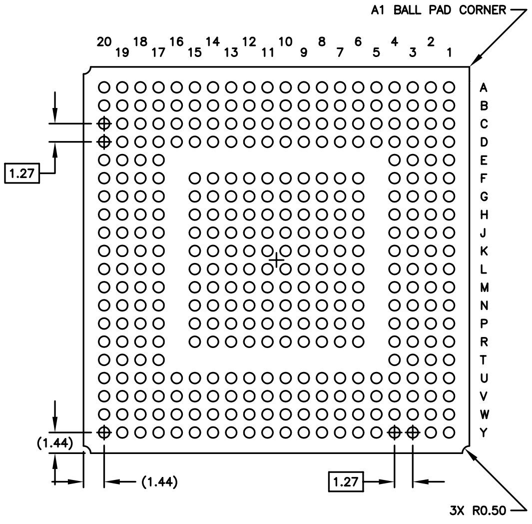
TABLE 8. θ_{JA} THERMAL RESISTANCE [°C/W]

Airflow [LFM]	0	250	500	750
No Heatsink	18	14.3	13.0	12.6
Wakefield 658-25AB	16.0	7.0	6.0	4.7

356 Ld HBGA Package

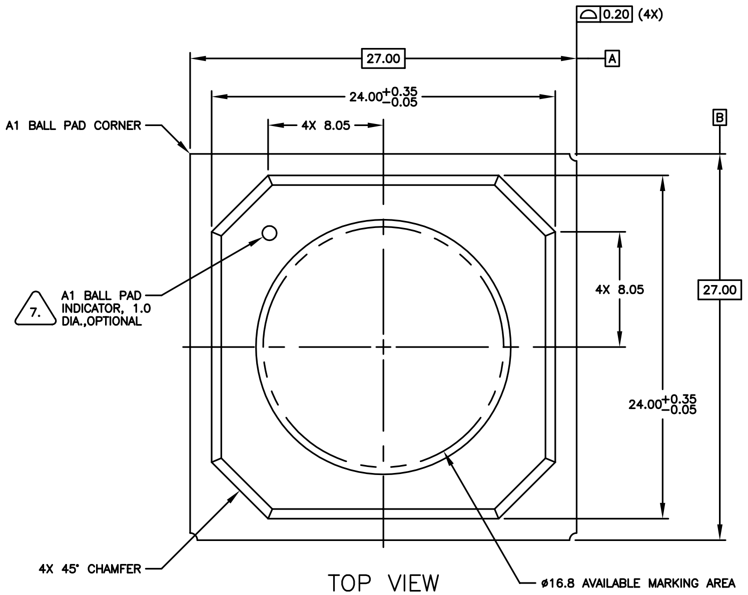
NOTES: UNLESS OTHERWISE SPECIFIED

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M−1994.
2. THE BASIC SOLDER BALL GRID PITCH IS 1.27mm.
3. THE MAXIMUM SOLDER BALL MATRIX SIZE IS 20 X 20.
4. THE MAXIMUM ALLOWABLE NUMBER OF SOLDER BALLS IS 400.
5. DIMENSION IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM C.
6. PRIMARY DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
7. A1 BALL PAD CORNER I.D. FOR PLATE MOLD: TO BE MARKED BY INK.
   AUTO MOLD: DIMPLE TO BE FORMED BY MOLD CAP.
8. REFERENCE SPECIFICATIONS:
   A. THIS DRAWING CONFORMS TO THE JEDEC REGISTERED OUTLINE MS−034/A VARIATION BAL−2.

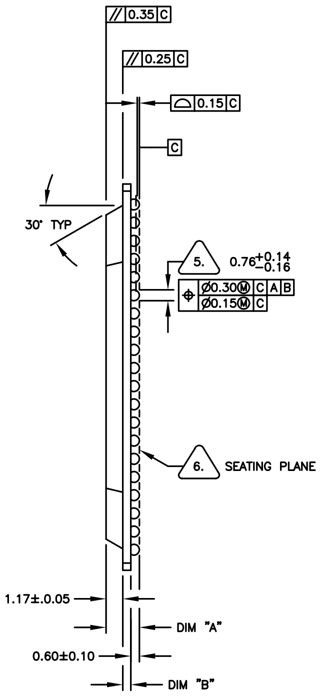


BOTTOM VIEW

356 SOLDER BALLS



TOP VIEW



SIDE VIEW

Drawing#: V356.27x27A
Rev: 0
Date: 2/28/06
Units: mm

PACKAGE OUTLINE DRAWING − 356 HPBGA
27 x 27 mm x 1.17 mm MOLD CAP
1.27 mm PITCH SUBSTRATE

NO. LAYERS	DIM "A"	DIM "B"	NOTES
4	2.38±0.21	0.61±0.06	STANDARD

HPBGA THICKNESS SCHEDULE