PROTEK DEVICES

PLC496

ULTRA LOW CAPACITANCE TVS ARRAY

APPLICATIONS

✔ Sensor & Control Circuits
✔ FireWire
✔ Ethernet - 10/100/1000 Base T
✔ Handheld Electronics
✔ RF Applications

IEC COMPATIBILITY (EN61000-4)

✔ 61000-4-2 (ESD): Air - 15kV, Contact - 8kV
✔ 61000-4-4 (EFT): 40A - 5/50ns
✔ 61000-4-5 (Surge): 24A, 8/20µs - Level 2(Line-Ground) & Level 3(Line-Line)

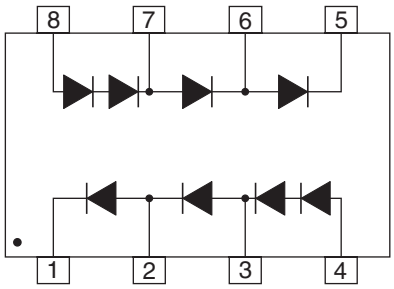
FEATURES

✔ 500 Watts Peak Pulse Power per Line (tp = 8/20µs)
✔ Bidirectional Configuration
✔ ESD Protection > 40 kilovolts
✔ Low Clamping Voltage < 5 Volts
✔ Ultra Low Capacitance: 1.25pF
✔ RoHS Compliant

MECHANICAL CHARACTERISTICS

✔ Molded JEDEC SO-8
✔ Weight 70 milligrams (Approximate)
✔ Available in Lead-Free Pure-Tin Plating(Annealed)
✔ Solder Reflow Temperature:
Pure-Tin - Sn, 100: 260-270°C
✔ Consult Factory for Leaded Device Availability
✔ Flammability Rating UL 94V-0
✔ 12mm Tape and Reel Per EIA Standard 481
✔ Marking: Logo, Marking Code, Date Code & Pin One Defined by Dot on Top of Package

PIN CONFIGURATION



DEVICE CHARACTERISTICS

MAXIMUM RATINGS @ 25°C Unless Otherwise Specified			
PARAMETER	**SYMBOL**	**VALUE**	**UNITS**
Peak Pulse Power (tp = 8/20µs) - See Figure 1	P_{PP}	500	Watts
Operating Temperature	T_L	-55 to 150	°C
Storage Temperature	T_{STG}	-55 to 150	°C

ELECTRICAL CHARACTERISTICS PER LINE @ 25°C Unless Otherwise Specified								
PART NUMBER	DEVICE MARKING CODE	RATED STAND-OFF VOLTAGE V_{WM} VOLTS	MINIMUM BREAKDOWN VOLTAGE (See Note 1) @1mA $V_{(BR)}$ VOLTS	MAXIMUM REVERSE LEAKAGE CURRENT (See Note 1) @V_{WM} I_D µA	MAXIMUM CLAMPING VOLTAGE (See Note 1) (See Fig. 2) @8/20µs V_C @ I_{PP}	WORKING INVERSE BLOCKING VOLTAGE (See Note 2) V_{WIB} VOLTS	INVERSE BLOCKING LEAKAGE CURRENT (See Note 2) @V_{WIB} I_R µA	MAXIMUM CAPACITANCE (See Note 3) @0V, 1MHz C pF
PLC496	VEC	1.0	2.5	20	12.5V @ 30A	75	1.0	1.25

Note 1: Apply positive voltage from pin 4 to 1 and pin 8 to 5.
Note 2: Apply positive voltage from pin 1 to 4 and pin 5 to 8.
Note 3: Capcitance from pin 1 to 4 < 1.25pF. Capacitance from pin 8 to 5 < 1.25pF.

FIGURE 1
PEAK PULSE POWER VS PULSE TIME

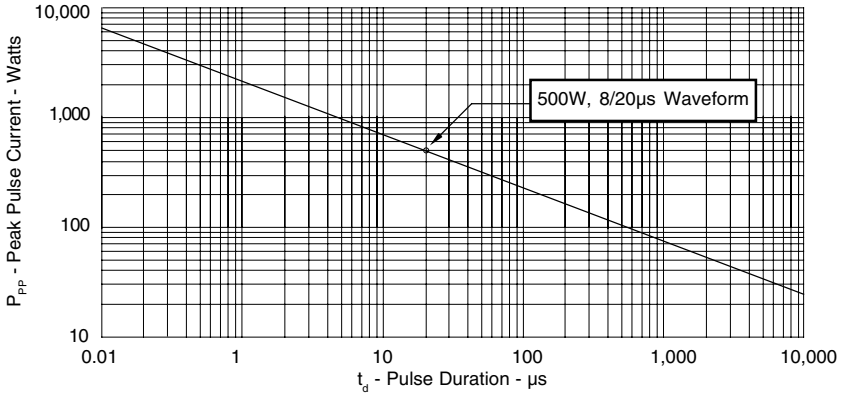
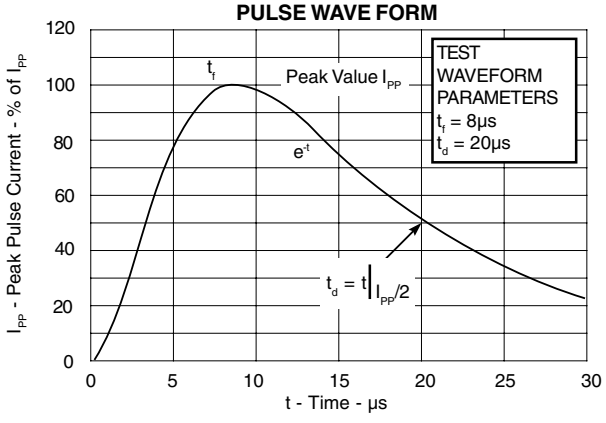


FIGURE 2
PULSE WAVE FORM



GRAPHS

FIGURE 3
POWER DERATING CURVE

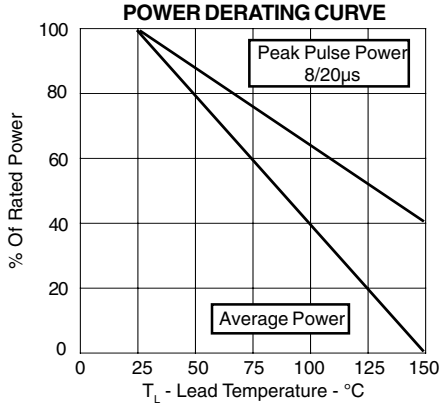
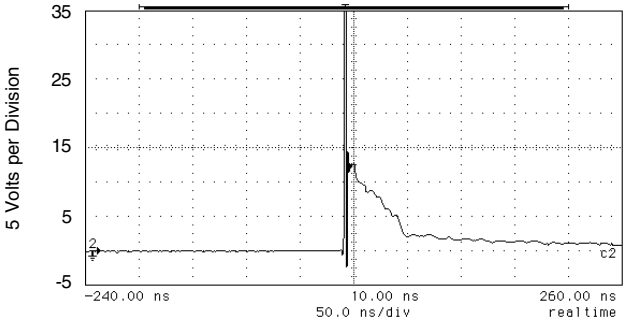


FIGURE 4
OVERSHOOT & CLAMPING VOLTAGE FOR PLC496



ESD Test Pulse: 25 kilovolt, 1/30ns (waveshape)

APPLICATION NOTE

The PLC496 is an ultra low capacitance, bidirectional array that is designed to protect I/O or high speed data lines from the damaging effects of ESD or EFT. This product has a surge capability of 500 Watts P_{PP} per line for an 8/20µs waveshape and offers ESD protection > 40kV.

DIFFERENTIAL-MODE CONFIGURATION (Figure 1)

The PLC496 is designed to protect one bidirectional line where the normal signal voltage is both positive and negative. Figure 1 shows a typical differential-mode line to line) I/O port protection circuit application.

Circuit connectivity is as follows:
✔ Pins 1, 4 5 and 8 are connected to the data lines
✔ Pins 2, 3, 7 and 6 are not connected.

COMMON-MODE CONFIGURATION (Figure 2)

The PLC496 can provide protection for sensor circuit applications. Figure 2, is a typical common-mode (line to ground) sensor circuit application.

Circuit connectivity is as follows:
✔ Pins 1 and 8 connected to the dataline
✔ Pins 4 and 5 connected to ground
✔ Pins 2, 3, 6, and 7 are not connected

CIRCUIT BOARD LAYOUT RECOMMENDATIONS

Circuit board layout is critical for Electromagnetic Compatibility (EMC) protection. The following guidelines are recommended:

✔ The protection device should be placed near the input terminals or connectors, the device will divert the transient current immediately before it can be coupled into the nearby traces.

✔ The path length between the TVS device and the protected line should be minimized.

✔ All conductive loops including power and ground loops should be minimized.

✔ The transient current return path to ground should be kept as short as possible to reduce parasitic inductance.

✔ Ground planes should be used whenever possible. For multilayer PCBs, use ground vias.

Figure 1. Typical Differential Mode I/O Port Protection

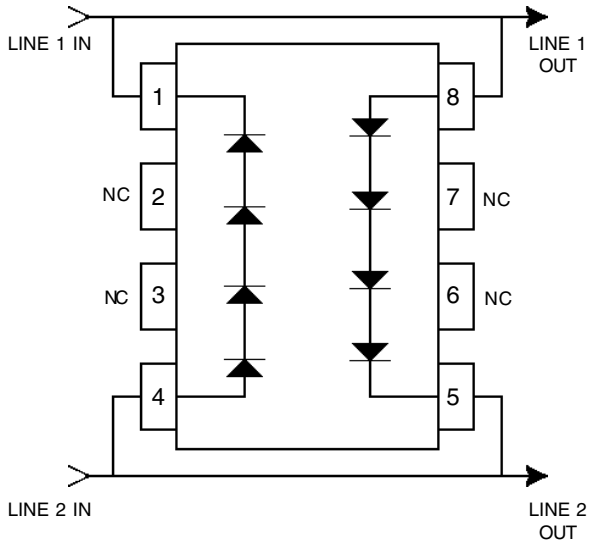
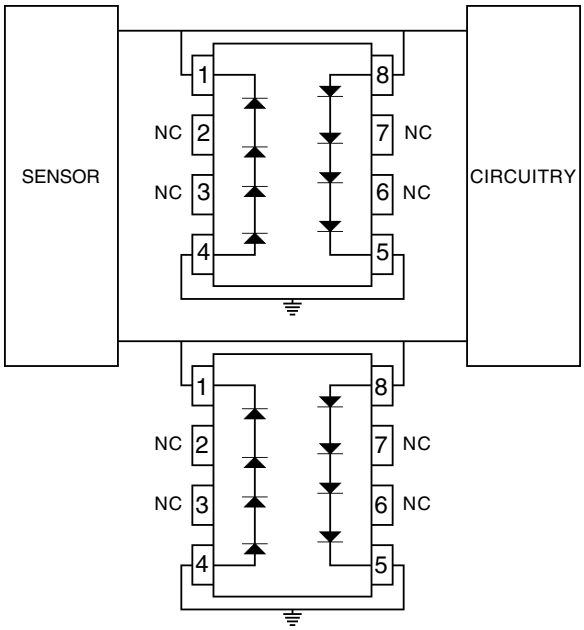
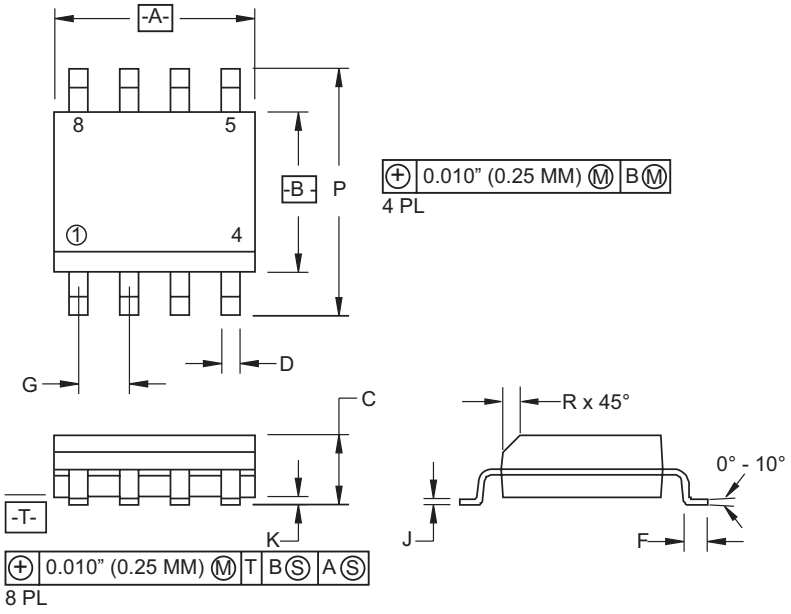


Figure 2. Typical Common Mode Sensor Protection Circuit

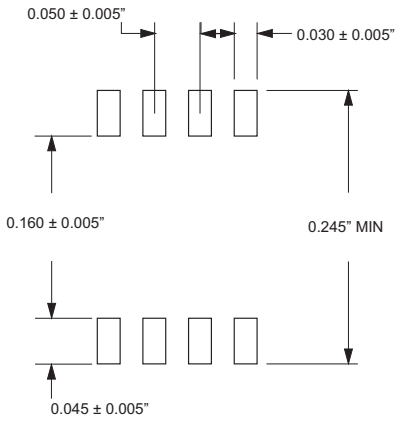


SO-8 PACKAGE OUTLINE & DIMENSIONS

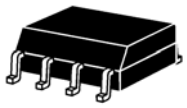
PACKAGE OUTLINE



MOUNTING PAD



SO-8



PACKAGE DIMENSIONS

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	4.80	5.00	0.189	0.196
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.250	0.016	0.049
G	1.27 BSC	1.27 BSC	0.05 BSC	0.05 BSC
J	0.18	0.25	0.007	0.009
K	0.10	0.25	0.004	0.008
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

NOTES

1. - T - = Seating Plane and Datum Surface.
2. Dimensions "A" and "B" are Datum.
3. Dimensions "A" and "B" do not include mold protrusion.
4. Maximum mold protrusion is 0.015" (0.380 mm) per side.
5. Dimensioning and tolerances per ANSI Y14.5M, 1982.
6. Dimensions are exclusive of mold flash and metal burrs.

TAPE & REEL/BULK ORDERING NOMENCLATURE

1. Surface mount product is taped and reeled in accordance with EIA-481.
2. Suffix-T7 = 7 Inch Reel - 1,000 pieces per 12mm tape, i.e. PLC496-T7..
3. Suffix-T13 = 13 Inch Reel - 2,500 pieces per 12mm tape, i.e., PLC496-T13.
4. Suffix - LF = Lead-Free, Pure-Tin Plating, i.e., PLC496-LF-T7.
5. No Suffix = Product Shipped in Tubes of 98 pcs per Tube.

Outline & Dimensions: Rev 1 - 11/01, 06009

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