Description

The SFC05-4 is a quad flip chip CSP TVS diode array. They are state-of-the-art devices that utilize solid-state silicon-avalanche technology for superior clamping performance and DC electrical characteristics. The SFC series TVS diodes are designed to protect sensitive semiconductor components from damage or latch-up due to electrostatic discharge (ESD) and other voltage induced transient events.

The SFC05-4 is a 6-bump, 0.5mm pitch flip chip array with a 3x2 bump grid. It measures 1.5 x 1.0 x 0.65mm. This small outline makes the SFC05-4 especially well suited for portable applications. CSP TVS devices are compatible with current pick and place equipment and assembly methods.

Each device will protect up to four data or I/O lines. The CSP design results in lower inductance, virtually eliminating voltage overshoot due to leads and interconnecting bond wires. They may be used to meet the ESD immunity requirements of IEC 61000-4-2, Level 4 (15kV air, 8kV contact discharge).

Features

- 300 Watts peak pulse power (tp = 8/20µs)
- Transient protection for data lines to
  IEC 61000-4-2 (ESD) 15kV (air), 8kV (contact)
  IEC 61000-4-4 (EFT) 40A (5/50ns)
  IEC 61000-4-5 (Lightning) 24A (8/20µs)
- Small chip scale package requires less board space
- Low profile (< 0.65mm)
- No need for underfill material
- Protects four I/O or data lines
- Low clamping voltage
- Working voltage: 5V
- Solid-state silicon-avalanche technology

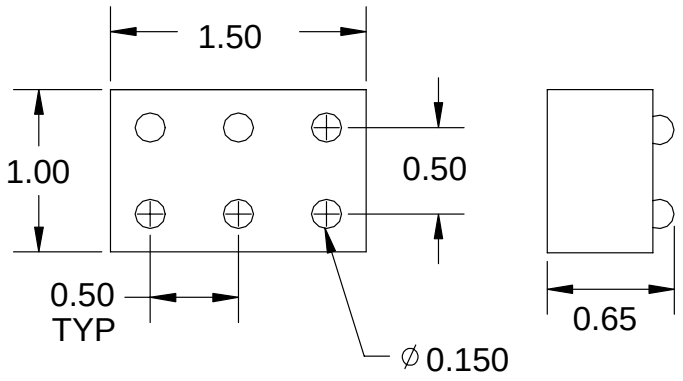
Mechanical Characteristics

- JEDEC MO-211, Variation BB, 0.50 mm Pitch Chip Scale Package (CSP)
- Marking : Marking Code
- Packaging : Tape and Reel

Applications

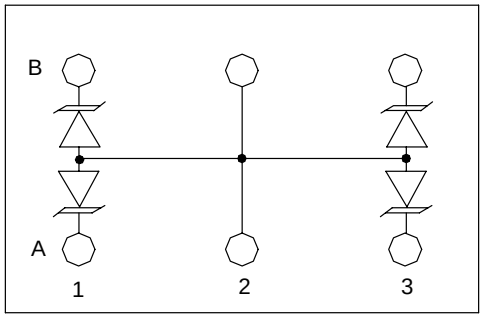
- Cell Phone Handsets and Accessories
- Personal Digital Assistants (PDA's)
- Notebook & Hand Held Computers
- Portable Instrumentation
- Pagers
- Smart Cards
- MP3 Players
- GPS

Device Dimensions



SFC05-4 Maximum Dimensions (mm)

Schematic & PIN Configuration



3 x 2 Grid CSP TVS (Bottom View)

Absolute Maximum Rating

Rating	Symbol	Value	Units
Peak Pulse Power (tp = 8/20µs)	P_{pk}	300	Watts
Peak Pulse Current (tp = 8/20µs)	I_{PP}	24	A
ESD per IEC 61000-4-2 (Air) ESD per IEC 61000-4-2 (Contact)	V_{ESD}	>25 >15	kV
Soldering Temperature	T_L	260 (10 seconds)	°C
Operating Temperature	T_J	-55 to +125	°C
Storage Temperature	T_{STG}	-55 to +150	°C

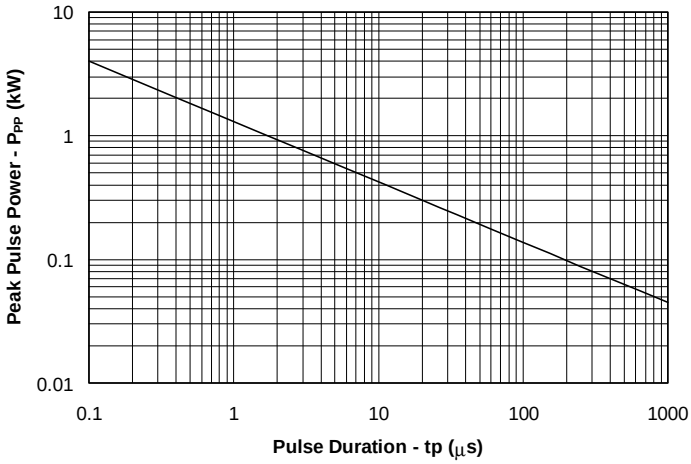
Electrical Characteristics

SFC05-4 for 5V Lines

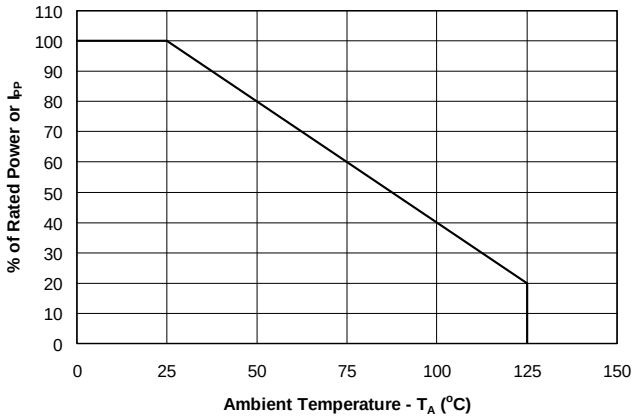
Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units
Reverse Stand-Off Voltage	V_{RWM}				5	V
Reverse Breakdown Voltage	V_{BR}	I_t = 1mA	6			V
Reverse Leakage Current	I_R	V_{RWM} = 5V, T=25°C			10	µA
Clamping Voltage	V_C	I_{PP} = 5A, tp = 8/20µs			9.5	V
Clamping Voltage	V_C	I_{PP} = 24A, tp = 8/20µs			11	V
Junction Capacitance	C_j	V_R = 0V, f = 1MHz			350	pF

Typical Characteristics

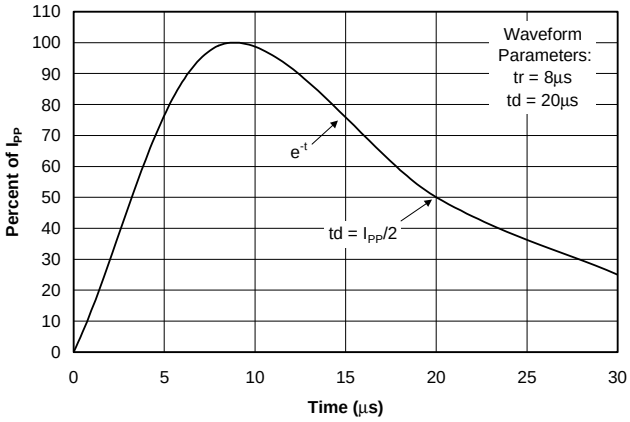
Non-Repetitive Peak Pulse Power vs. Pulse Time



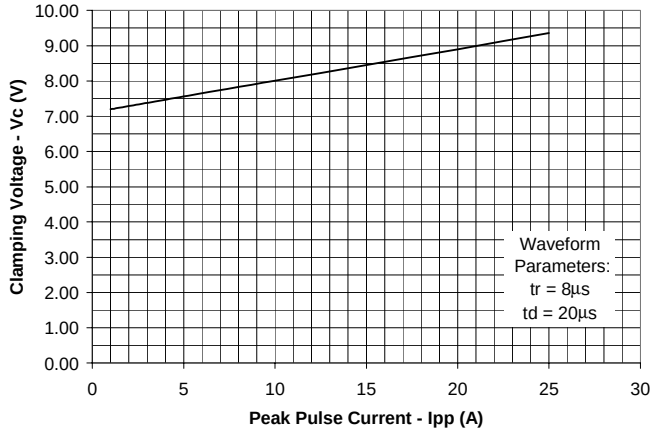
Power Derating Curve



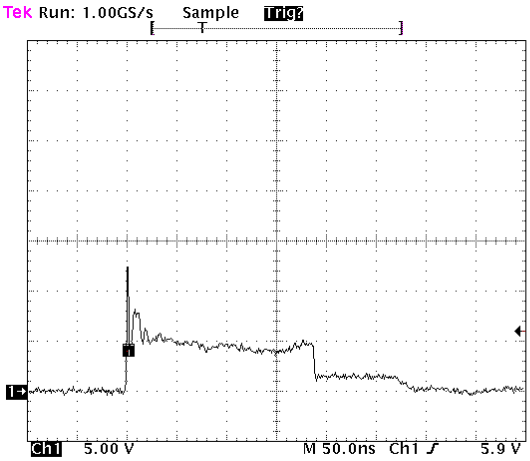
Pulse Waveform



Clamping Voltage vs. Peak Pulse Current



ESD Clamping (8kV Contact Discharge)



Applications Information

Device Connection Options

The SFC05-4 has solder bumps located in a 3 x 2 matrix layout on the active side of the device. The bumps are designated by the numbers 1 - 3 along the horizontal axis and letters A - B along the vertical axis. The lines to be protected are connected at bumps A1, B1, A3, and B3. Bumps A2 & B2 are connected to ground. All path lengths should be kept as short as possible to minimize the effects of parasitic inductance in the board traces.

Wafer Level CSP TVS

CSP TVS devices are wafer level chip scale packages. They eliminate external plastic packages and leads and thus result in a significant board space savings. Manufacturing costs are minimized since they do not require an intermediate level interconnect or interposer layer for reliable operation. They are compatible with current pick and place equipment further reducing manufacturing costs. Certain precautions and design considerations have to be observed however for maximum solder joint reliability. These include solder pad definition, board finish, and assembly parameters.

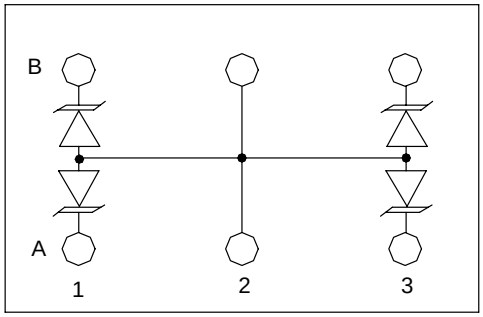
Printed Circuit Board Mounting

Non-solder mask defined (NSMD) land patterns are recommended for mounting the SFC05-4. Solder mask defined (SMD) pads produce stress points near the solder mask on the PCB side that can result in solder joint cracking when exposed to extreme fatigue conditions. The recommended pad size is 0.200 ± 10 mm with a solder mask opening of 0.350 ± 0.025 mm.

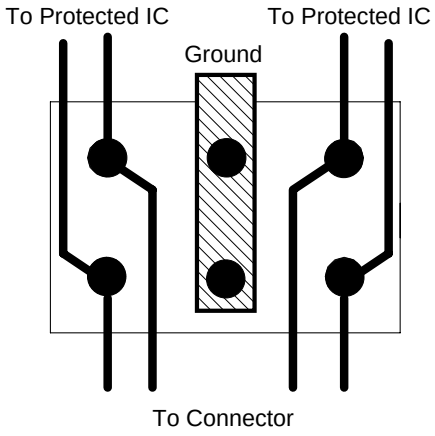
Grid Courtyard

The recommended grid placement courtyard is 1.3 x 1.8 mm. The grid courtyard is intended to encompass the land pattern and the component body that is centered in the land pattern. When placing parts on a PCB, the highest recommended density is when one courtyard touches another.

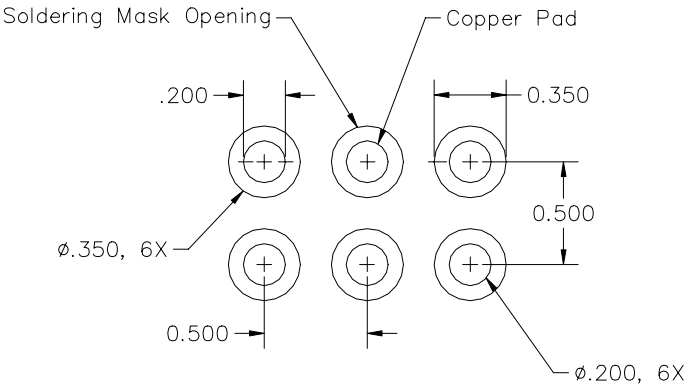
Device Schematic & Pin Configuration



Layout Example



NSMD Package Footprint



Applications Information *(Continued)*

Printed Circuit Board Finish

A uniform board finish is critical for good assembly yield. Two finishes that provide uniform surface coatings are immersion nickel gold and organic surface protectant (OSP). A non-uniform finish such as hot air solder leveling (HASL) can lead to mounting problems and should be avoided.

Stencil Design

A properly designed stencil is key to achieving adequate solder volume without compromising assembly yields. A 0.100mm thick, laser cut, electro-polished stencil with 0.275mm square apertures and rounded corners is recommended.

Reflow Profile

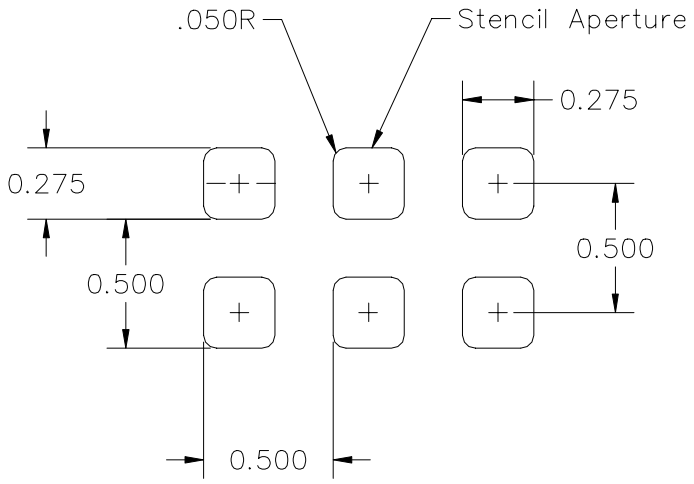
The flip chip TVS can be assembled using standard SMT reflow processes. As with any component, thermal profiles at specific board locations can vary & must be determined by the manufacturer. The flip chip TVS peak reflow temperature is 230 ± 10 °C, but the device can withstand up to 260 °C peak reflow temperature. Time above eutectic temperature (183 °C) should be 50 ± 10 seconds. During reflow, the component self-aligns itself on the pad.

Circuit Board Layout Recommendations for Suppression of ESD

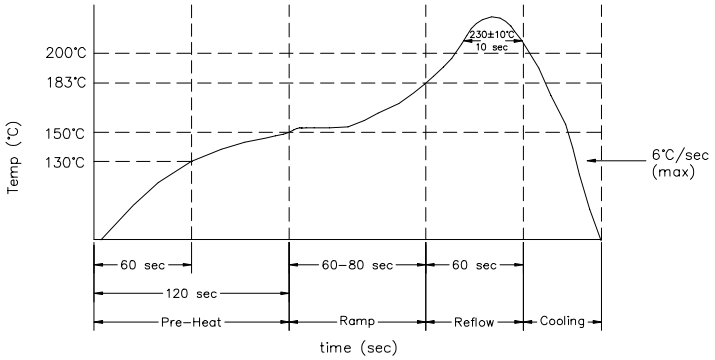
Good circuit board layout is critical for the suppression of ESD induced transients. The following guidelines are recommended:

- Place the TVS near the input terminals or connectors to restrict transient coupling.
- Minimize the path length between the TVS and the protected line.
- Minimize all conductive loops including power and ground loops.
- The ESD transient return path to ground should be kept as short as possible.
- Never run critical signals near board edges.
- Use ground planes whenever possible.

Stencil Design



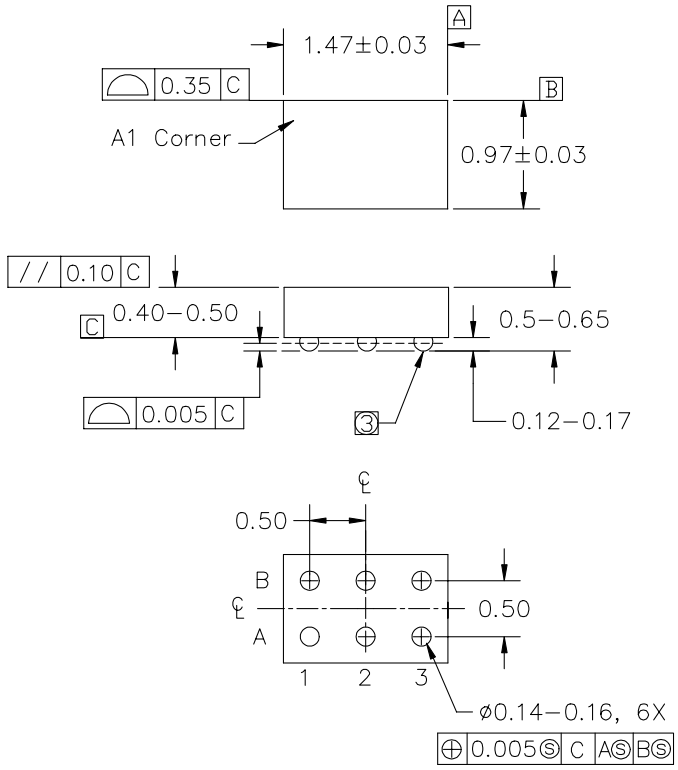
Reflow Profile



Typical solder reflow profile for OSP finish FR-4 bond.

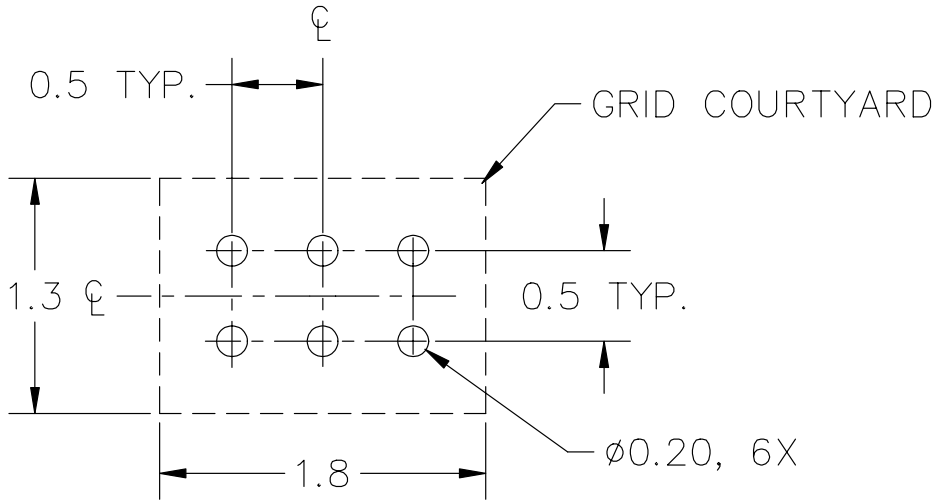
Pre-heat to 150°C	120 sec max
Time to eutectic (183°C)	60-80 sec
Time above eutectic	50±10 sec
Peak reflow temp	230±10°C
Time w/in 10°C of peak	10 seconds
Ramp down rate	6°C/sec max

Outline Drawing - SFC05-4



1. Dimensions in millimeters.
2. Reference Jedec Registration MO–211, Variation BB.
3. 63Sn/Pb Eutectic Bump

Land Pattern - SFC05-4



1. Dimensions in millimeters.

Marking Codes

Part Number	Marking Code
SFC05-4	F45U

Ordering Information

Part Number	Working Voltage	Qty per Reel	Reel Size
SFC05-4.TM	5V	6,000	7 Inch

Contact Information

Semtech Corporation
Protection Products Division
652 Mitchell Rd., Newbury Park, CA 91320
Phone: (805)498-2111 FAX (805)498-3804