December 1998

8 - Bit Micro-controller

with 64KB flash embedded

Product List

SM2964C16, 16 MHz 64KB internal flash MCU
SM2964C25, 25 MHz 64KB internal flash MCU
SM2964C40, 40 MHz 64KB internal flash MCU

Description

The SM2964 series product is an 8 - bit single chip micro controller with 64KB flash embedded.It provides hardware features and a powerful instruction set, necessary to make it a versatile and cost effective controller for those applications demand up to 32 I/O pins or need up to 64 K byte memory either for program or for data or mixed.
To program the flash block, a commercial programmer is capable to do it.

Ordering Information

yyww
SM2964ihhk

yy: year, ww:week
v: version identifier { , A, B, ...}
i: process identifier {C}
hh: working clock in MHz {16, 25, 40}
k: package type postfix {as below table}

Postfix	Package	Pin/Pad Configuration	Dimension	Logo Size at Top Marking
P	40L PDIP	page 2	page 11	5.0 x 4.2 mm
J	44L PLCC	page 2	page 12	4.5 x 3.8 mm
Q	44L PQFP	page 2	-	2.8 x 2.4 mm
U	44L LQFP	page 2	-	2.8 x 2.4 mm

Features

- Working voltage:4.5V through 5.5V
- General 8051 family compatible
- 12 clocks per machine cycle
- 64K byte internal flash memory
- 256 byte data RAM
- Three 16 bit Timers/Counters
- Four 8-bit I/O ports
- Full duplex serial channel
- Bit operation instructions
- Page free jumps
- 8-bit Unsigned Division
- 8-bit Unsigned Multiply
- BCD arithmetic
- Direct Addressing
- Indirect Addressing
- Nested Interrupt
- Two priority level interrupt
- A serial I/O port
- Power save modes:
  Idle mode and Power down mode
- Code protection function

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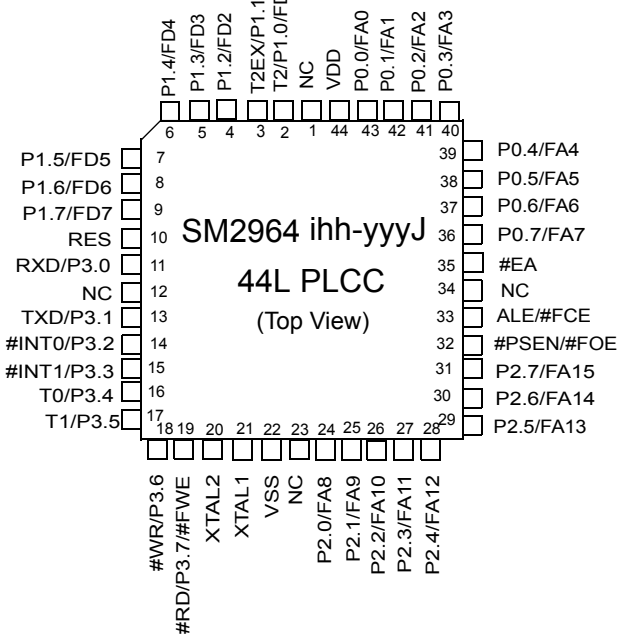
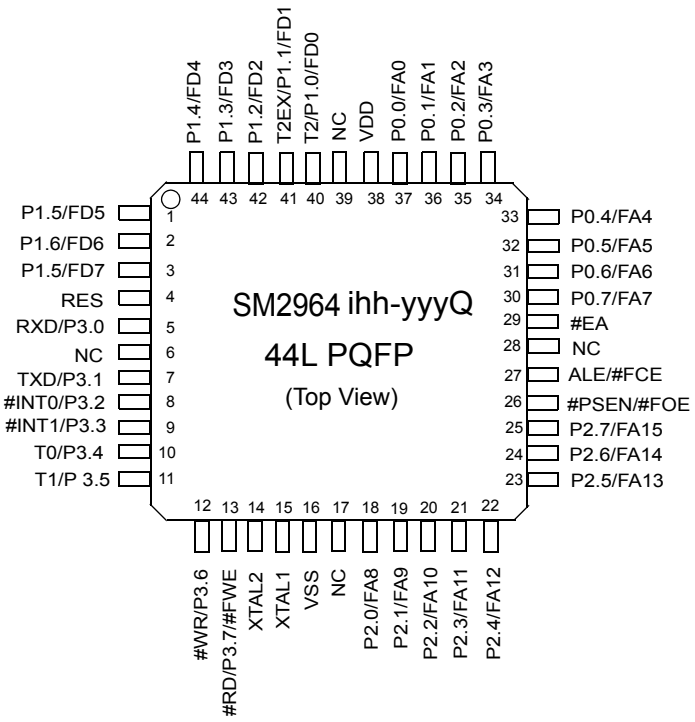
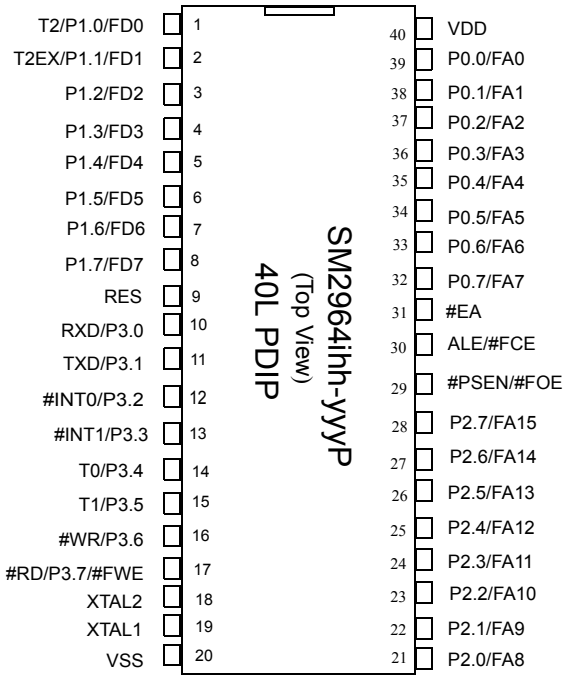
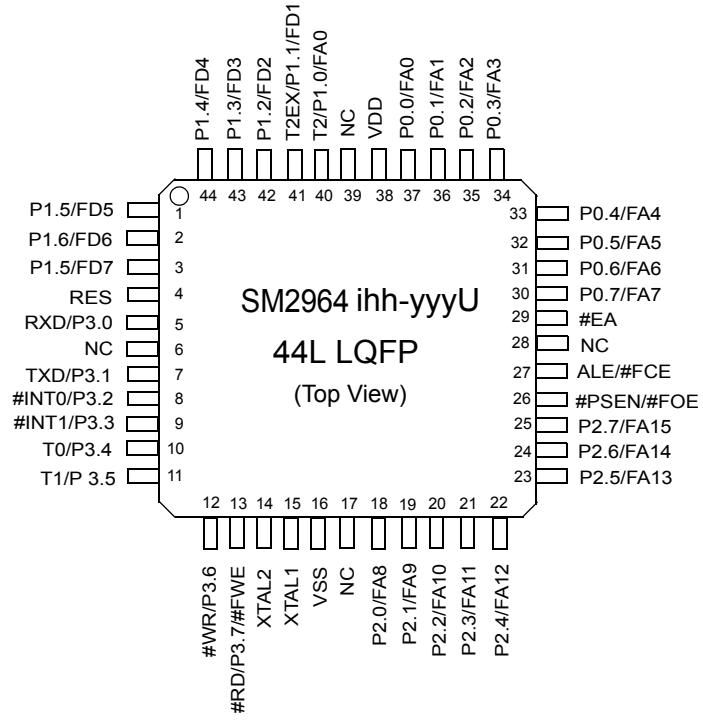
Pin Configurations

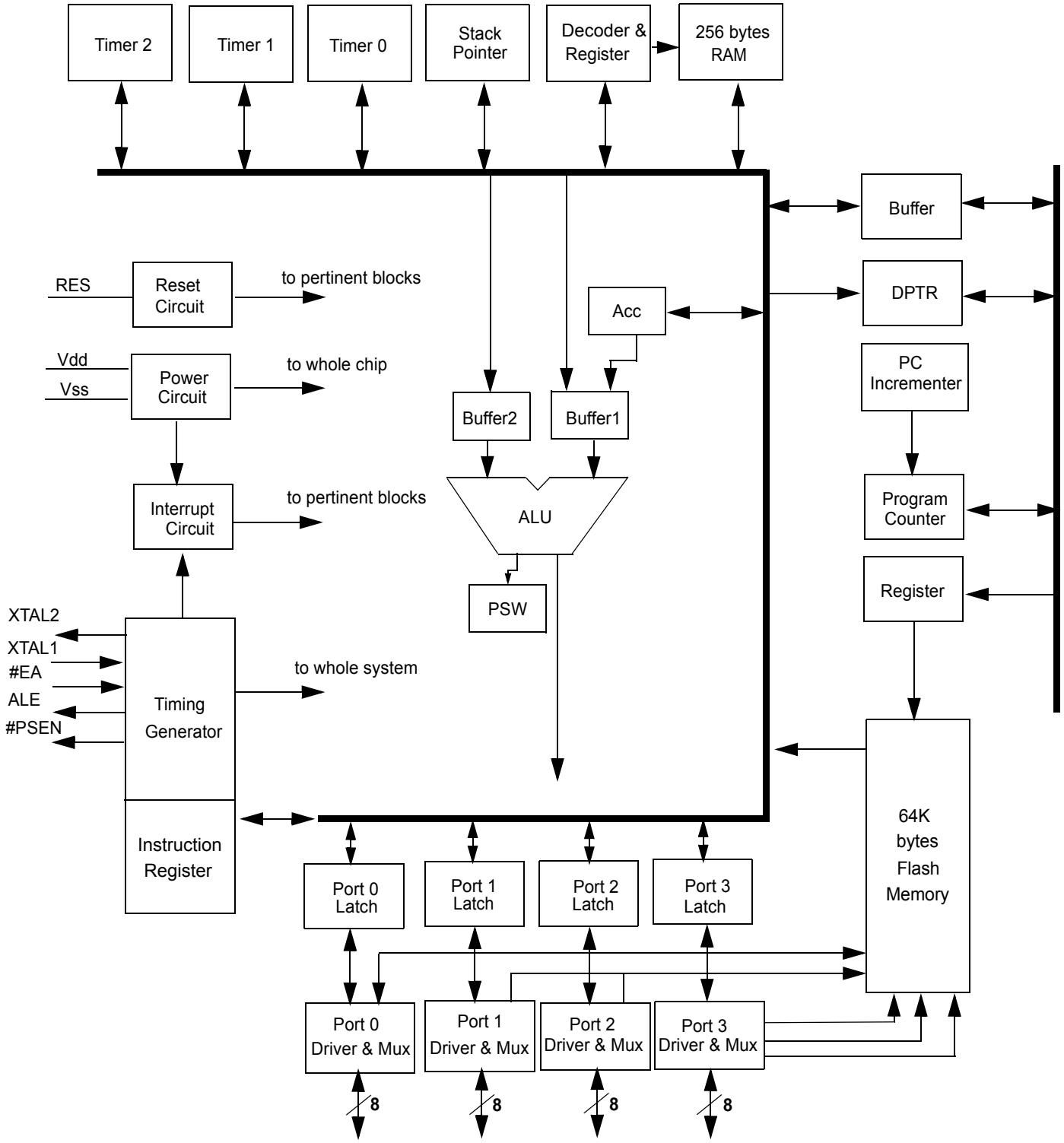








Block Diagram



Pin Descriptions

40L PDIP Pin#	44L LQFP Pin#	44L PQFP Pin#	44L PLCC Pin#	Symbol	Active	I/O	Names
1	40	40	2	T2/P1.0/FD0		i/o	bit 0 of port 1 & timer 2 & bit 0 of flash block address
2	41	41	3	T2EX/P1.1/FD1		i/o	bit 1 of port 1 & timer control & bit 1 of flash block address
3	42	42	4	P1.2/FD2		i/o	bit 2 of port 1 & bit 2 of flash/ext. memory address
4	43	43	5	P1.3/FD3		i/o	bit 3 of port 1 & bit 3 of flash/ext. memory address
5	44	44	6	P1.4/FD4		i/o	bit 4 of port 1 & bit 4 of flash/ext. memory address
6	1	1	7	P1.5/FD5		i/o	bit 5 of port 1 & bit 5 of flash/ext. memory address
7	2	2	8	P1.6/FD6		i/o	bit 6 of port 1 & bit 6 of flash/ext. memory address
8	3	3	9	P1.7/FD7		i/o	bit 7 of port 1 & bit 7 of flash/ext. memory address
9	4	4	10	RES	H	i	Reset
10	5	5	11	RXD/P3.0		i/o	bit 0 of port 3 & Receive data & flash block enable
11	7	7	13	TXD/P3.1		i/o	bit 1 of port 3 & Transmit data
12	8	8	14	#INT0/P3.2	L/ -	i/o	bit 2 of port 3 & low true interrupt 0
13	9	9	15	#INT1/P3.3	L/ -	i/o	bit 3 of port 3 & low true interrupt 1
14	10	10	16	T0/P3.4		i/o	bit 4 of port 3 & Timer 0
15	11	11	17	T1/P3.5		i/o	bit 5 of port 3 & Timer 1
16	12	12	18	#WR/P3.6	L/ -	i/o	bit 6 of port 3 & o/p enable to flash block (low enable)
17	13	13	19	#RD/P3.7/#FWE	L/ - /L	i/o	bit 7 of port 3 & write enable to flash block (low enable)
18	14	14	20	XTAL2		o	Crystal out
19	15	15	21	XTAL1		i	Crystal in
20	16	16	22	VSS			Sink Voltage, Ground
21	18	18	24	P2.0/FA8		i/o	bit 0 of port 2 & bit 8 of flash block address
22	19	19	25	P2.1/FA9		i/o	bit 1 of port 2 & bit 9 of flash block address
23	20	20	26	P2.2/FA10		i/o	bit 2 of port 2 & bit 10 of flash block address
24	21	21	27	P2.3/FA11		i/o	bit 3 of port 2 & bit 11 of flash block address
25	22	22	28	P2.4/FA12		i/o	bit 4 of port 2 & bit 12 of flash block address
26	23	23	29	P2.5/FA13		i/o	bit 5 of port 2 & bit 13 of flash block address
27	24	24	30	P2.6/FA14		i/o	bit 6 of port 2 & bit 14 of flash block address
28	25	25	31	P2.7/FA15	L/L	i/o	bit 7 of port 2 & bit 15 of flash block address
29	26	26	32	#PSEN/#FOE	- /L	o/i	program storage enable
30	27	27	33	ALE/#FCE	L	o/i	address latch enable
31	29	29	35	#EA		i	external access
32	30	30	36	P0.7/FA7		i/o	bit 7 of port 0 & data bit 7 of flash block
33	31	31	37	P0.6/FA6		i/o	bit 6 of port 0 & data bit 6 of flash block
34	32	32	38	P0.5/FA5		i/o	bit 5 of port 0 & data bit 5 of flash block
35	33	33	39	P0.4/FA4		i/o	bit 4 of port 0 & data bit 4 of flash block
36	34	34	40	P0.3/FA3		i/o	bit 3 of port 0 & data bit 3 of flash block
37	35	35	41	P0.2/FA2		i/o	bit 2 of port 0 & data bit 2 of flash block
38	36	36	42	P0.1/FA1		i/o	bit 1 of port 0 & data bit 1 of flash block
39	37	37	43	P0.0/FA0		i/o	bit 0 of port 0 & data bit 0 of flash block
40	38	38	44	VDD			Drive Voltage, +5 Vcc

Operating Conditions

Symbol	Description	Min.	Typ.	Max.	Unit.	Remarks
TA	Ambient temperature under bias	0	25	70	degree C	
VCC5	Supply voltage	4.5	5.0	5.5	V	SM2964C
Fosc 16	Oscillator Frequency	3.0	16	16	MHz	SM2964C16
Fosc 25		16	25	25	MHz	SM2964C25
Fosc 40		25	40	40	MHz	SM2964C40

AC Characteristics

(16/25/40 MHZ, operating conditions; CL for Port 0, ALE and PSEN Outputs=150uF; CL for all Other Output=80pF)

Symbol	Parameter	Valid Cycle	f osc 16			Variable f osc			Unit	Remarks
			Min.	Typ.	Max	Min.	Typ.	Max		
T LHLL	ALE pulse width	RD/WRT	115			2xT - 10			nS	
T AVLL	Address Valid to ALE low	RD/WRT	43			T - 20			nS	
T LLAX	Address Hold after ALE low	RD/WRT	53			T - 10			nS	
T LLIV	ALE low to Valid Instruction In	RD			240			4xT - 10	nS	
T LLPL	ALE low to #PSEN low	RD	53			T - 10			nS	
T PLPH	#PSEN pulse width	RD	173			3xT - 15			nS	
T PLIV	#PSEN low to Valid Instruction In	RD			177			3xT - 10	nS	
T PXIX	Instruction Hold after #PSEN	RD	0			0			nS	
T PXIZ	Instruction Float after #PSEN	RD			87			T + 25	nS	
T AVIV	Address to Valid Instruction In	RD			292			5xT - 20	nS	
T PLAZ	#PSEN low to Address Float	RD			10			10	nS	
T RLRH	#RD pulse width	RD	365			6xT - 10			nS	
T WLWH	#WR pulse width	WRT	365			6xT - 10			nS	
T RLDV	#RD low to Valid Data In	RD			302			5xT - 10	nS	
T RHDX	Data Hold after #RD	RD	0			0			nS	
T RHDZ	Data Float after #RD	RD			145			2xT + 20	nS	
T LLDV	ALE low to Valid Data In	RD			590			8xT - 10	nS	
T AVDV	Address to Valid Data In	RD			542			9xT - 20	nS	
T LLYL	ALE low to #WR High or #RD low	RD/WRT	178		197	3xT - 10		3xT + 10	nS	
T AVYL	Address Valid to #WR or #RD low	RD/WRT	230			4xT - 20			nS	
T QVWH	Data Valid to #WR High	WRT	403			7xT - 35			nS	
T QVWX	Data Valid to #WR transition	WRT	38			T - 25			nS	
T WHQX	Data hold after #WR	WRT	73			T + 10			nS	
T RLAZ	#RD low to Address Float	RD						5	nS	
T YALH	#WR or #RD high to ALE high	RD/WRT	53		72	T -10		T + 10	nS	
T CHCL	clock fall time								nS	
T CLCX	clock low time								nS	
T CLCH	clock rise time								nS	
T CHCX	clock high time								nS	
T , TCLCL	clock period			63			1/fosc		nS	

DC Characteristics

(12MHz, typical operating conditions, valid for SM2964C series)

Symbol	Parameter	Valid	Min.	Typ.	Max	Unit	Test Conditions
VILX	Input low voltage	XTAL1	-0.5		20%Vcc-0.1	V	
		#EA	0		20%Vcc-0.3	V	
VILR	"	RES	-0.5		20%Vcc-0.1	V	
VIHX	Input High Voltage	XTAL1	70% Vcc		Vcc+0.5	V	
		#EA	20%Vcc+0.9		Vcc+0.5	V	
VIHR	"	RES	70%Vcc		Vcc+0.5	V	
	Output Low Voltage	ALE, #PSEN			450	mV	IOL=3.2mA
VOL0	"	ports 0,3			450	mV	IOL=3.2mA
VOL1	"	ports 1,2			350	mV	IOL=1.6mA
	Output High Voltage	ALE, #PSEN	2.4			V	IOH= -60uA
	"		90%Vcc			V	IOH= -10uA
VOH0	"	port 0	2.4			V	IOH= -800uA
	"		90%Vcc			V	IOH= -80uA
VOH1	"	port 1,3	2.4			V	IOH= -60uA
	"		90%Vcc			V	IOH= -10uA
VOH2	"	port 2	2.4			V	IOH= -60uA
	"		90%Vcc			V	IOH= -10uA
IOL0	Output Low Current	ports 0,3				mA	VOL=0.45V,note1
IIL	Logical 0 Input Current	ports 1,2,3			50	uA	Vin=0.45V
IIH	Logical 1 Input Current	port 0			1.5	uA	Vin=5.0V
ITL	Logic Transition Current	port 1,2,3			650	uA	Vin=2.0V
ILI	Input Leakage Current	port 0			10	uA	0.45V<Vin<Vcc
R RES	Reset Pull-down Resistance	RES	50		150	Kohm	
R X	Crystal feedback Resistance	XTAL1,2	50		330	Kohm	
CIO	Pin Capacitance				10	pF	Freq=1MHZ,Ta=25° C
ICC	Power Supply Current	Vdd			20	mA	Active mode, 12MHZ
		Vdd			6.5	mA	Idle mode, 12MHZ
		Vdd			150	uA	Power down mode
VIL1	Input Low Voltage	port 0,1,2,3,#EA			0.5	V	Vcc= 5V
VIL2	"	RST			0.4	V	"
VIL3	"	XTAL1			0.4	V	"
VIH1	Input Low Voltage	port 0,1,2,3,#EA	1.3			V	"
VIH2	"	RST	3.0			V	"
VIH3	"	XTAL1	3.0			V	"

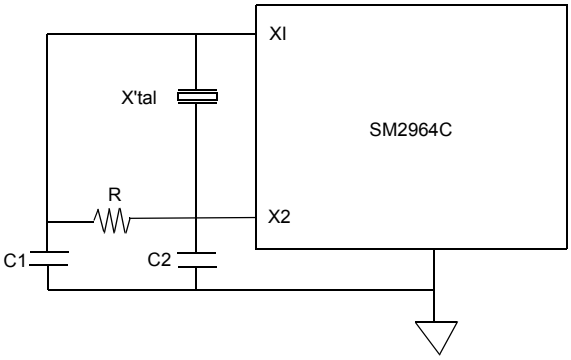
note1: no more than 80 mA IOLs for all 16-bit ports & 3 output pins.

To Programme

The Program mean is identical to MVI's flash V29C51002 except the memory size. This SM2964 has 512K bit (64K x 8) while the V29C51002 has 2 mega bit (256K x 8). Of course, the pin configuration is not identical. MVI provides an adapter board M9015 to transform those pins to fit into pins of commercial 2-mega-bit flash which is organized in 8-bit width.

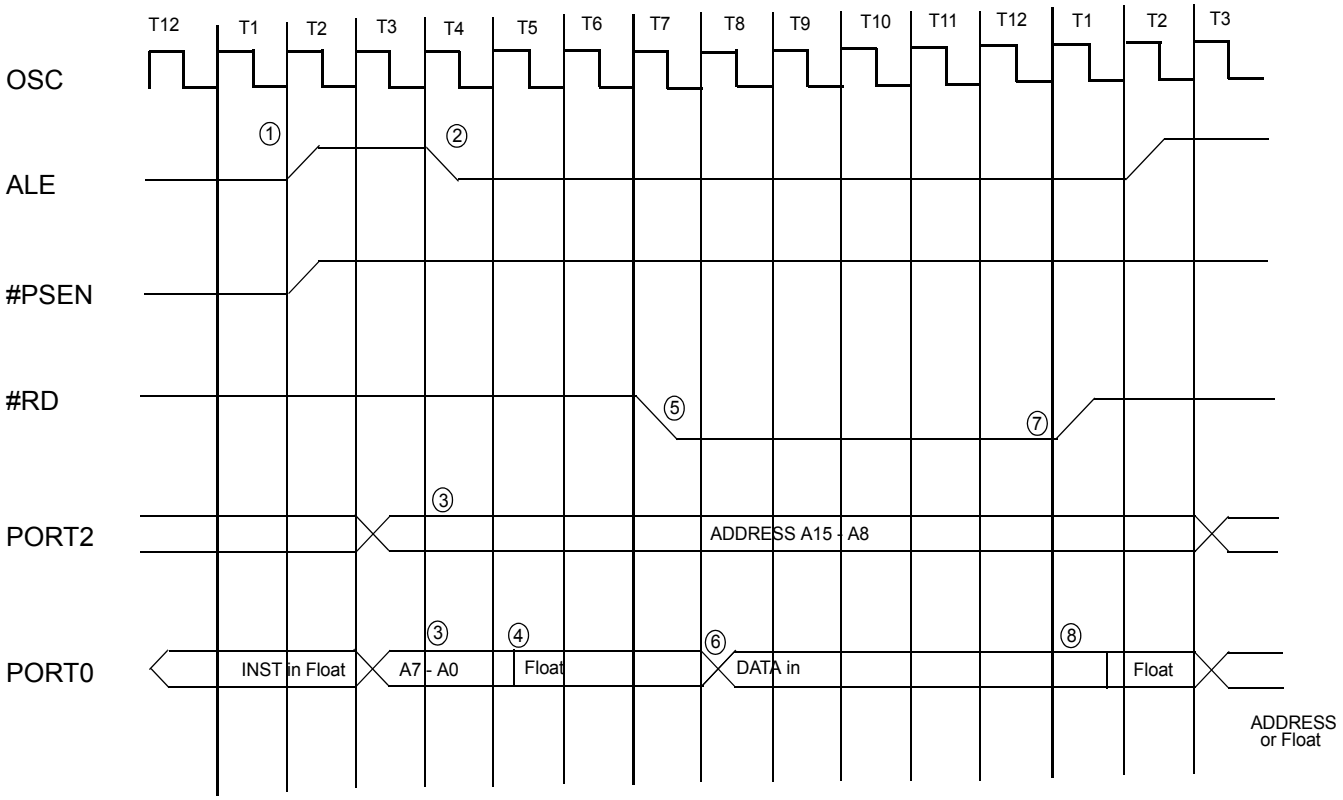
Application Reference

Valid for SM2964C				
X'tal	3MHz	6MHz	9MHz	12MHz
C1	30 pF	30 pF	30 pF	30 pF
C2	30 pF	30 pF	30 pF	30 pF
R	open	open	open	open
X'tal	16MHz	25MHz	33MHz	40MHz
C1	30 pF	15 pF	10 pF	2 pF
C2	30 pF	15 pF	10 pF	2 pF
R	open	62KΩ	6.8KΩ	4.7KΩ

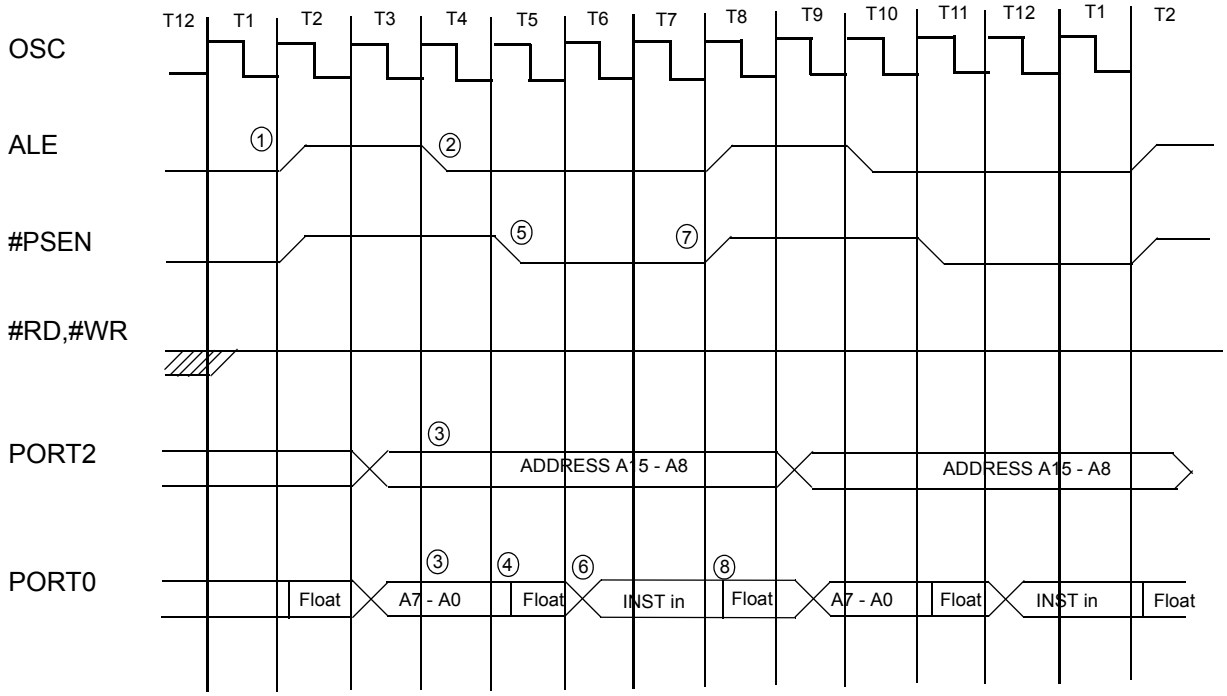


NOTE : Oscillation circuit may differs with different crystal or ceramic resonator, especially in higher oscillation frequency which was due to each crystal or ceramic resonator has its own characteristics. User should check with the crystal or ceramic resonator manufacture for appropriate value of external components.

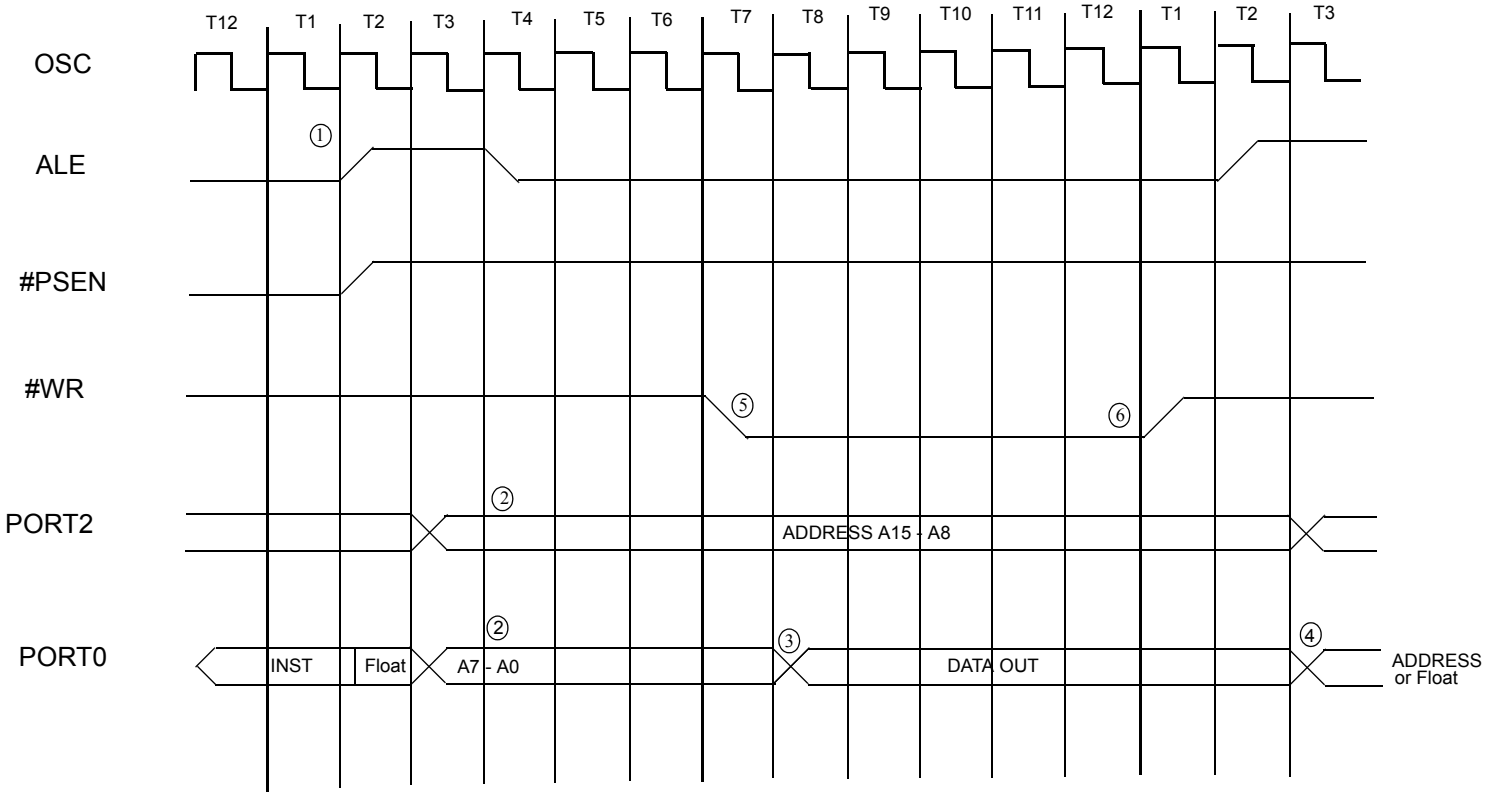
Data Memory Read Cycle Timing



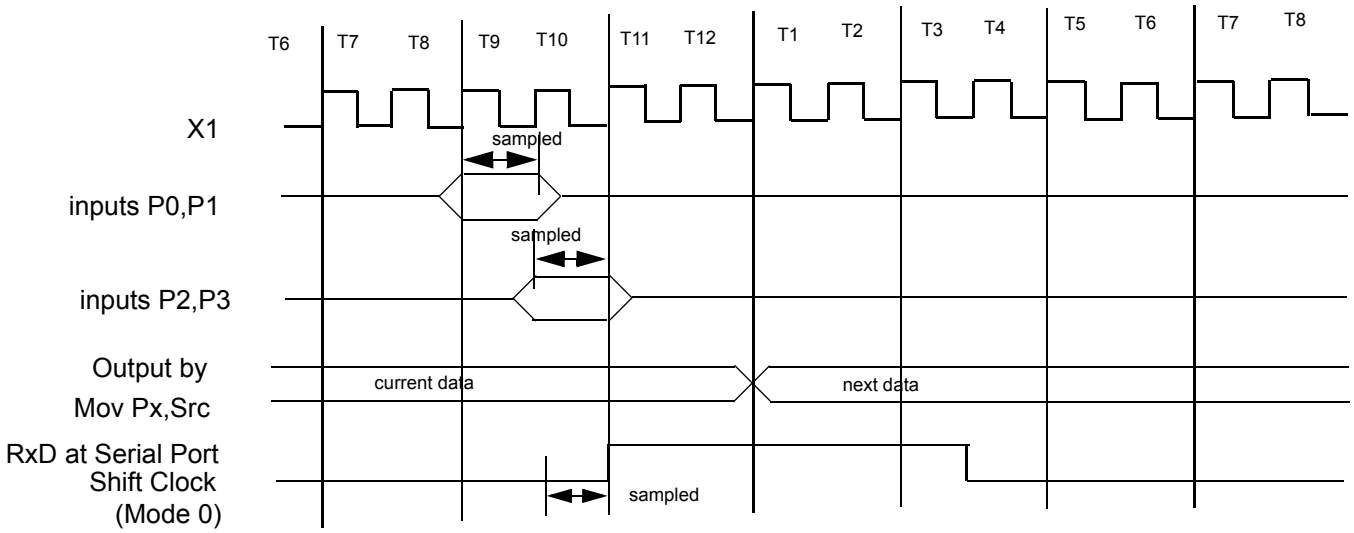
Program Memory Read Cycle Timing



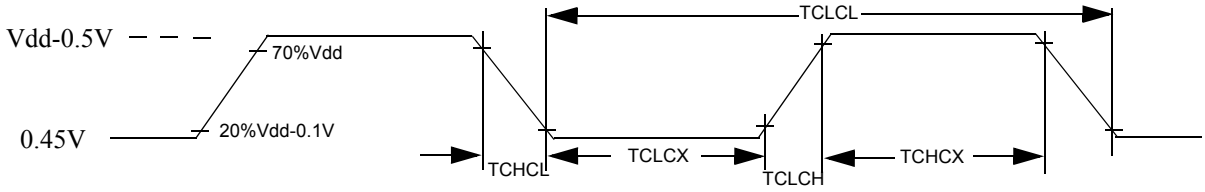
Data Memory Write Cycle Timing



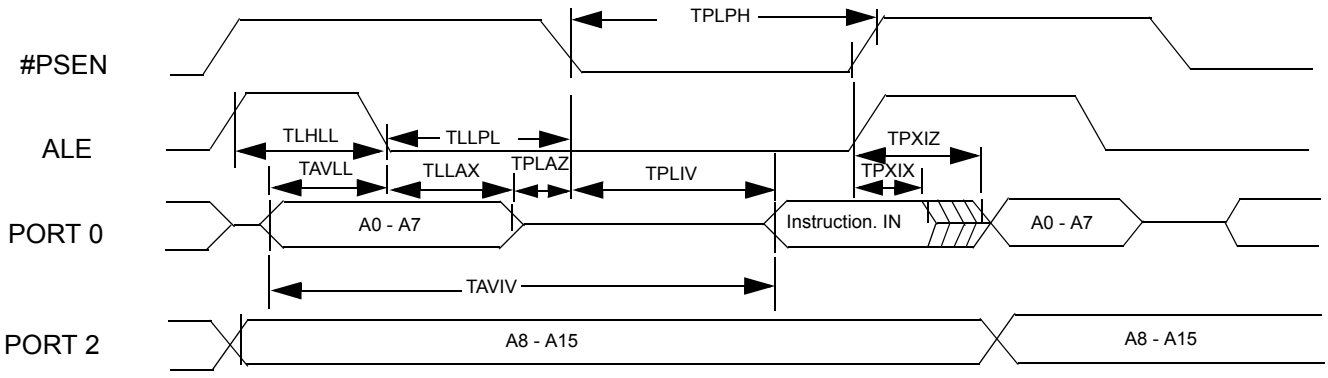
I/O Ports Timing



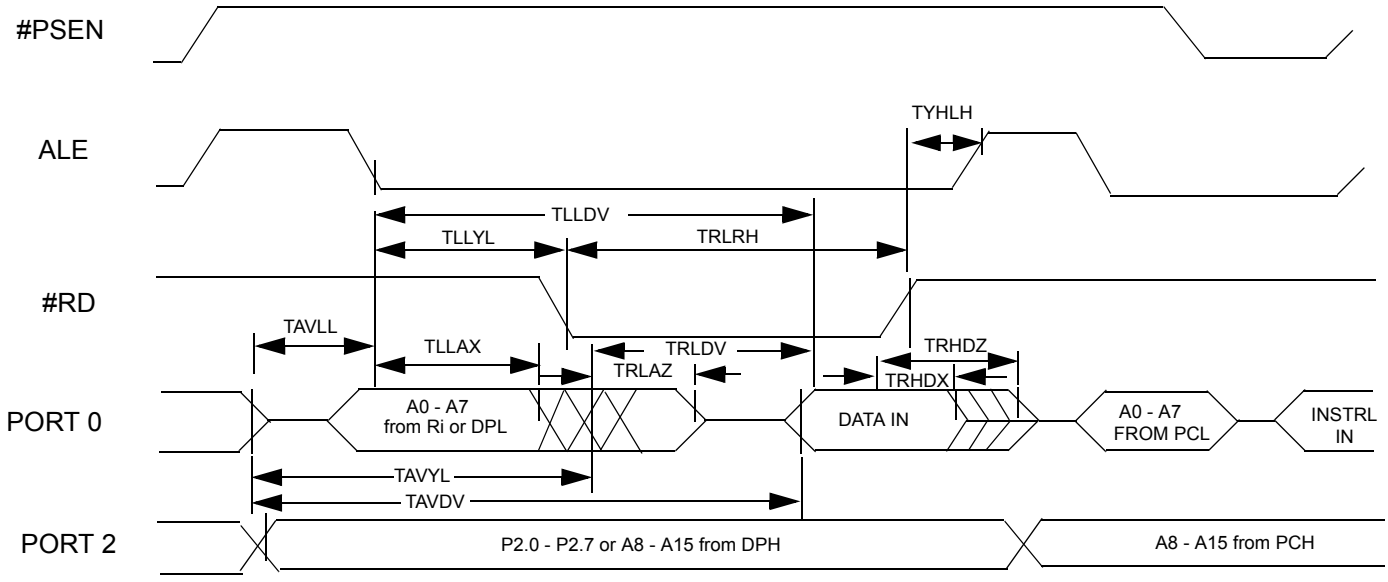
Timing Critical, Requirement of External Clock (Vss=0.0V is assumed)



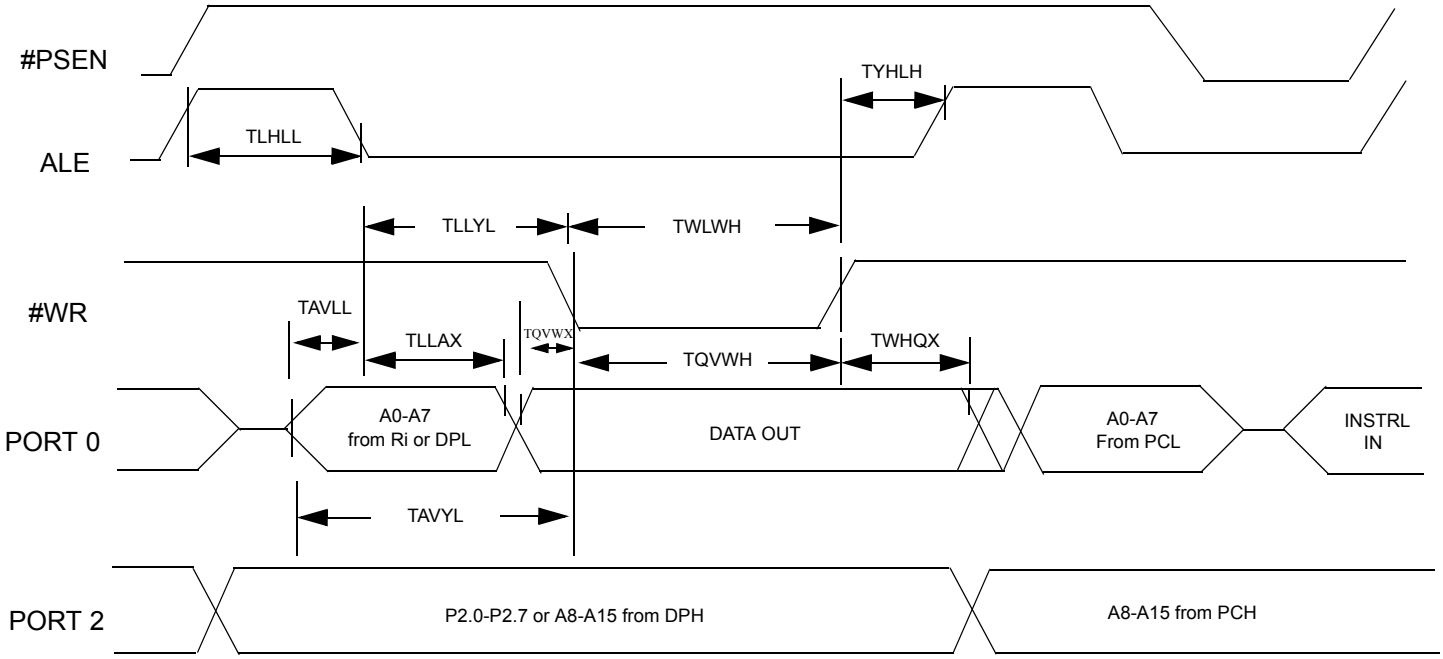
Tm.I External Program Memory Read Cycle



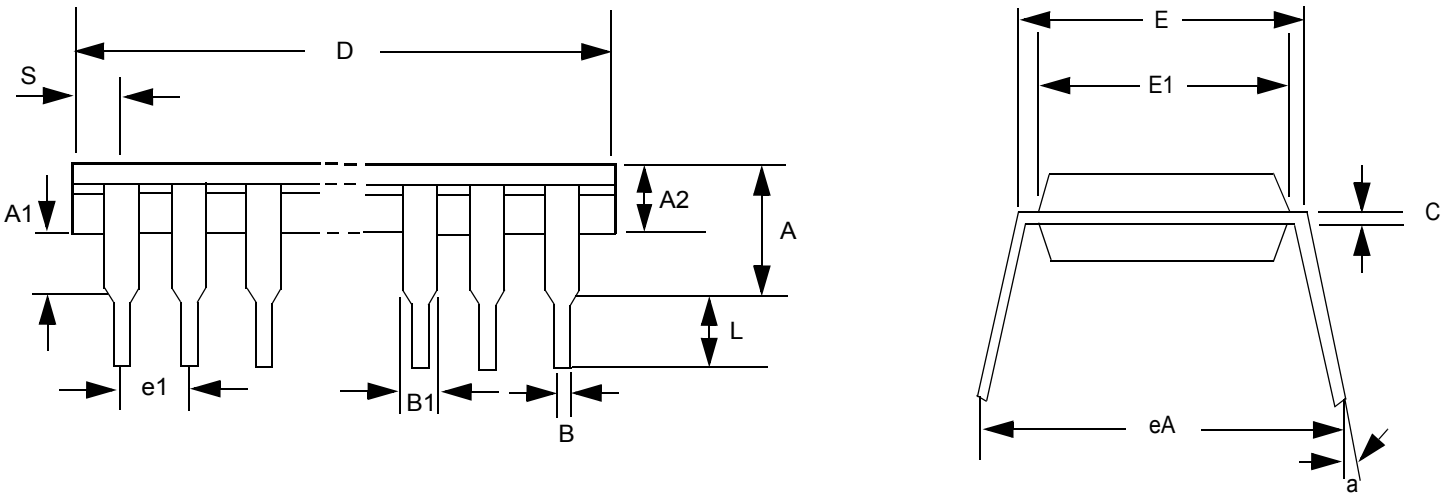
Tm.II External Data Memory Read Cycle



Tm.III External Data Memory Write Cycle



40L 600mil PDIP Information



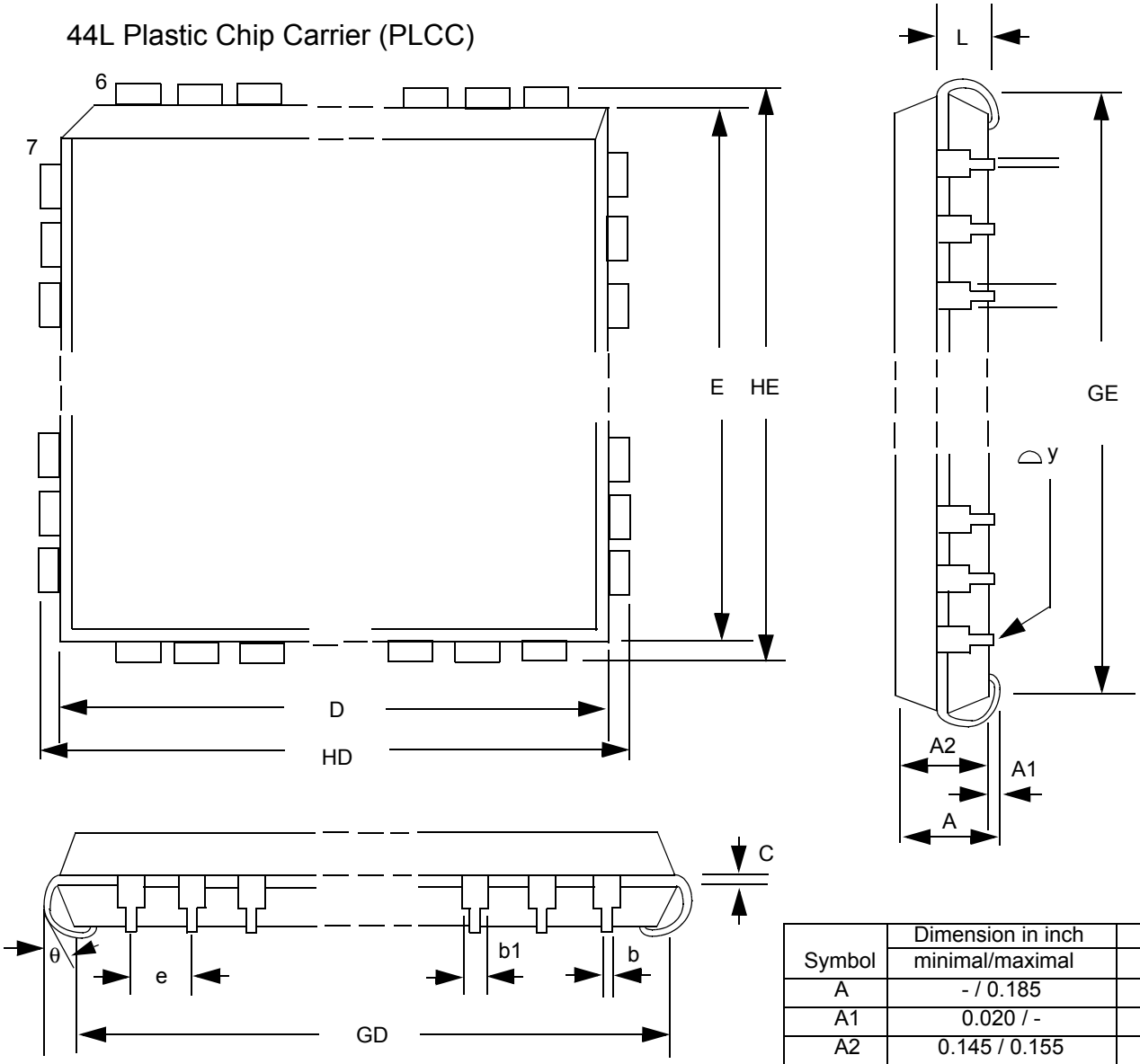
Note:

1. Dimension D Max & S include mold flash or tie bar burrs.
2. Dimension E1 does not include inter lead flash.
3. Dimension D & E1 include mold mismatch and are determined at the mold parting line.
4. Dimension B1 does not include dam bar protrusion/ infusion.
5. Controlling dimension is inch.
6. General appearance spec. should base on final visual inspection spec.

Symbol	Dimension in inch minimal/maximal	Dimension in mm minimal/maximal
A	- / 0.210	- / 5.33
A1	0.010 / -	0.25 / -
A2	0.150 / 0.160	3.81 / 4.06
B	0.016 / 0.022	0.41 / 0.56
B1	0.048 / 0.054	1.22 / 1.37
C	0.008 / 0.014	0.20 / 0.36
D	- / 2.070	- / 52.58
E	0.590 / 0.610	14.99 / 15.49
E1	0.540 / 0.552	13.72 / 14.02
e1	0.090 / 0.110	2.29 / 2.79
L	0.120 / 0.140	3.05 / 3.56
a	0° / 15°	0° / 15°
eA	0.630 / 0.670	16.00 / 17.02
S	- / 0.090	- / 2.29

December 1998

44L Plastic Chip Carrier (PLCC)



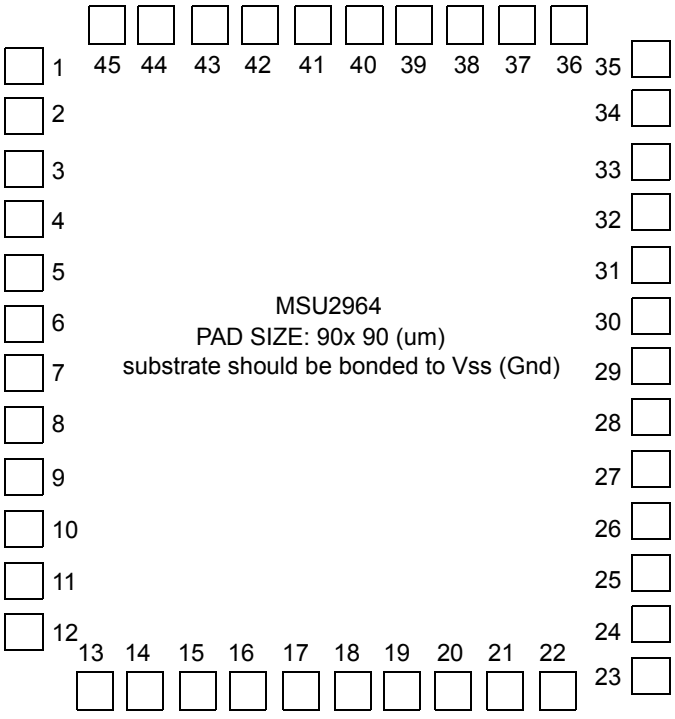
Note:

1.Dimension D & E does not include inter lead flash.
2.Dimension b1 does not include dam bar protrusion/ intrusion.
3.Controlling dimension: Inch
4.General appearance spec. should base on final visual inspection spec.

Symbol	Dimension in inch minimal/maximal	Dimension in mm minimal/maximal
A	- / 0.185	- / 4.70
A1	0.020 / -	0.51 / -
A2	0.145 / 0.155	3.68 / 3.94
b1	0.026 / 0.032	0.66 / 0.81
b	0.016 / 0.022	0.41 / 0.56
C	0.008 / 0.014	0.20 / 0.36
D	0.648 / 0.658	16.46 / 16.71
E	0.648 / 0.658	16.46 / 16.71
e	0.050 BSC	1.27 BSC
GD	0.590 / 0.630	14.99 / 16.00
GE	0.590 / 0.630	14.99 / 16.00
HD	0.680 / 0.700	17.27 / 17.78
HE	0.680 / 0.700	17.27 / 17.78
L	0.090 / 0.110	2.29 / 2.79
θ	- / 0.004	- / 0.10
⌓ y	/	/

Dice Pad Assignment

INDEX	PAD-NAME	INDEX	PAD-NAME	INDEX	PAD-NAME	INDEX	PAD-NAME
1	P3.6	13	P2.5	23	P0.3	36	P1.5
2	P3.7	14	P2.6	24	P0.2	37	P1.6
3	XTAL2	15	P2.7	25	P0.1	38	P1.7
4	XTAL1	16	#FOE	26	P0.0	39	RES
5	Vss	17	#FCE	27	Vdd	40	P3.0
6	Vss	18	#EA	28	Vdd	41	P3.1
7	Vss	19	P0.7	29	Vdd	42	P3.2
8	P2.0	20	P0.6	30	Vss	43	P3.3
9	P2.1	21	P0.5	31	P1.0	44	P3.4
10	P2.2	22	P0.4	32	P1.1	45	P3.5
11	P2.3			33	P1.2		
12	P2.4			34	P1.3		
				35	P1.4		



pid 264* 02/98
pid 264** 04/98
pid 264*** 11/98
pid 264**** 12/98
pid 264A 01/99
pid 264A* 08/00

Feedback / Inquiry:

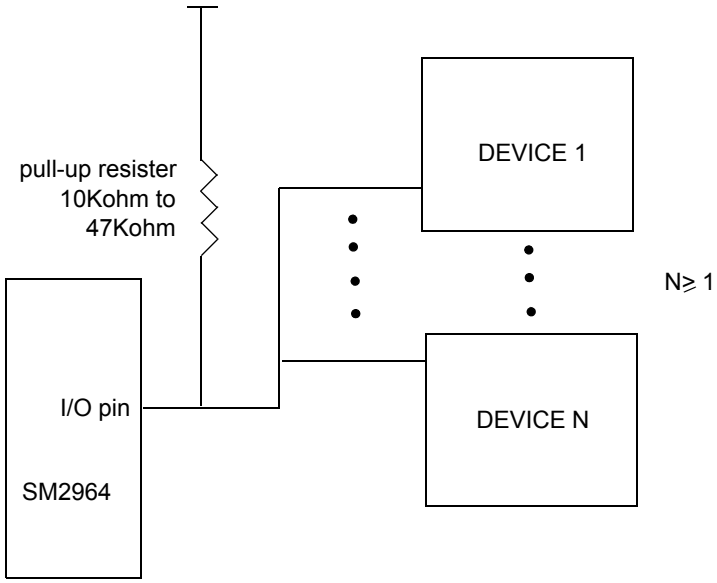
To :SyncMOS Technologies, Inc. Attn :MKT / Customer Service Dept. Fax :886-3-579-2960 :886-3-578-0493 Tel :886-3-579-2988 :886-3-579-2926	From : Company : Dept, Section : Position Title : Inquiry Date : Ref No :

☐ **Logo Top Marking Request & Spec.**
Below is the specification of logo in 20:1 scale base. This logo diagram is clear enough and is able to be shrunk directly to fit into available top marking area on top of the device package.

Description:

SM2964 Application Note

- SM2964 may need pull-up resistor when driving multiple device with its I/O pins.The pull-up resistor value 10Kohm to 47Kohm



- When using port 0 as input pin, user need to set corresponding SFR (special function register) to 1 before read in data through port 0. Otherwise data read may be incorrect.

e.g. Original program

```
mov   b,#0dh
djnz   b,$
mov   c,p0.2
mov   acc.7, c
```

Modified program

```
mov   b,#0dh
djnz   b,$
setb   p0.2
mov c,p0.2
mov.7, c
```

Extra instruction added

- SM2964 has 64KB internal ROM addressing space which fully occupies 16-bit address line.
  /EA pin of SM2964 will be disabled after internal ROM been protected. This feature will prevent internal ROM content been dump externally.
  If the internal ROM not been protected, /EA pin function of SM2964 will be the same as /EA pin function of intel 80C52.