AP393

LOW POWER LOW OFFSET VOLTAGE DUAL COMPARATORS

Features

- Wide supply
  Voltage range: 2.0V to 36V
  Single or dual supplies: ±1.0V to ±18V
- Very low supply current drain (0.4mA) – independent of supply voltage
- Low input biasing current: 25nA
- Low input offset current: ±5nA
- Maximum offset voltage: ±3mV
- Input common-mode voltage range includes ground
- Differential input voltage range equal to the power supply voltage
- Low output saturation voltage: 250mV at 4mA
- Output voltage compatible with TTL, DTL, ECL, MOS and CMOS logic systems
- SOP-8L, PDIP-8L package
- SOP-8L: Available in "Green" Molding Compound (No Br, Sb) (Note 1)
- Lead Free Finish/RoHS Compliant for Lead Free and "Green" Products (Note 2)

General Description

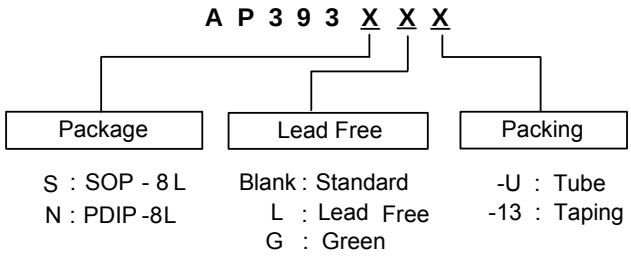
The AP393 consists of two independent precision voltage comparators with an offset voltage specification as low as 2.0mV max for two comparators which were designed specifically to operate from a single power supply over a wide range of voltages. Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage. These comparators also have a unique characteristic in that the input common-mode voltage range includes ground, even though operated from a single power supply voltage.

Application areas include limit comparators, simple analog to digital converters; pulse, squarewave and time delay generators; wide range VCO; MOS clock timers; multivibrators and high voltage digital logic gates. The AP393 is designed to directly interface with TTL and CMOS. When operated from both plus and minus power supplies, the AP393 will directly interface with MOS logic where their low power drain is a distinct advantage over standard comparators.

Applications

- High precision comparators
- Reduced V_{OS} drift over temperature
- Eliminates need for dual supplies
- Allows sensing near ground
- Compatible with all forms of logic
- Power drain suitable for battery operation

Ordering Information

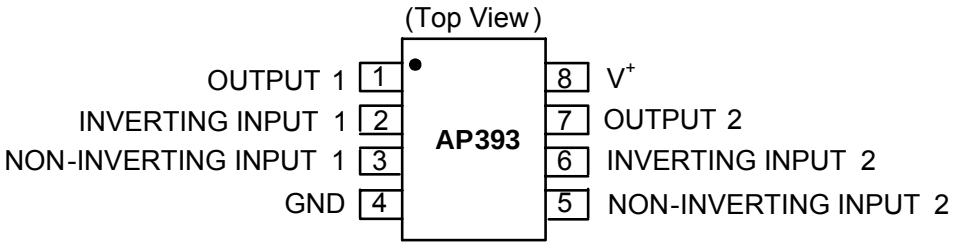


Note: 1. SOP-8L is "Green" product only.
2. RoHS revision 13.2.2003. Glass and High Temperature Solder Exemptions Applied, see *EU Directive Annex Notes 5 and 7.*

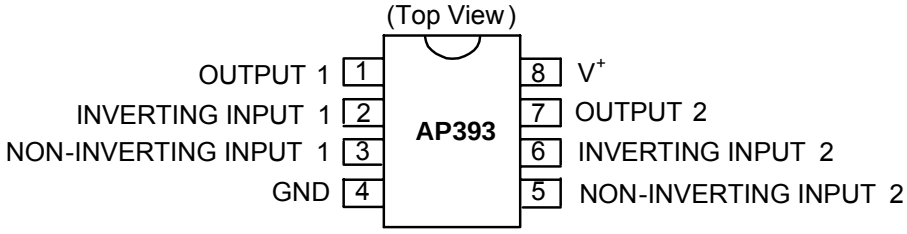
Device	Package Code	Packaging	Tube		13" Tape and Reel	
			Quantity	Part Number Suffix	Quantity	Part Number Suffix
AP393S	S	SOP-8L	100	- U	2500/Tape & Reel	-13
AP393N	N	PDIP-8L	60	- U	NA	NA

Note: 3. Pad layout as shown on Diodes Inc. suggested pad layout document AP02001, which can be found on our website at http://www.diodes.com/datasheets/ap02001.pdf.

Pin Assignments



SOP-8L

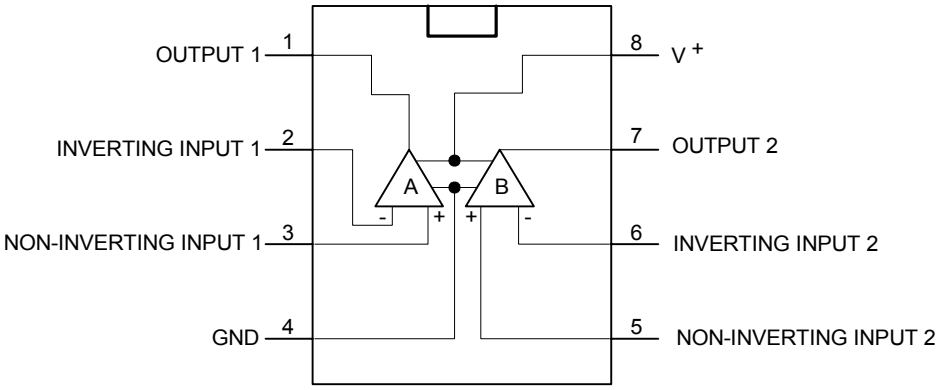


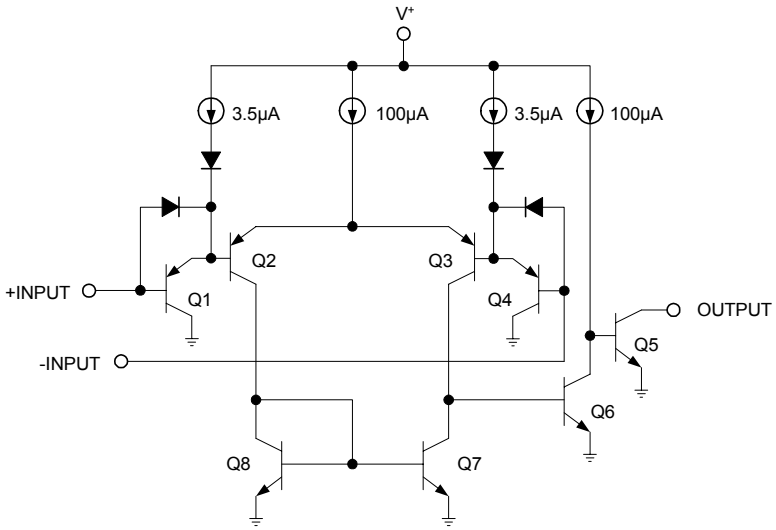
PDIP -8L

Pin Descriptions

Pin Name	Pin No.	Description
OUTPUT 1	1	Channel 1 Output
INVERTING INPUT 1	2	Channel 1 Negative Input
NON-INVERTING INPUT 1	3	Channel 1 Positive Input
GND	4	Ground
NON-INVERTING INPUT 2	5	Channel 2 Positive Input
INVERTING INPUT 2	6	Channel 2 Negative Input
OUTPUT 2	7	Channel 2 Output
V^+	8	V_{CC}

Block Diagram





Absolute Maximum Ratings (Note 13)

Symbol	Parameter		Rating	Unit
V_{CC}	Supply Voltage		36	V
V_{IN}	Differential Input Voltage **(Note 11)**		36	V
V_{IN}	Input Voltage		-0.3 to +36	V
I_{CC}	Input Current (V_{IN}-0.3V) **(Note 6)**		50	mA
P_D	Power Dissipation **(Note 4)**	PDIP-8L	780	mW
		SOP-8L	510	
	Output Short-Circuit to Ground **(Note 5)**		Continuous	
T_{OP}	Operating Junction Temperature Range		0 to +70	°C
T_{ST}	Storage Temperature Range		-65 to +150	°C

Electrical Characteristics (V_{CC} = 5V, T_A = 25°C, unless otherwise stated)

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Unit
V_{OFFSET}	Input Offset Voltage	**(Note 12)**		-	1.0	5.0	mV
I_{BIAS}	Input Bias Current	I_{IN}(+) or I_{IN}(-) with Output In Linear Range, V_{CM} = 0V **(Note 8)**		-	25	250	nA
I_{OFFSET}	Input Offset Current	I_{IN}(+) - I_{IN}(-) V_{CM} = 0V		-	5.0	50	nA
	Input Common Mode Voltage Range	V^+ = 30V **(Note 9)**		0	-	V^+ -1.5	V
I_{CC}	Supply Current	R_L = ∞	V^+ = 5V	-	0.4	1	mA
			V^+ = 36V	-	1	2.5	
	Voltage Gain	$R_L \geq$ 15kΩ, V^+ = 15V V_O = 1V to 11V		50	200	-	V/mV
	Large Signal Response Time	V_{IN} = TTL Logic Swing, V_{REF} = 1.4V, V_{RL} = 5V, R_L = 5.1kΩ		-	300	-	ns
	Response Time	V_{RL} = 5V, R_L = 5.1kΩ **(Note 10)**		-	1.3	-	µs
$I_{O(Sink)}$	Output Sink Current	V_{IN}(-) = 1V, V_{IN}(+) = 0, $V_O \leq$ 1.5V		6.0	16	-	mA
V_{SAT}	Saturation Voltage	V_{IN}(-) = 1V, V_{IN}(+) = 0, $I_{SINK} \leq$ 4mA		-	250	400	mV
$I_{O(Leak)}$	Output Leakage Current	V_{IN}(-) = 0, V_{IN}(+) = 1V, V_O = 5V		-	0.1	-	nA

Electrical Characteristics (V_{CC} = 5V) **(Note 7)**

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{OFFSET}	Input Offset Voltage	**(Note 12)**	-	-	9	mV
I_{OFFSET}	Input Offset Current	$I_{IN}(+)$ -$I_{IN}(-)$, V_{CM} = 0V	-	-	150	nA
I_{BIAS}	Input Bias Current	$I_{IN}(+)$ or $I_{IN}(-)$ with Output In Linear Range, V_{CM} = 0V **(Note 8)**	-	-	400	nA
	Input Common Mode Voltage Range	V^+ =30V **(Note 9)**	0	-	V^+-2.0	V
V_{SAT}	Saturation Voltage	$V_{IN}(-)$ = 1V, $V_{IN}(+)$ = 0, $I_{SINK} \leq$ 4mA	-	-	700	mV
$I_{O(Leak)}$	Output Leakage Current	$V_{IN}(-)$ = 0, $V_{IN}(+)$ = 1V, V_O = 30V	-	-	1.0	µA
	Differential Input Voltage	Keep All V_{IN}'s $\geq$ 0V (or V^-, if Used), **(Note 11)**	-	-	36	V

Note:
4. For operating at high temperatures, the AP393 must be derated based on a 125°C maximum junction temperature and a thermal resistance of 170°C/W which applies for the device soldered in a printed circuit board, operating in a still air ambient. The low bias dissipation and the "ON-OFF" characteristic of the outputs keeps the chip dissipation very small ($P_D \leq$100mW), provided the output transistors are allowed to saturate.
5. Short circuits from the output to V^+ can cause excessive heating and eventual destruction. When considering short circuits to ground, the maximum output current is approximately 20mA independent of the magnitude of V^+.
6. This input current will only exist when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistors becoming forward biased and thereby acting as input diode clamps. In addition to this diode action, there is also lateral NPN parasitic transistor action on the IC chip. This transistor action can cause the output voltages of the comparators to go to the V^+ voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This is not destructive and normal output states will re-establish when the input voltage, which is negative, again returns to a value greater than -0.3V.
7. The AP393 temperature specifications are limited to 0°C $\leq T_{OP} \leq$ +70°C.
8. The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the reference or input lines.
9. The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is V^+-1.5V at 25°C, but either or both inputs can go to 36V without damage, independent of the magnitude of V^+.
10. The response time specified is for a 100mV input step with 5mV overdrive. For larger overdrive signals 300ns can be obtained, see typical performance characteristics section.
11. Positive excursions of input voltage may exceed the power supply level. As long as the other voltage remains within the common-mode range, the comparator will provide a proper output state. The low input voltage state must not be less than -0.3V (or 0.3V below the magnitude of the negative power supply, if used).
12. At output switch point, $V_O \simeq$ 1.4V, R_S=0Ω with V^+ from 5V to 30V; and over the full input common-mode range (0V to V^+-1.5V), at 25°C.
13. Refer to RETS193AX for AP393 military specifications.

Application Information

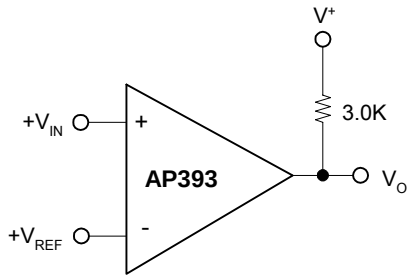
The AP393 is high gain, wide bandwidth devices, like most comparators, can easily oscillate if the output lead is inadvertently allowed to capacitively couple to the inputs via stray capacitance. This shows up only during the output voltage transition intervals as the comparator change states. Power supply bypassing is not required to solve this problem. Standard PC board layout is helpful as it reduces stray input-output coupling. Reducing the input resistors to < 10kΩ reduces the feedback signal levels and finally, adding even a small amount (1.0 to 10 mV) of positive feedback (hysteresis) causes such a rapid transition that oscillations due to stray feedback are not possible. Simply socketing the IC and attaching resistors to the pins will cause input-output oscillations during the small transition intervals unless hysteresis is used. If the input signal is a pulse waveform, with relatively fast rise and fall times, hysteresis is not required. All input pins of any unused comparators should be tied to the negative supply.

The bias network of the AP393 establishes a drain current independent of the magnitude of the power supply voltage over the range of from 2.0 V_{DC} to 30 V_{DC}. It is usually unnecessary to use a bypass capacitor across the power supply line.

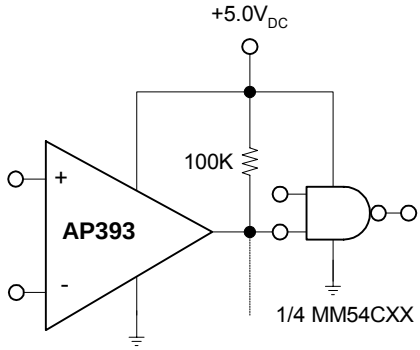
The differential input voltage may be larger than V+ without damaging the device (Note 8). Protection should be provided to prevent the input voltages from going negative more than -0.3 V_{DC} (at 25°C). An input clamp diode can be used as shown in the applications section.

The output of the AP393 is the uncommitted collector of a grounded-emitter NPN output transistor. Many collectors can be tied together to provide an output OR'ing function. An output pull-up resistor can be connected to any available power supply voltage within the permitted supply voltage range and there is no restriction on this voltage due to the magnitude of the voltage applied to the V^+ terminal of the AP393 package. The output can also be used as a simple SPST switch to ground (when a pull-up resistor is not used). The amount of current the output device can sink is limited by the drive available (which is independent of V^+) and the β of this device. When the maximum current limit is reached (approximately 16mA), the output transistor will come out of saturation and the output voltage will rise very rapidly. The output saturation voltage is limited by the approximately 60Ω r_{SAT} of the output transistor. The low offset voltage of the output transistor (1.0 mV) allows the output to clamp essentially to ground level for small load currents.

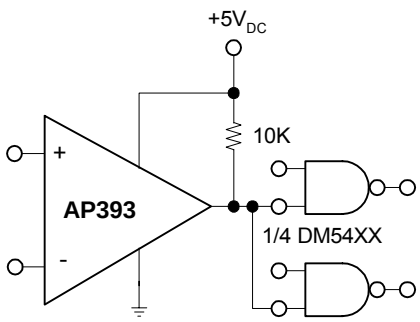
Typical Circuit (V_{CC} = 5.0V_{DC})



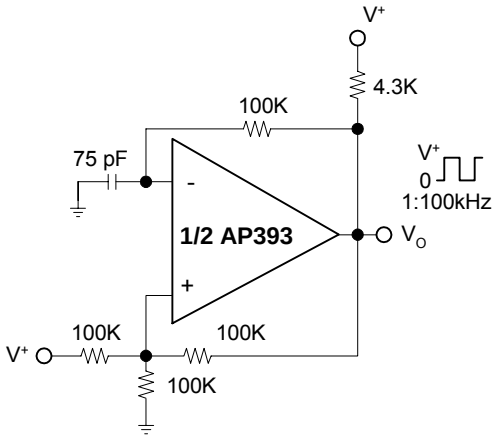
Basic Comparator



Driving CMOS

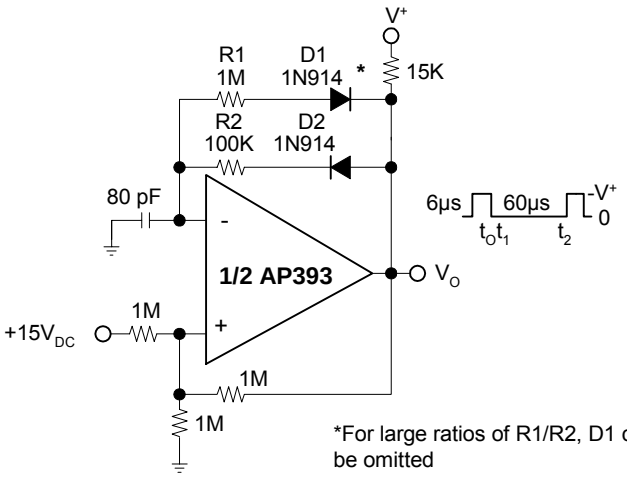


Driving TTL

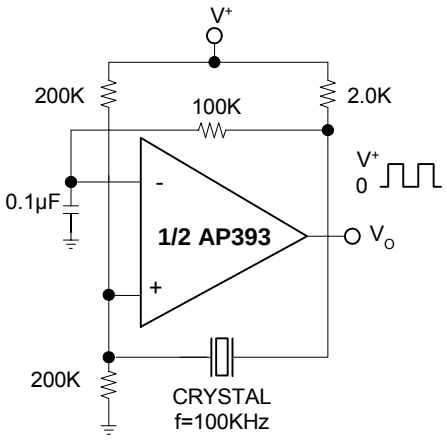


Squarewave Oscillator

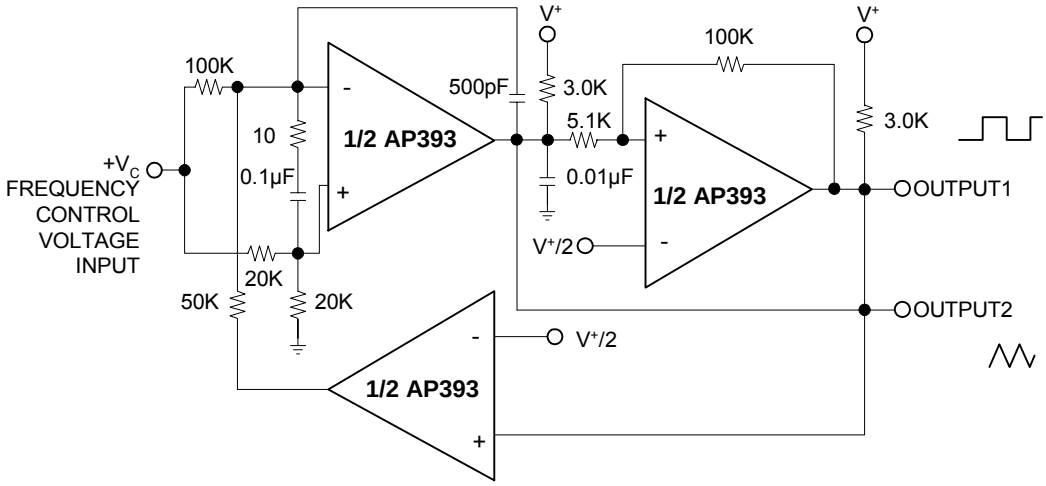
Typical Circuit (Continued) (V_{CC} = 5.0V_{DC})



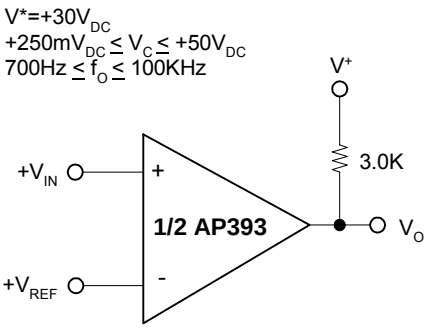
Pulse Generator



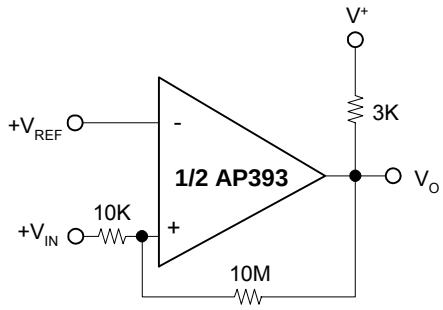
Crystal Controlled Oscillator



Two-Decade High Frequency VCO

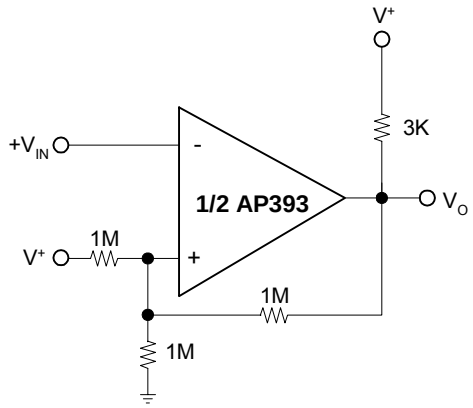


Basic Comparator

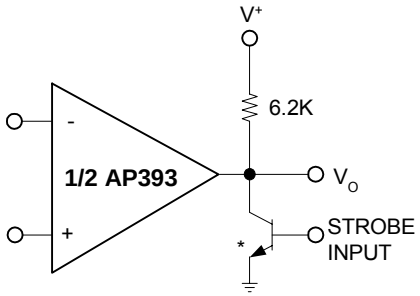


Non-Inverting Comparator with Hysteresis

Typical Circuit (Continued) (V_{CC} = 5.0V_{DC})

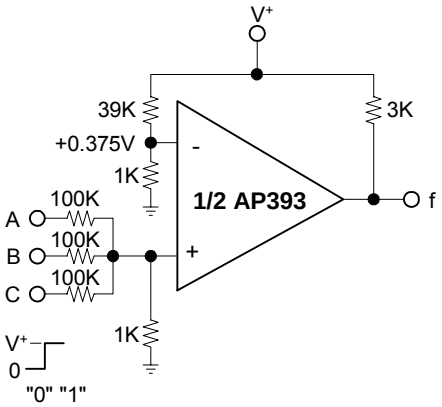


Inverting Comparator with Hysteresis

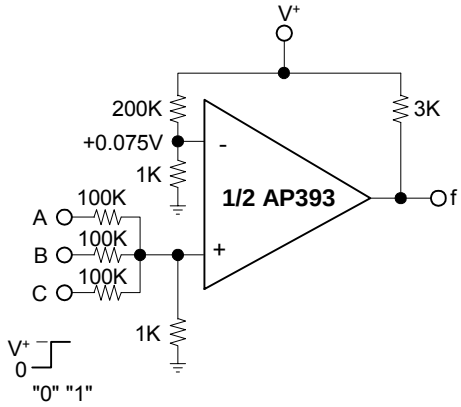


* OR LOGIC GATE WITHOUT PULL-UP RESISTOR

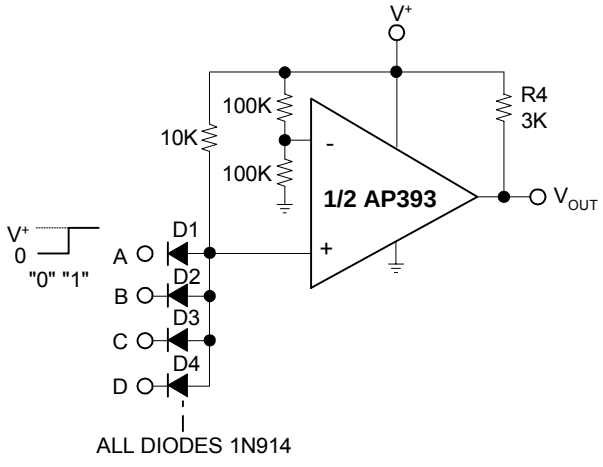
Output Strobing



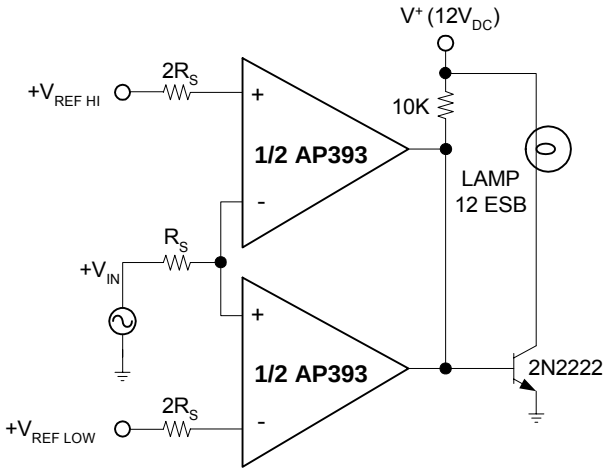
AND Gate



Or Gate

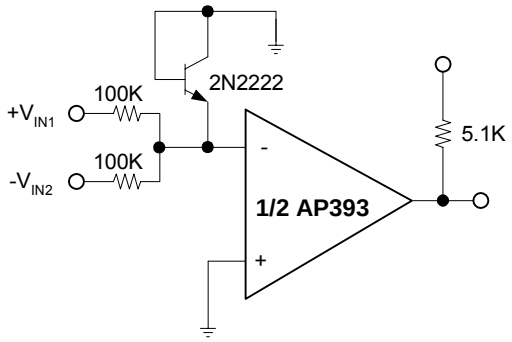


Large Fan-in AND Gate

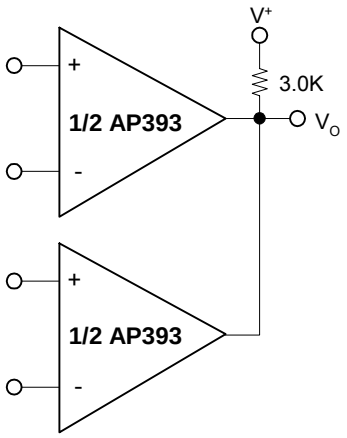


Limit Comparator

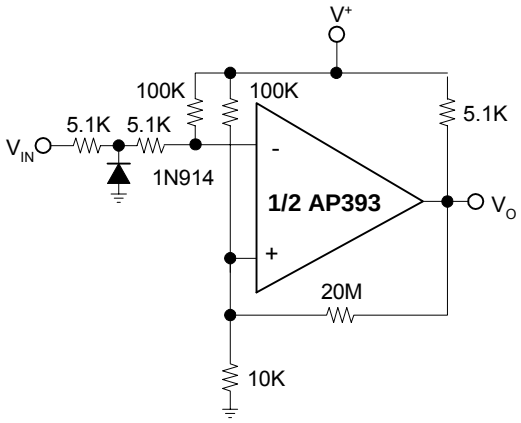
Typical Circuit (Continued) (V_{CC} = 5.0V_{DC})



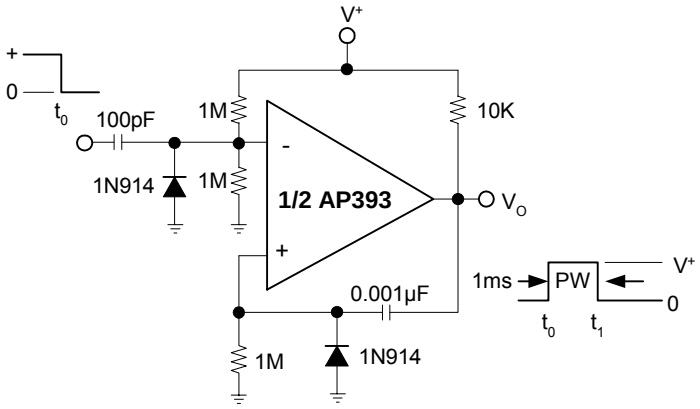
Comparing Input Voltages of Opposite Polarity



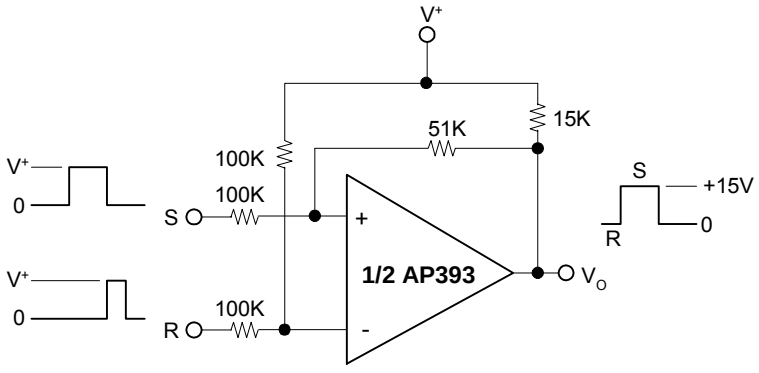
ORing the Outputs



Zero Crossing Detector (Single Power Supply)

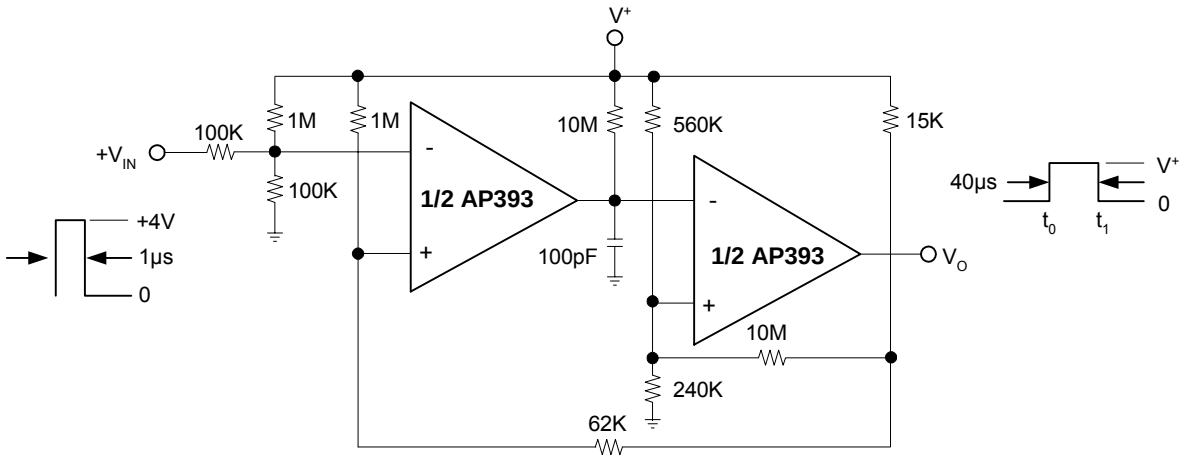


One-Shot Multivibrator

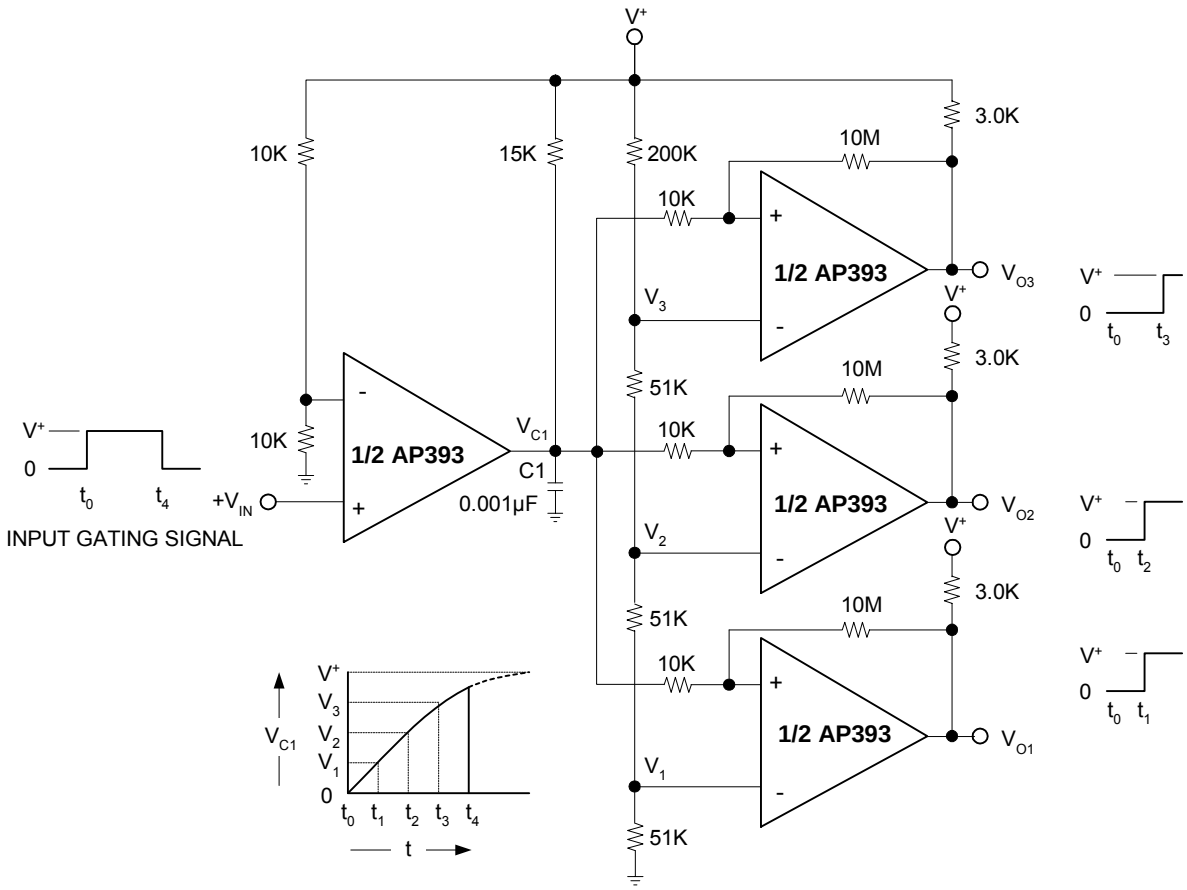


Bi-Stable Multivibrator

Typical Circuit (Continued) (V_{CC} = 5.0V_{DC})

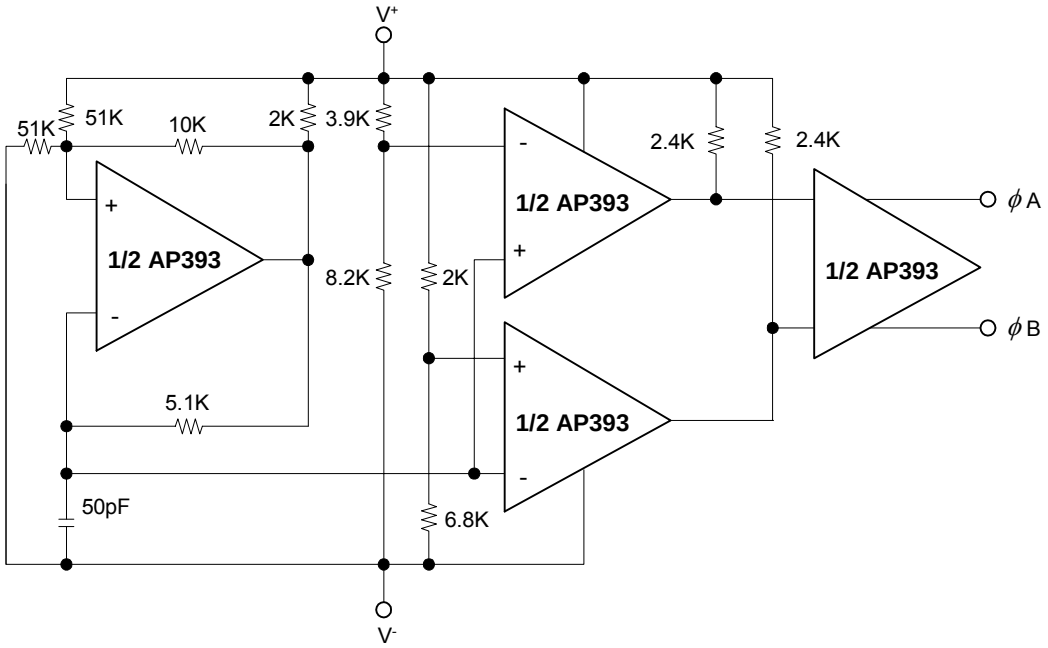


One-Shot Multivibrator with Input Lock Out

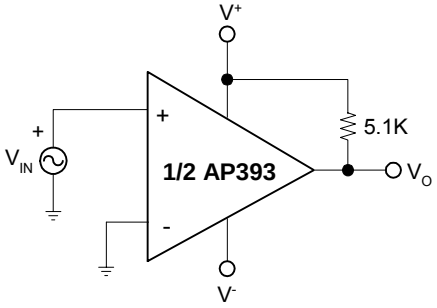


Time Delay Generator

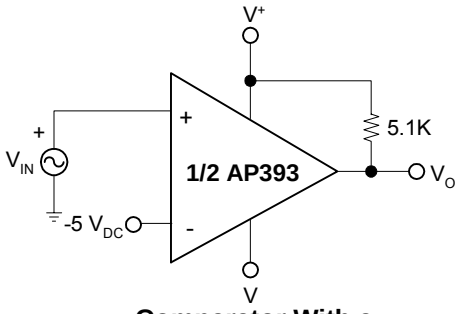
Split-Supply Applications ($V^+ = +15V_{DC}$ and $V^- = -15\ V_{DC}$)



MOS Clock Driver

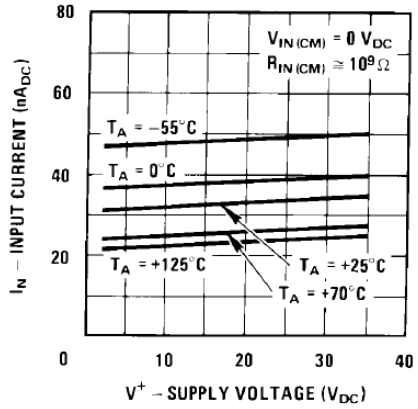


Zero Crossing Detector

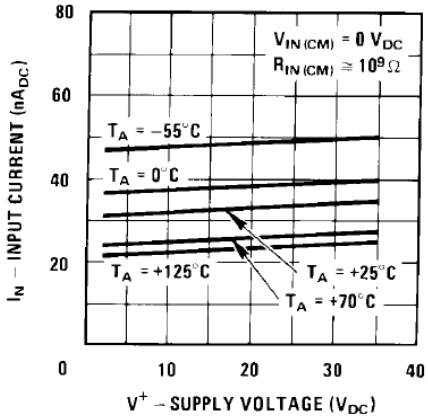


Comparator With a Negative Reference

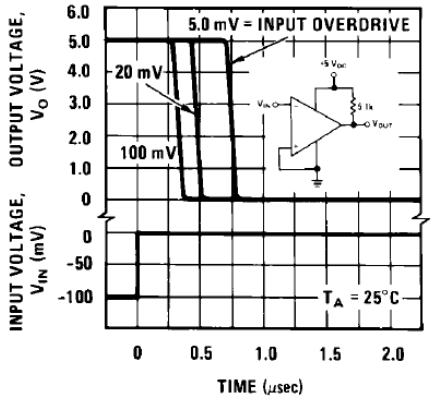
Typical Characteristics



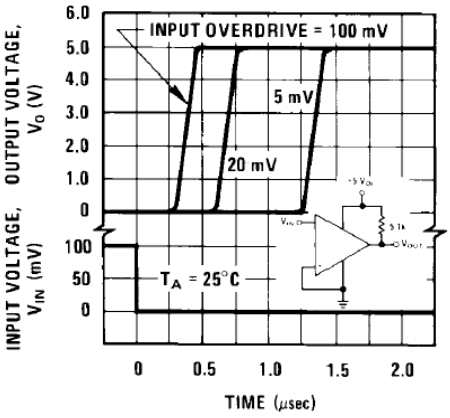
Supply Current



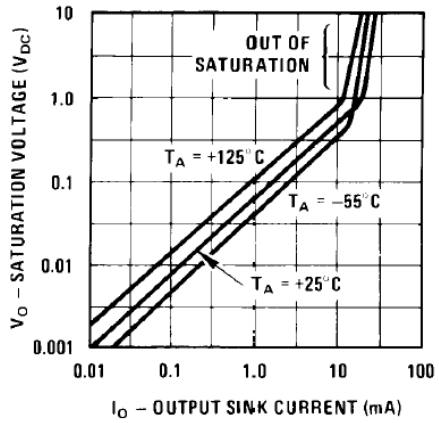
Input Current



Response Time for Various Input Overdrives—Negative Transition



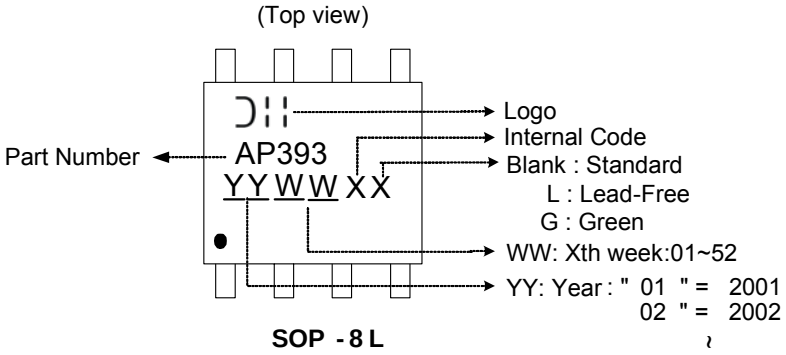
Response Time for Various Input Overdrives—Positive Transition



Output Saturation Voltage

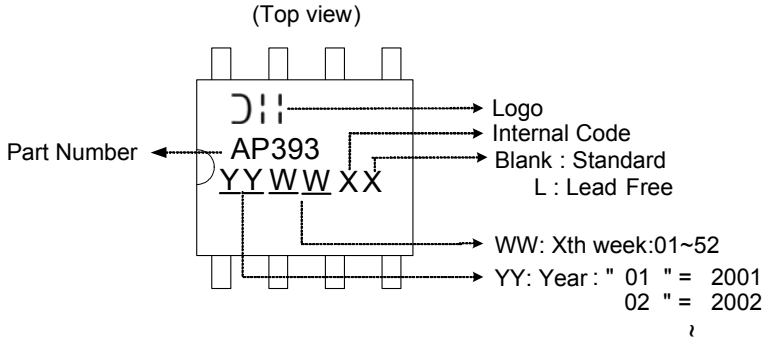
Marking Information

(1) SOP-8L



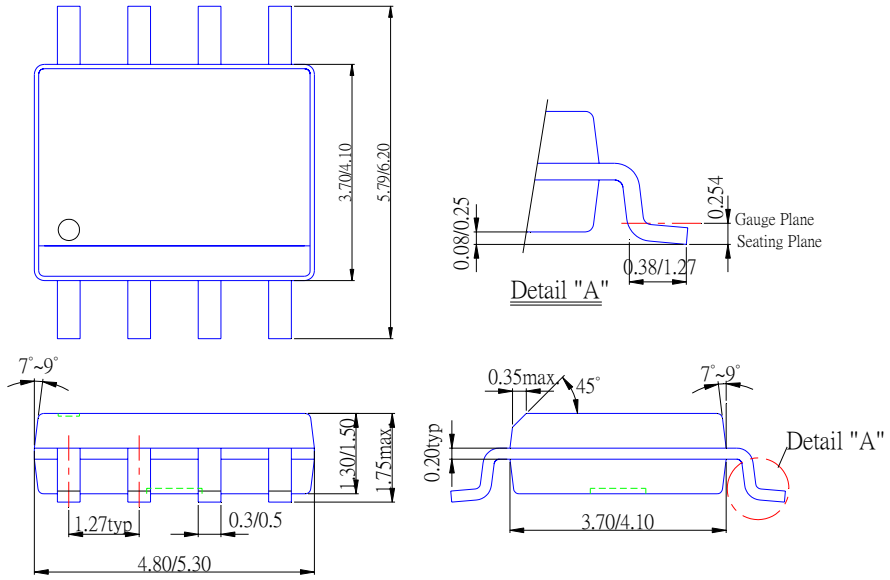
SOP - 8 L

(2) PDIP-8L

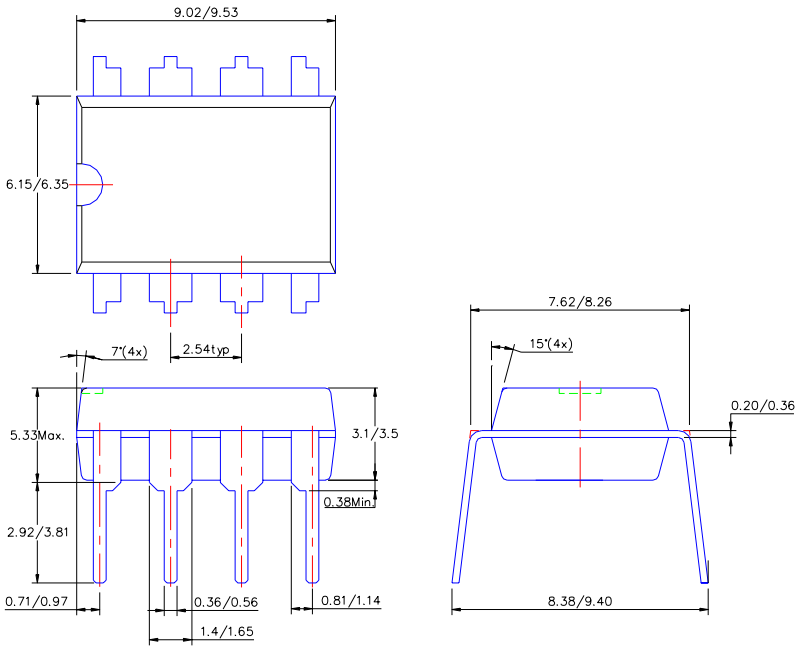


Package Information

(1) SOP-8L (JEDEC Small Outline Package)



(2) PDIP-8L



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