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FUJITSU

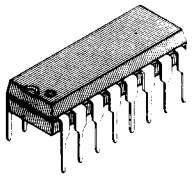
DATA SHEET

MB87002
1200 BPS MSK MODEM

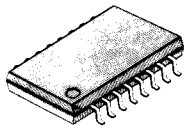
1200 BPS MSK (Minimum Shift Keying) MODEM

The MB87002 is a 1200–bps CMOS minimum shift keying (MSK) single–chip modem for multichannel access (MCA) and radio communication application. Its operation at low supply voltages and low power consumption is especially suitable for portable application.

- Data rate: 1200–bps
- Low power consumption (20 mW with 5 V power supply)
- Low supply voltage operation: 3.0 to 5.5 V (5 V typical)
- On–chip crystal oscillator: 3.6864 MHz
- Switched–capacitor filter (SCF)
- Selectable timing regenerator pull–in characteristic (within 15 bits for high–speed, and within 25 bits for low–speed operation)
- Low external component count
- TTL compatible inputs and outputs



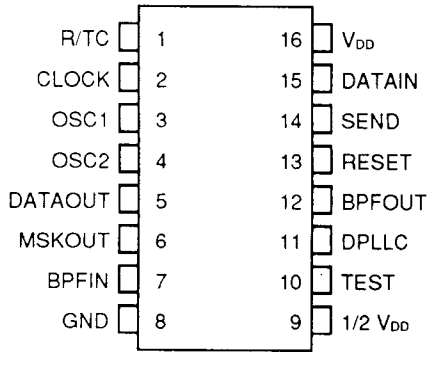
PLASTIC PACKAGE
(DIP-16P-M03)



PLASTIC PACKAGE
(FPT-16P-M03)

PIN ASSIGNMENT

(TOP VIEW)



ABSOLUTE MAXIMUM RATINGS (See NOTE)

Parameter	Symbol	Pin name	Value			Unit
			Min	Typ	Max	
Power Supply Voltage	V_{DD}	V_{DD}	GND – 0.3	–	7	V
Input Voltage	V_{IN}	All input pins	GND – 0.3	–	V_{DD} + 0.3	V
Output Voltage	V_{OUT}	All output pins	GND – 0.3	–	V_{DD} + 0.3	V
Output Current	I_{OUT}	All output pins	–10	–	10	mA
Storage Temperature	T_{STG}	–	–55	–	125	°C

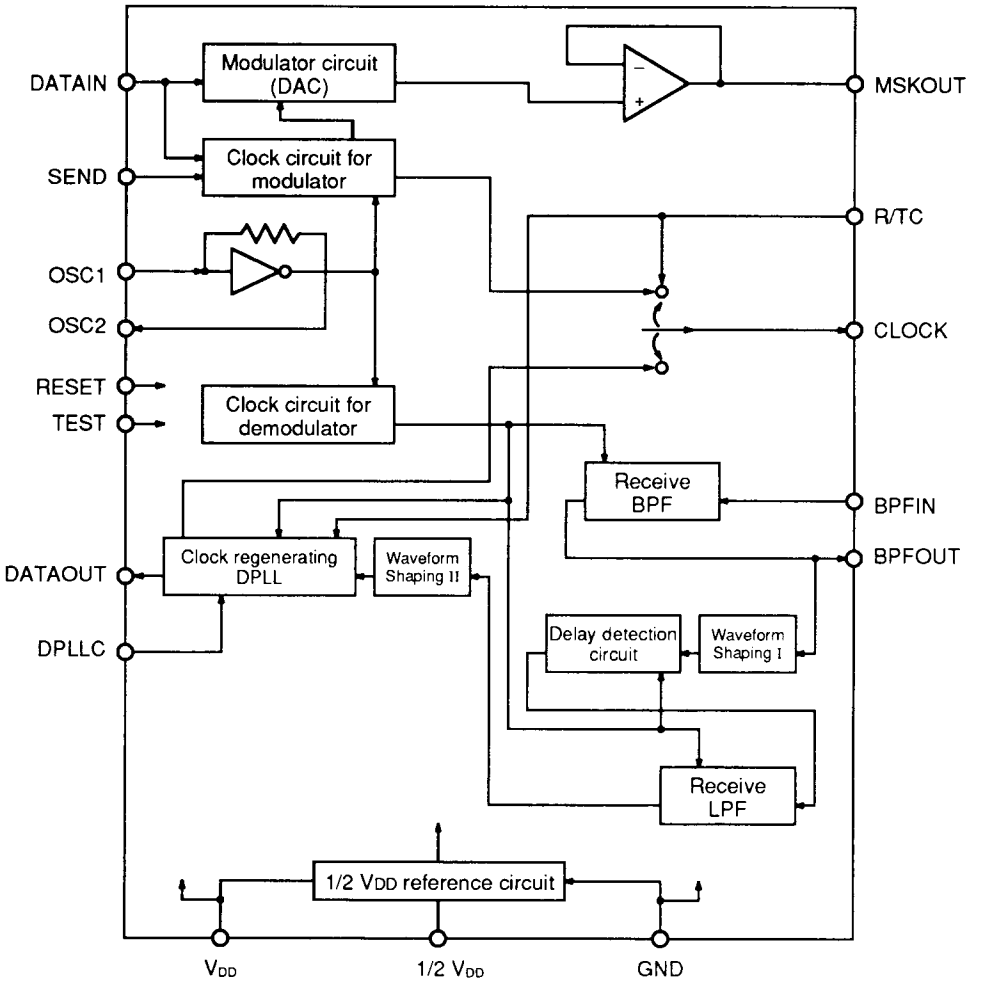
NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

PIN DESCRIPTIONS

Pin No.	Symbol	I/O	Functional descriptions
1	R/TC	I	Transmit–receive clock output control. When pulled high, the 1.2 kHz transmit clock is output from the CLOCK pin and DATAOUT becomes low. When pulled low, the 1.2 kHz receive clock is output from the CLOCK pin.
2	CLOCK	O	Transmit–receive clock output pin. When R/TC pin is pulled high, 1.2 kHz transmit clock is output. When R/TC pin is pulled low, the 1.2 kHz receive clock is output.
3	OSC1	I	Pin for external crystal (3.6864 MHz) connection.
4	OSC2	O	Pin for external crystal (3.6864 MHz) connection.
5	DATAOUT	O	Regenerated data output signal.
6	MSKOUT	O	Modulated signal output pin. $V_{DD}/2$ is output when the RESET pin is pulled low.
7	BPFIN	I	Demodulated signal input to the receive band–pass filter (BPF).
8	GND	–	Ground
9	1/2 V_{DD}	O	$V_{DD}/2$ reference voltage output
10	TEST	I	Test function control signal input. In the normal mode, this pin is pulled high or left open. In the test mode, it is pulled low. In the test mode, the BPF IN pin directly accepts Waveform Shaping I and receive LPF input signals, and the DATA IN pin directly accepts Waveform Shaping II input signals. In this mode, the delay detection circuit signal is output from BPFOUT and the receive LPF signal is output from MSKOUT.
11	DPLLC	I	DPLL pull–in time control signal input. When pulled low, high–speed operation is selected. When pulled high, low–speed operation is selected.
12	BPFOUT	O	Receive BPF output pin.
13	RESET	I	Device reset signal input. A low on this pin resets all circuits. Pulled high or left open to enable device operation.
14	SEND	I	Data transmit enable. With the reset high or open, transmit signals are output when this pin is pulled low to high.
15	DATAIN	I	Transmit data input to the receive BPF.
16	V_{DD}	–	Supply voltage pin (+3.0 to +5.5 V).

MB87002 BLOCK DIAGRAM



FUNCTION DESCRIPTION

The timing generating section generates the clock signals required by the modulator and demodulator. The basic clock is generated by an internal oscillator and external crystal (3.6864 MHz).
Modulator uses a programmable DAC with a 6 bit resistor string. The MSKOUT output is 1200 Hz for input 1 and 1800 Hz for input 0 synchronized with transmit clock. Before the transmit signal is output, a fixed level of 1/2 V_{DD} is output by pulling the SEND pin low.
The demodulator is composed of a band–pass filter (BPF), a delay detection circuit, a low–pass filter (LPF), and a digital phase–locked loop (DPLL). The BPF removes noise components from the 1,200 Hz and 1,800 Hz receive signals from the BPFIN pin and consists of a 10th–order Chebyshev switched–capacitor filter (SCF). The delay detection circuit, after conversion of the BPF output from analog to digital in the waveform shaping circuit, regenerates data by delay detection. The noise components in the regenerated data are removed by the LPF. The LPF is a third–order Butterworth filter and removes noise components of 800 Hz or higher. The DPLL extracts the receive clock from the regenerated data. The regenerated data is output from the DATAOUT pin synchronized with the receive clock. The DPLL has a tendency to degrade the bit error rate when the pull–in time is shortened. This IC allows users to choose between two pull–in times. When the DPLLC pin is pulled low, the high–speed mode is selected. When pulled high, the low–speed mode is selected.
The on–chip 1/2 V_{DD} circuit supplies the reference voltage required by BPF, LPF, and waveform shaping circuits and reduces external circuitry and component count.

NOTE: Devices consisting of mixed analog and digital signal processing circuits are usually difficult to test. The MB87002 incorporates a test circuit which simplifiers independent testing of the BPF, delay detection circuit, LPF, and DPLL.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Pin name	Value			Unit
			Min	Typ	Max	
Power Supply Voltage	V_{DD}	V_{DD}	3.0	5.0	5.5	V
Input Voltage	V_{IN}	All input pins	0	–	V_{DD}	V
OSC1 Pin Load Capacitance	C_{OSC1}	OSC1	25	–	50	pF
OSC2 Pin Load Capacitance	C_{OSC2}	OSC2	25	–	50	pF
Analog Output Load Resistance	R_{MO}	MSKOUT	10	–	–	kΩ
Analog Output Load Capacitance	C_{MO}	MSKOUT	–	–	30	pF
Operating Temperature	T_A	–	–10	–	70	°C

ELECTRICAL CHARACTERISTICS

DC characteristics (V_{DD} = 4.5 ~ 5.5 V)

T_A = 25°C

Parameter	Symbol	Pin name	Condition	Value			Unit
				Min	Typ	Max	
Power Supply Current	I_{DD}	V_{DD}		–	4	8	mA
Digital Input Low Voltage	V_{IL}	RESET, SEND, DATAIN, DPLLC, R/TC, TEST		0	–	0.8	V
Digital Input High Voltage	V_{IH}	RESET, SEND, DATAIN, DPLLC, R/TC, TEST		2.2	–	V_{DD}	V
Digital Input Low Current	I_{IL}	SEND, DATAIN, DPLLC, R/TC	V_{IN} = GND	–10	–	0	µA
Digital Input High Current	I_{IH}	RESET, SEND, DATAIN, DPLLC, R/TC, TEST	V_{IN} = V_{DD}	0	–	10	µA
Pull–up Resistance	R_{PLU}	RESET, TEST		25	50	100	kΩ
Digital Output Low Voltage	V_{OL}	DATAOUT, CLOCK	I_{OL} = 2.0 mA	0	–	0.4	V
Digital Output High Voltage	V_{OH}	DATAOUT, CLOCK	I_{OH} = 1.0 mA	2.4	–	V_{DD}	V
Oscillator Frequency	OSC_{IN}	OSC1, OSC2		–	3.6864	–	MHz
Analog Input Resistance 1	R_{AIN1}	BPFIN	Input pin–1/2 V_{DD}	50	100	200	kΩ
Analog Input Voltage 1	V_{AIN1}	BPFIN		0.5	–	2.5	V_{P-P}
Analog Output Voltage 1	A_{OUT1}	MSKOUT	Operation	0.8	1.0	1.2	V_{P-P}
			Offset voltage in operation	1/2 V_{DD} –0.3	1/2 V_{DD}	1/2 V_{DD} +0.3	V
			RESET = Low	1/2 V_{DD} –0.3	1/2 V_{DD}	1/2 V_{DD} +0.3	V
Receive BPF Absolute Gain	ABS_1	–	Input frequency 1500 Hz	–1.0	0	1.0	dB
Receive BPF Frequency Characteristics	F_1	–	0–300 Hz 900–1200 Hz 1200–1800 Hz 1800–2100 Hz 3000–5000 Hz Reference frequency 1500 Hz	– –3.5 –1.0 –3.5 –	– – – – –	–40.0 – – – –30.0	dB dB dB dB dB
Receive LPF Cutoff Frequency	F_0	–	3 dB down	–	800	–	Hz
Receive LPF Absolute Gain	ABS_2	–	0 Hz < Input frequency ≤ 300 Hz	–	–6.0	–	dB

DC characteristics (V_{DD} = 3.0 ~ 4.5 V)

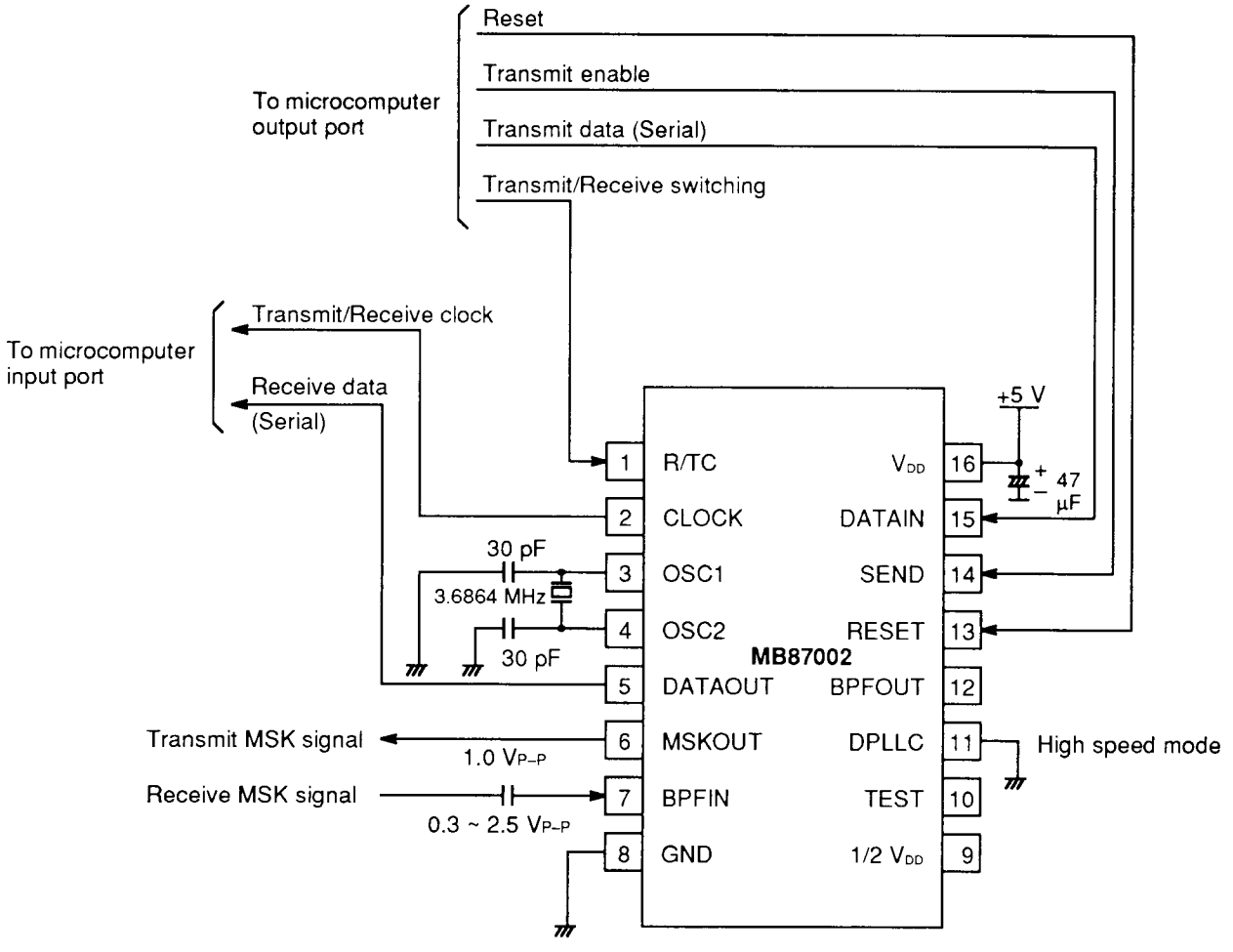
T_A = 25°C

Parameter	Symbol	Pin name	Condition	Value			Unit
				Min	Typ	Max	
Power Supply Current	I_{DD}	V_{DD}		–	–	8	mA
Digital Input Low Voltage	V_{IL}	RESET, SEND, DATAIN, DPLLC, R/TC, TEST		0	–	0.6	V
Digital Input High Voltage	V_{IH}	RESET, SEND, DATAIN, DPLLC, R/TC, TEST		2.2	–	V_{DD}	V
Digital Input Low Current	I_{IL}	SEND, DATAIN, DPLLC, R/TC	V_{IN} = GND	–10	–	0	µA
Digital Input High Current	I_{IH}	RESET, SEND, DATAIN, DPLLC, R/TC, TEST	V_{IN} = V_{DD}	0	–	10	µA
Pull–up Resistance	R_{PLU}	RESET, TEST		25	50	100	kΩ
Digital Output Low Voltage	V_{OL}	DATAOUT, CLOCK	I_{OL} = 0.5 mA	0	–	0.4	V
Digital Output High Voltage	V_{OH}	DATAOUT, CLOCK	I_{OH} = 0.5 mA	2.4	–	V_{DD}	V
Oscillator Frequency	OSC_{IN}	OSC1, OSC2		–	3.6864	–	MHz
Analog Input Resistance 1	R_{AIN1}	BPFIN	Input pin–1/2 V_{DD}	50	100	200	kΩ
Analog Input Voltage 1	V_{AIN1}	BPFIN		0.5	–	V_{DD} – 2.0	V_{P-P}
Analog Output Voltage 1	A_{OUT1}	MSKOUT	Operation	V_{DD} x 0.16	V_{DD} x 0.2	V_{DD} x 0.24	V_{P-P}
			Offset voltage in operation	1/2 V_{DD} –0.3	1/2 V_{DD}	1/2 V_{DD} +0.3	V
			RESET = Low	1/2 V_{DD} –0.3	1/2 V_{DD}	1/2 V_{DD} +0.3	V
Receive BPF Absolute Gain	ABS_1	–	Input frequency 1500 Hz	–2.0	0	2.0	dB
Receive BPF Frequency Characteristics	F_1	–	0–300 Hz 900–1200 Hz 1200–1800 Hz 1800–2100 Hz 3000–5000 Hz Reference frequency 1500 Hz	– –3.5 –1.0 –3.5 – 	– – – – – 	–30.0 – – – –25.0 	dB dB dB dB dB
Receive LPF Cutoff Frequency	F_0	–	3 dB down	–	800	–	Hz
Receive LPF Absolute Gain	ABS_2	–	0 Hz < Input frequency ≤ 300 Hz	–	–6.0	–	dB

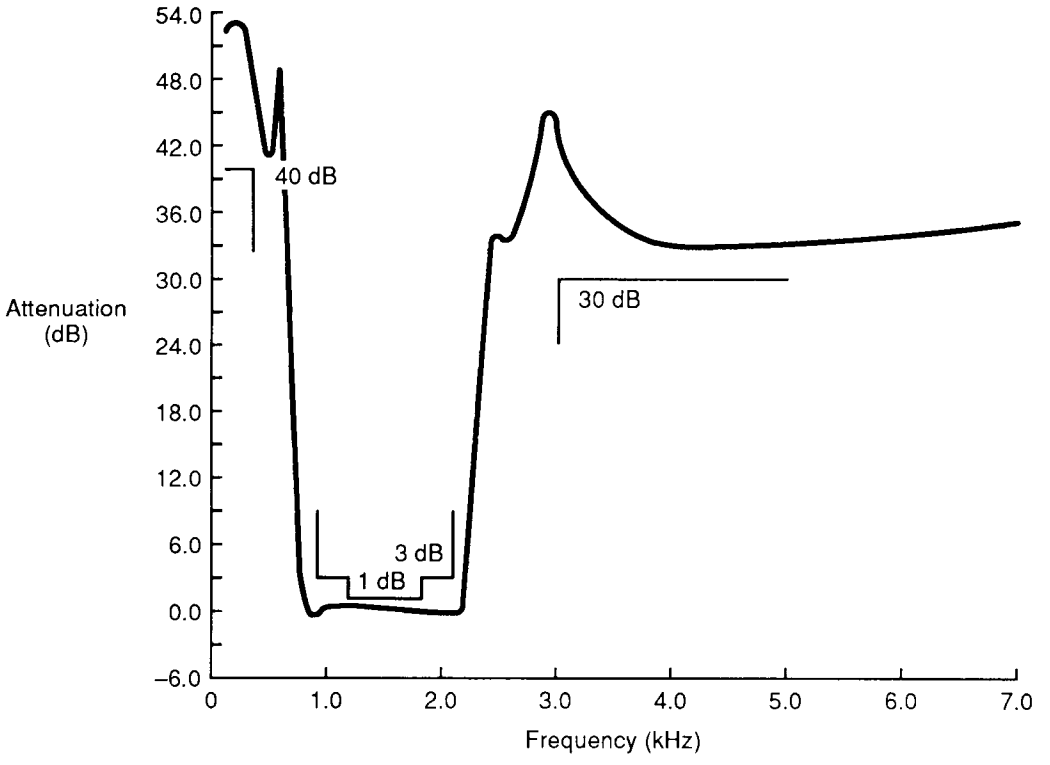
AC characteristics (V_{DD} = 3.0 ~ 5.5 V)

Parameter	Symbol	Pin name	Condition	Value			Unit
				Min	Typ	Max	
Transmit Clock Delay Time 1	t_{dRCH}	CLOCK	R/TC = "H"	0	150	417	µs
Transmit Clock Delay Time 2	t_{dSCH}	CLOCK	R/TC = "H"	417	570	834	µs
Transmit Clock Delay Time 3	t_{dSCL}	CLOCK	R/TC = "H"	0	150	417	µs
Transmit Clock High Width	t_{wHC1}	CLOCK	R/TC = "H"	390	417	444	µs
Transmit Clock Low Width	t_{wLC1}	CLOCK	R/TC = "H"	390	417	444	µs
SEND Setup Time	t_{SSC}	SEND	R/TC = "H"	1	–	–	µs
SEND Hold Time	t_{hSC}	SEND	R/TC = "H"	1	–	–	µs
DATAIN Setup Time	t_{SDC}	DATAIN	R/TC = "H"	1	–	–	µs
DATAIN Hold Time	t_{hDC}	DATAIN	R/TC = "H"	1	–	–	µs
MSKOUT Output Delay Time 1	t_{dCM1}	MSKOUT	R/TC = "H"	–	–	10	µs
MSKOUT Output Delay Time 2	t_{dCM2}	MSKOUT	R/TC = "H"	–	–	10	µs
BPFIN Invalid Time	t_{dRB}	BPFIN		0	–	10	ms
Pull–in Bit Number	N	–	R/TC = "L", DPLLC = "L", BPFIN: No noise	–	–	15	bit
Demodulator Delay Time	t_{dBD}	DATAOUT	R/TC = "L", DPLLC = "L", N ≥ 15 BPFIN: No noise	1483	1900	2317	µs
DATAOUT Timing	t_{dCD}	DATAOUT	R/TC = "L"	–1	–	1	µs
Receive Clock High Width	t_{wHC2}	CLOCK	R/TC = "L", DPLLC = "L", N ≥ 15 BPFIN: No noise	338	417	496	µs
Receive Clock Low Width	t_{wLC2}	CLOCK	R/TC = "L", DPLLC = "L", N ≥ 15 BPFIN: No noise	338	417	496	µs
RESET Low Width	t_{wLR}	RESET		20	–	–	µs
MSKOUT Output Delay Time 3	t_{dRM}	MSKOUT		0	–	10	µs
Transmit Clock Delay Time 4	t_{dTC4}	CLOCK		0	–	2	µs
Receive Clock Delay Time 1	t_{dRC1}	CLOCK		0	–	2	µs

TYPICAL CONNECTION EXAMPLE

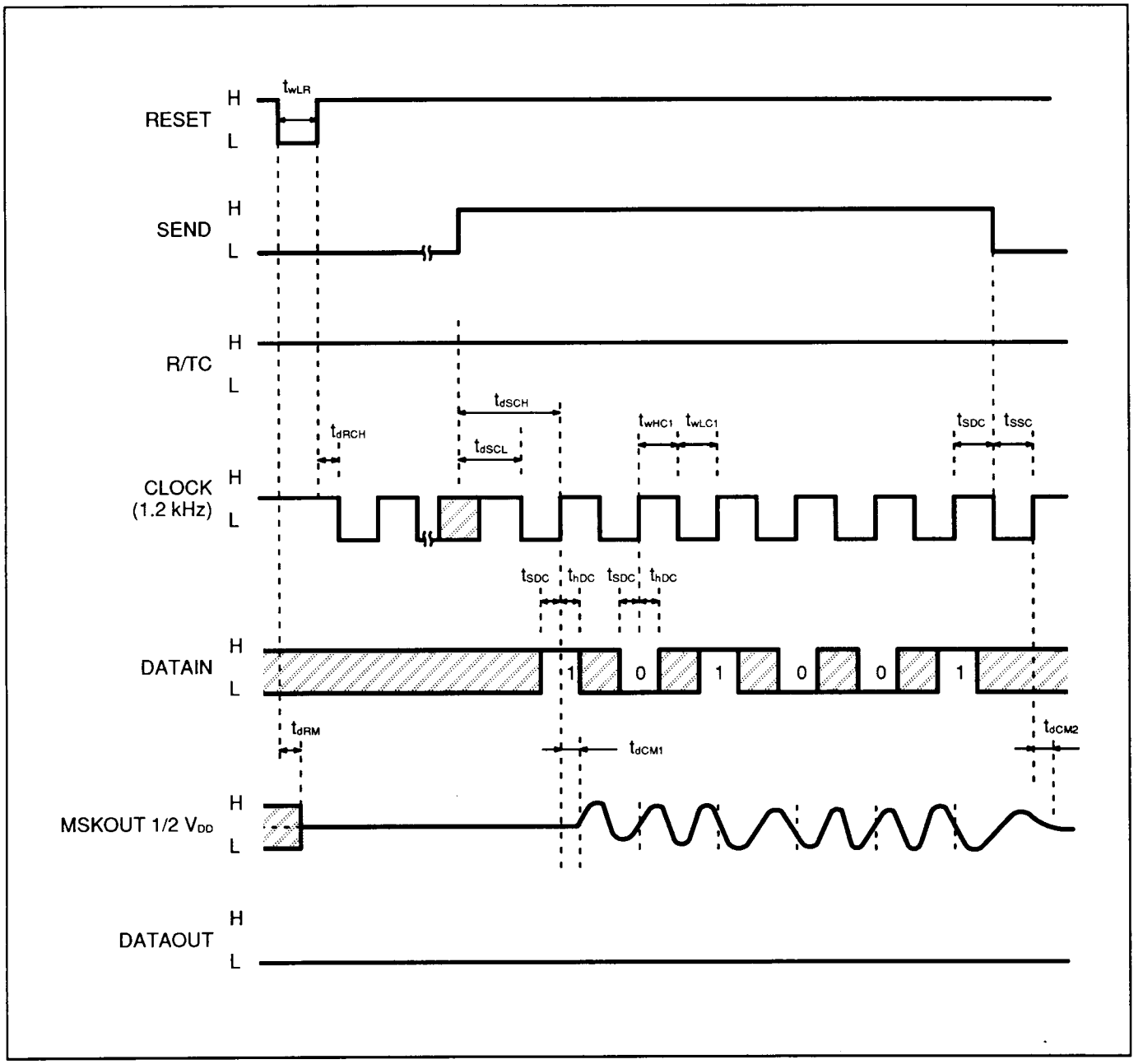


BPF FREQUENCY CHARACTERISTICS



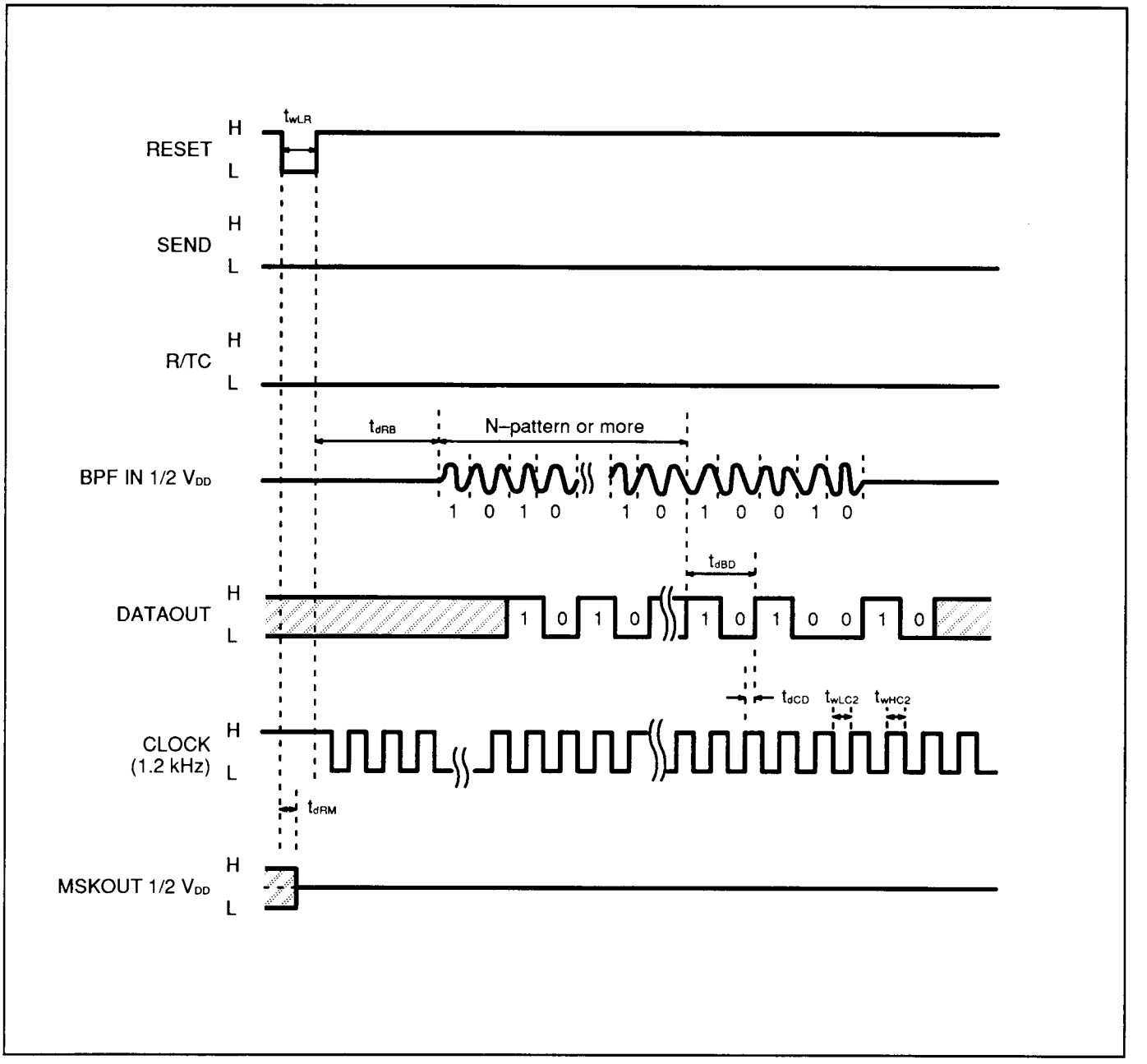
TIMING CHART

Modulator timing chart (TEST pin = High or Open)



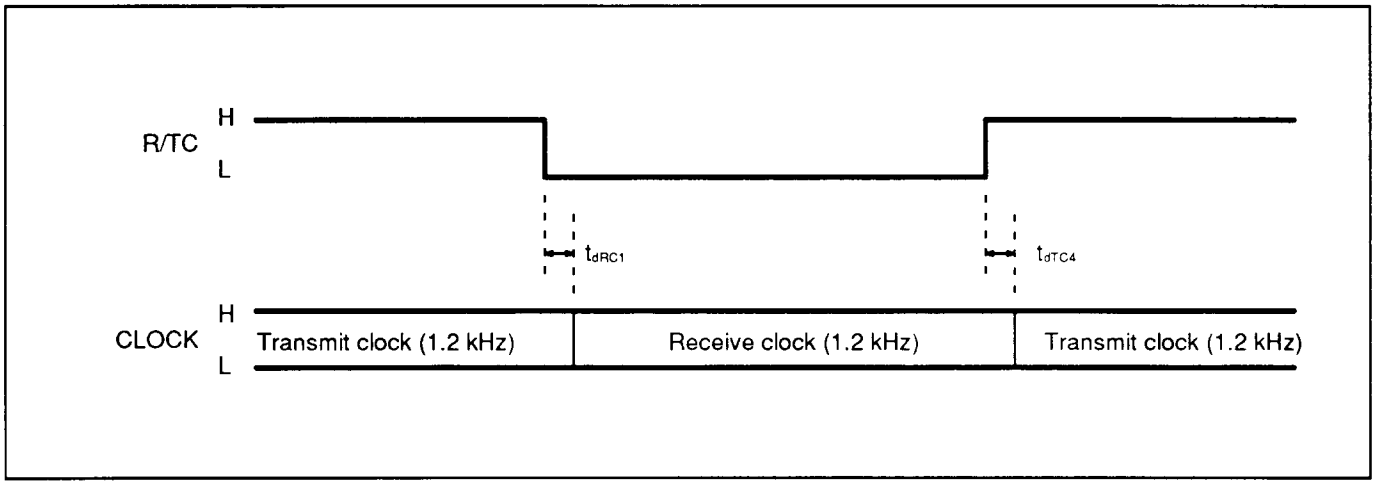
NOTE: 1. SEND pin is pulled high after low–to–high transition of the RESET pin.
2. DATAIN signal is read at the rising edge of the CLOCK.
3. When SEND pin changes from low to high, the CLOCK pin is pulled high once. Then 1.2 kHz clock is output.
4. When R/TC pin is pulled high, DATAOUT pin outputs low.
5. When power is first applied, RESET pin must be set to low to rest all circuits before use.

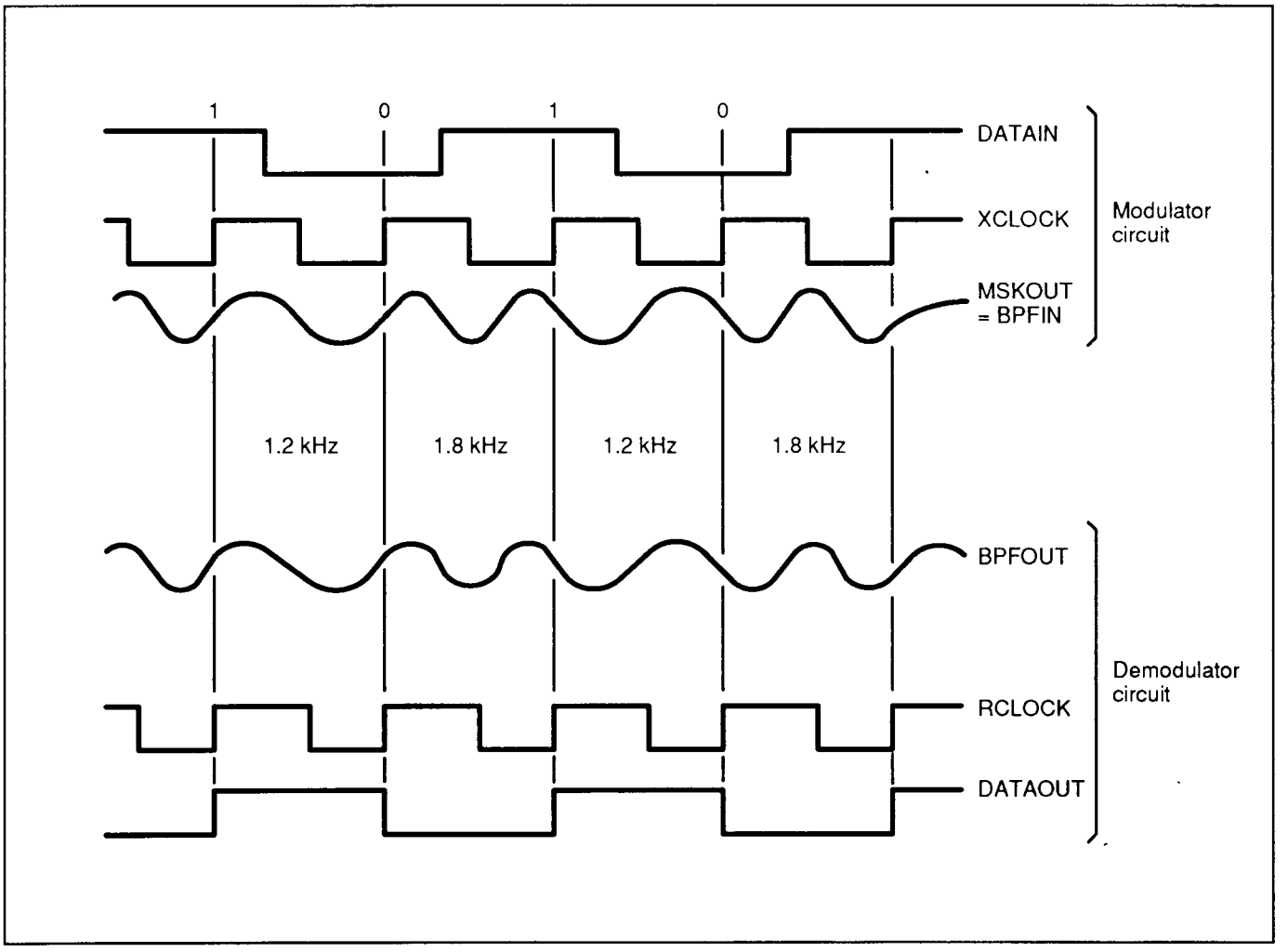
Demodulator timing chart (TEST pin = High or Open)



NOTE: 1. DATAOUT is output synchronized with the rising edge of the CLOCK.
2. When demodulator section is used, SEND pin must be set to high or low. When SEND pin is set to low, MSKOUT is fixed to 1/2 V_{DD}.
3. When power is first applied, RESET pin must be set to low to reset all circuits before use.

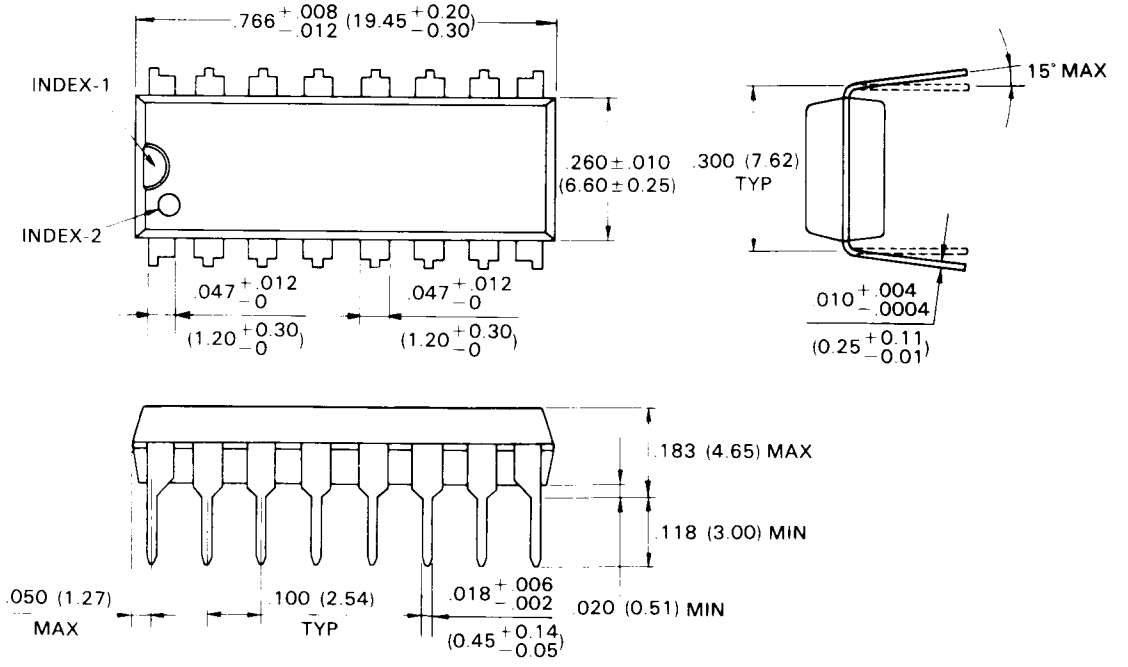
Clock output timing chart





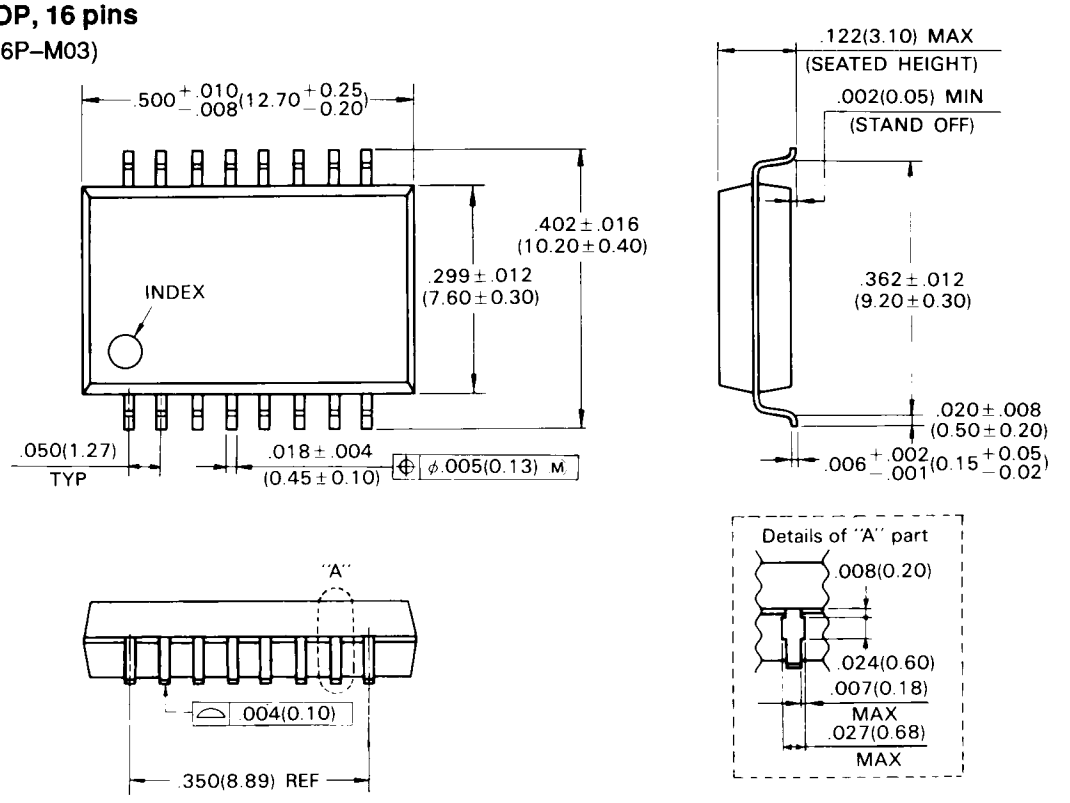
PACKAGE DIMENSIONS

Plastic DIP, 16 pins
(DIP–16P–M03)



Units: mm (inches)

Plastic SOP, 16 pins
(FPT–16P–M03)



Units: mm (inches)