

STRH40N25FSY3

N-channel 250V - 0.084Ω - TO-254AA Rad-hard low gate charge STripFET™ Power MOSFET

PRELIMINARY DATA

Features

Туре	V _{DSS}
STRH40N25FSY3	250V

- Low R_{DS(on)}
- Fast switching
- Single event effect (SEE) hardened
- Low total gate charge
- Light weight
- 100% avalanche tested
- Application oriented characterization
- Hermetically sealed
- Heavy ion SOA
- 100kRad TID
- SEL & SEGR with 34Mev/cm²/mg LET ions

Description

This Power MOSFET series realized with STMicroelectronics unique STripFET process has specifically been designed to improve immunity to space effect. It is therefore suitable as power switch in mainly high-efficiency DC-DC converters and Motor Control applications. It is also intended for any application with low gate charge drive requirements.

Applications

- Satellite
- High reliability applications

Order codes

Part number	Marking	Package	Packaging
STRH40N25FSY1 ⁽¹⁾	RH40N25FSY1	TO-254AA	Individual strip pack
STRH40N25FSY3 ⁽²⁾	RH40N25FSY3	TO-254AA	Individual strip pack

1. Mil temp range

2. Space flights parts (full ESA flow screening)

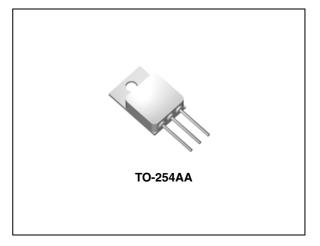
March 2007

Rev 2

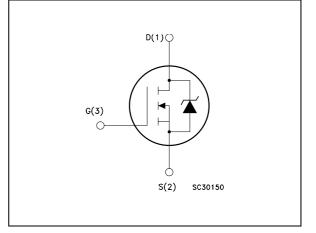


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This is preliminary information on a new product now in development or undergoing evaluation. Details are subject to change without notice.



Internal schematic diagram



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1 Electrical ratings

Symbol	Parameter	Value	Unit
V _{DS}	Drain-source voltage (V _{GS} = 0)	250	V
V _{GS}	Gate-source voltage	±16	V
I _D ⁽¹⁾	Drain current (continuous) at $T_C = 25^{\circ}C$	36	А
I _D ⁽¹⁾	Drain current (continuous) at T _C = 100°C	23	А
I _{DM} ⁽²⁾	Drain current (pulsed)	144	Α
$P_{TOT}^{(1)}$	Total dissipation at T_{C} = 25°C	278	W
dv/dt ⁽³⁾	Peak diode recovery voltage slope	4	V/ns
T _{stg}	Storage temperature	-55 to 150	°C
Тj	Max. operating junction temperature	150	°C

Table 1.	Absolute	maximum	ratings	(pre-irradiation	١
	Absolute	maximum	raunyə	(pre-intaulation	

1. Rated according to the Rthj-case

2. Pulse width limited by safe operating area

3. $I_{SD} \le 40A$, di/dt $\le 400A/\mu s$, $V_{DD} = 80\% V_{(BR)DSS}$

Symbol	Parameter	Value	Unit
Rthj-case	Thermal resistance junction-case	0.45	°C/W
Rthc-s	Case-to-sink	0.21	°C/W
Rthj-amb	Thermal resistance junction -amb	48	°C/W

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
I _{AR}	Avalanche current, repetitive or not-repetitive (pulse width limited by Tj Max)	40	А
E _{AS}	Single pulse avalanche energy (starting Tj=25°C, Id=Iar, Vdd=50V)	320	mJ
E _{AR}	Repetitive avalanche	25	mJ



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2 Electrical characteristics

(T_{CASE} = 25°C unless otherwise specified)

2.1 Pre-irradiation

	On/on states					
Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
I _{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	80% BV _{Dss}			10	μA
I _{GSS}	Gate body leakage current (V _{DS} = 0)	$V_{GS} = \pm 16V$			±100	nA
BV _{DSS}	Drain-to-source breakdown voltage	$I_D = 1mA, V_{GS} = 0V$	250			V
V _{GS(th)}	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 1mA$	2		4.5	۷
R _{DS(on)}	Static drain-source on resistance	V _{GS} = 12V, I _D = 20A		0.084	0.1	Ω

Table 4. On/off states

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
C _{iss} C _{oss} C _{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V _{DS} = 0V, f=1MHz, V _{GS} =12V		9100 650 45		pF pF pF
Q _g Q _{gs} Q _{gd}	Total gate charge Gate-to-source charge Gate-to-drain ("Miller") charge	V _{DD} = 200V, I _D = 40A, V _{GS} =12V		202 34 58	280 47 80	nC nC nC
R _G	Gate input resistance	f=1MHz Gate DC Bias=0 Test signal level=20mV open drain		1.4	3	Ω

Table 6.Switching times

Symbol	Parameter	Test conditions	Min.	Тур.	Max	Unit
t _{d(on)}	Turn-on delay time			33		ns
t _r	Rise time	V _{DD} = 125V, I _D =40 A,		80		ns
t _{d(off)}	Turn-off-delay time	R _G = 4.7Ω, V _{GS} = 12V		123		ns
t _f	Fall time			145		ns

Symbol	Parameter	Test conditions	Min.	Тур.	Max	Unit
I _{SD} I _{SDM} ⁽¹⁾	Source-drain current Source-drain current (pulsed)				36 144	A A
V _{SD} ⁽²⁾	Forward on voltage	$I_{SD} = 40A, V_{GS} = 0$			1.5	V
t _{rr} Q _{rr} I _{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I _{SD} = 40A, di/dt = 100A/µs V _{DD} = 50V, Tj = 150°C		484 8.4 35		ns μC Α

 Table 7.
 Source drain diode

1. Pulse width limited by safe operating area

2. Pulsed: pulse duration = 300µs, duty cycle 1.5%

2.2 Post-irradiation

The ST Rad-Hard Power MOSFETs are tested to verify the radiation capability. The technology is extremely resistant to assurance well functioning of the device inside the radiation environments. Every manufacturing lot is tested for total ionizing dose.

(@Tj=25°C up to 100Krad ^(a))

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
I _{DSS}	Zero gate voltage drain current $(V_{GS} = 0)$	80% BV _{Dss}			10	μA
I _{GSS}	Gate body leakage current (V _{DS} = 0)	$V_{GS} = \pm 16V$			±100	nA
BV _{DSS}	Drain-to-source breakdown voltage	$I_D = 1mA, V_{GS} = 0V$	250			V
V _{GS(th)}	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 1mA$	2		4.5	V
R _{DS(on)}	Static drain-source on resistance	V _{GS} = 12V, I _D = 20A		0.084	0.1	Ω

Table 8. On/off states



a. According to ESCC 22900 specification, Co60 gamma rays, dose rags:0.1rad/sec.

	Single event eneod, SOA				
lon	Let (Mev/(mg/cm2))	Energy (MeV)	Range (µm)	V _{DS} (V) @V _{GS} 0V	
Kr	34	316	43	250	
Xe	55.9	459	43	244	

Table 9. Single event effect. SOA⁽¹⁾

1. Rad-Hard Power MOSFETs have been characterized in heavy ion environment for single event effect (SEE). Single event effect characterization is illustrated

Table 10. Source drain diode

Symbol	Parameter	Test conditions	Min.	Тур.	Max	Unit
I _{SD} I _{SDM} ⁽¹⁾	Source-drain current Source-drain current (pulsed)				36 144	A A
V _{SD} ⁽²⁾	Forward on voltage	I _{SD} = 40A, V _{GS} = 0			1.5	V
t _{rr} Q _{rr} I _{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I _{SD} = 40A, di/dt = 100A/µs V _{DD} = 50V, Tj = 150°C		484 8.4 35		ns μC Α

1. Pulse width limited by safe operating area

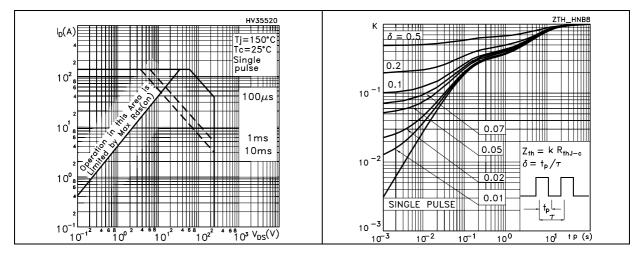
2. Pulsed: pulse duration = $300\mu s$, duty cycle 1.5%



2.3 Electrical characteristics (curves)

Figure 1. Safe operating area

Figure 2. Thermal impedance



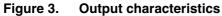
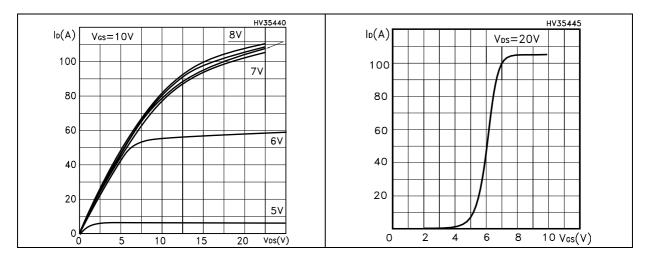


Figure 4. Transfer characteristics



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Figure 5. Gate charge vs. gate-source voltage

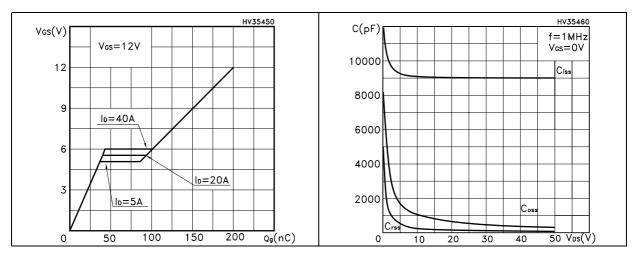
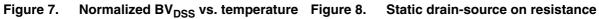


Figure 6. Capacitance variations



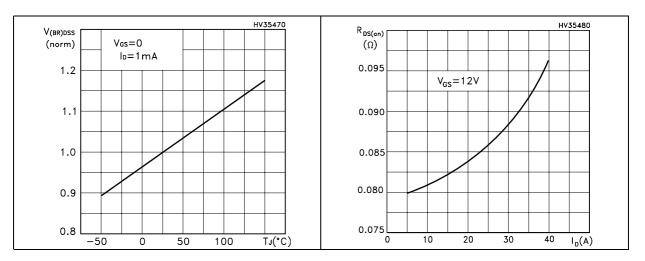
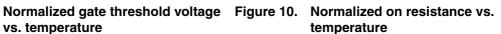


Figure 9. vs. temperature



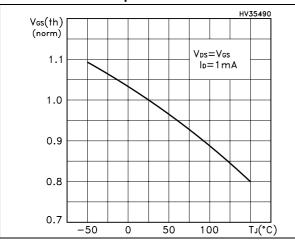
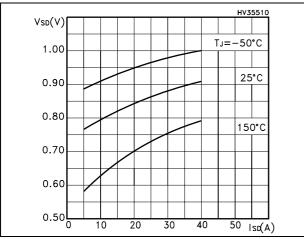
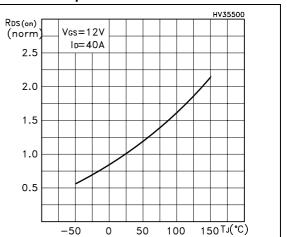


Figure 11. Source drain-diode forward characteristics





3 Test circuit

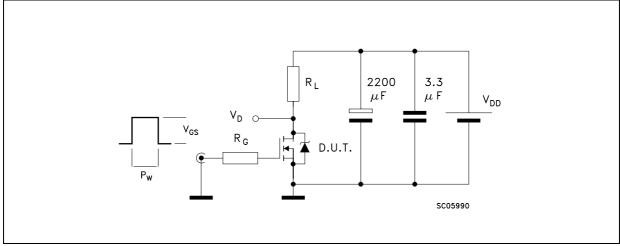


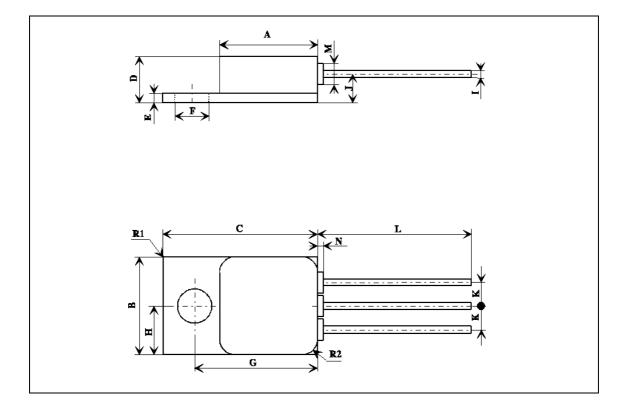
Figure 12. Switching times test circuit for resistive load ⁽¹⁾

1. Max driver V_{GS} slope = 1V/ns (no DUT)



4 Package mechanical data

DIM.	mm.			inch		
Diwi.	MIN.	ТҮР	MAX.	MIN.	TYP.	MAX.
А	13.59		13.84	0.535		0.545
В	13.59		13.84	0.535		0.545
С	20.07		20.32	0.790		0.80
D	6.32		6.60	0.249		0.260
E	1.02		1.27	0.040		0.050
F	3.53		3.78	0.139		0.149
G	16.89		17.40	0.665		0.685
Н		6.86			0.270	
I	0.89		1.14	0.035		0.045
J		3.81			0.150	
К		3.81			0.150	
L	12.95		14.50	0.510		0.570
М		3.05			0.120	
Ν			0.71			0.025
R1			1.0			0.040
R2		1.65			0.065	



TO-254AA MECHANICAL DATA

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5 Revision history

Table 11.	Revision	history
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Date	Revision	Changes
18-Dec-2006	1	First release
02-Mar-2007	2	Some values changed on Table 4 and Table 8



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