

Low Profile Fast Infrared Transceiver (FIR, 4 Mbit/s) for IrDA® Applications



Description

The TFBS6711 is the smallest FIR transceiver available. It is a low profile and low-power IrDA transceiver. Compliant to IrDA's Physical Layer specification, the TFBS6711 supports data transmission rates from 9.6 kbit/s to 4 Mbit/s with a typical link distance of 50 cm. It also enables mobile phones and PDAs to function as universal remote controls for televisions, DVDs and other home appliances. The TFBS6711 emitter covers a range of 6.5 meters with common remote control receivers. Integrated within the transceiver module is a PIN photodiode, an infrared emitter, and a low-power control IC. The TFBS6711 can be completely shutdown, achieving very low power consumption. The TFBS6711 has an I/O voltage



related to the supply voltage while TFBS6712 supports low voltage logic of 1.8 V allowing direct connection to a microcontroller's I/Os operating at 1.8 V.

Features

- Lowest profile: 1.9 mm
- Smallest footprint: 6.0 mm x 3.05 mm
- Surface mount package
- IrDA transmit distance: 50 cm typical
- Best Remote Control distance: ≥ 6.5 m on-axis
- Fast data rates: from 9.6 kbit/s to 4 Mbit/s
- Low shutdown current: 0.01 μ A
- Operating Voltage: 2.4 V to 3.6 V
- Reduced pin count: 6 pins
- I/O voltage equal to the supply voltage
- Pin compatibility: TFBS4711 and TFBS5711
- Integrated EMI Protection – no external shield required



- IEC 60825-1 Class 1, Eye Safe
- Qualified for lead (Pb)-free and Sn/Pb processing
- Compliant to IrDA Physical Layer Specification
- Split power supply, transmitter and receiver can be operated from two power supplies with relaxed requirements saving costs, US patent No. 6,157,476
- Lead (Pb)-free device
- Qualified for lead (Pb)-free and Sn/Pb processing (MSL4)
- Device in accordance with RoHS 2002/95/EC and WEEE 2002/96/EC

Applications

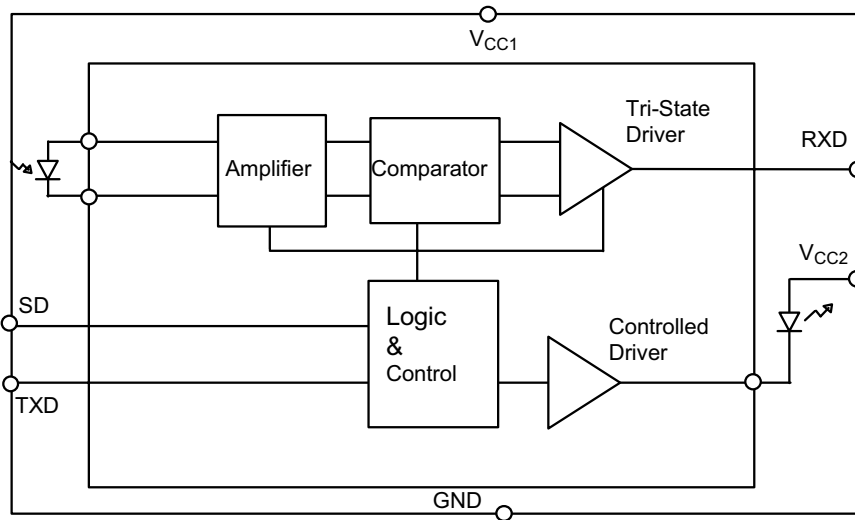
- High-speed data transfer using infrared wireless communication
- Mobile phones
- Camera phones
- PDAs
- MP3 Players
- Digital Cameras
- IrDA Adapters or Dongles

Package Options

Ordering Information

| Part Number | Qty/Reel or Tube | Description and Remarks |
|--------------|------------------|---|
| TFBS6711-TR1 | 1000 pcs | Oriented in carrier tape for side view surface mounting |
| TFBS6711-TR3 | 2500 pcs | Oriented in carrier tape for side view surface mounting |

Note: A version oriented in the carrier tape for top view mounting is available on request

Functional Block Diagram


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Figure 1. Functional Block Diagramm

Pin Description

| Pin Number | Function | Description | I/O | Active |
|------------|-------------------------------|---|-----|--------|
| 1 | V _{CC2} , IRED Anode | IRED anode to be externally connected to V _{CC2} . For higher voltages as 3.6 V an external resistor might be necessary for reducing the internal power dissipation. See derating curves. This pin is allowed to be supplied from an uncontrolled power supply separated from the controlled V _{CC1} - supply | | |
| 2 | TXD | Transmit Data Input | I | HIGH |
| 3 | RXD | Received Data Output, push-pull CMOS driver output capable of driving a standard CMOS load. No external pull-up or pull-down resistor is required. Floating with a weak pull-up of 500 kΩ (typ.) in shutdown mode. The RXD output echos the TXD input during transmission. | O | LOW |
| 4 | SD | Shutdown, also used for dynamic mode switching | I | HIGH |
| 5 | V _{CC1} | Supply voltage | | |
| 6 | GND | Ground | | |

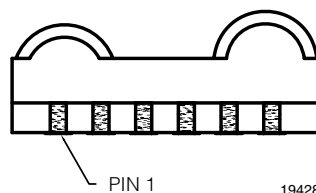
 TFBS6711
 Weight: 50 mg


Figure 2. Pinning

Absolute Maximum Ratings

Reference point Pin, GND unless otherwise noted.

Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

| Parameter | Test Conditions | Symbol | Min | Typ. | Max | Unit |
|---|---------------------------------------|-----------------|-------|------|------------------------------------|-------|
| Supply voltage range, transceiver | $0\text{ V} < V_{CC2} < 6\text{ V}$ | V_{CC1} | - 0.5 | | 6 | V |
| Supply voltage range, transmitter | $0\text{ V} < V_{CC1} < 6\text{ V}$ | V_{CC2} | - 0.5 | | 6.5 | V |
| Input currents | For all Pins, Except IRED Anode Pin | | | | 10 | mA |
| Output sinking current | | | | | 25 | mA |
| Power dissipation | | P_D | | | 500 | mW |
| Junction temperature | | T_J | | | 125 | °C |
| Ambient temperature range (operating) | | T_{amb} | - 25 | | + 85 | °C |
| Storage temperature range | | T_{stg} | - 25 | | + 85 | °C |
| Soldering temperature | | | | | 260 | °C |
| Average output current | | $I_{IRED (DC)}$ | | | 125 | mA |
| Repetitive pulse output current | $< 90\ \mu\text{s}$, $t_{on} < 20\%$ | $I_{IRED (RP)}$ | | | 600 | mA |
| IRED anode voltage | | I_{IREDA} | - 0.5 | | 6.5 | V |
| Voltage at all inputs and outputs | $V_{in} > V_{CC1}$ is allowed | V_{in} | - 0.5 | | 5.5 | V |
| Virtual source size | Method: (1-1/e) encircled energy | d | 1.5 | | | mm |
| Maximum Intensity for Class 1 operation of IEC60825-1 or EN60825-1, edition Jan. 2001 | | | | | internal limitation to class 1 500 | mW/sr |
| IrDA® specified maximum limit | | | | | | |
| Due to the internal limitation measures the device is a "class 1" device. It will not exceed the IrDA® intensity limit of 500 mW/sr | | | | | | |

Definitions:

In the Vishay transceiver data sheets the following nomenclature is used for defining the IrDA operating modes:

SIR: 2.4 kbit/s to 115.2 kbit/s, equivalent to the basic serial infrared standard with the physical layer version IrPhy 1.0

MIR: 576 kbit/s to 1152 kbit/s

FIR: 4 Mbit/s

VFIR: 16 Mbit/s

IrDA®, the Infrared Data Association, implemented MIR and FIR with IrPHY 1.1, followed by IrPhy 1.2, adding the SIR Low Power Standard. IrPhy 1.3 extended the Low Power Option to MIR and FIR and VFIR was added with IrPhy 1.4. A new version of the standard in any case obsoletes the former version.



Electrical Characteristics

$T_{amb} = 25\text{ }^{\circ}\text{C}$, $V_{CC} = 2.4\text{ V}$ to 3.6 V unless otherwise noted.

Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

| Parameters | Test Conditions/Pins | Symbol | Min | Typ. | Max | Unit |
|---------------------------------|---|-----------|---------------------|------|----------------|--------------------|
| Transceiver | | | | | | |
| Supply voltage | | V_{CC} | 2.4 | | 3.6 | V |
| Dynamic supply current | Receive mode only. In transmit mode, add additional 85 mA (typ) for IRED current. Add RXD output current depending on RXD load. | | | | | |
| | SD = Low, SIR mode | I_{CC} | | 1.7 | 3 | mA |
| | SD = Low, MIR/FIR mode | I_{CC} | | 1.9 | 3.3 | mA |
| Shutdown supply current | SD = High $T = 25\text{ }^{\circ}\text{C}$, not ambient light sensitive, detector is disabled in shutdown mode | I_{SD} | | | 1 | μA |
| | SD = High $T = 85\text{ }^{\circ}\text{C}$, not ambient light sensitive | I_{SD} | | | 5 | μA |
| Operating temperature range | | T_A | - 25 | | + 85 | $^{\circ}\text{C}$ |
| Output voltage low | $I_{OL} = 1\text{ mA}$ $C_{LOAD} = 15\text{ pF}$ | V_{OL} | | | 0.4 | V |
| Output voltage high | $I_{OH} = - 250\text{ }\mu\text{A}$ $C_{LOAD} = 15\text{ pF}$ | V_{OH} | $0.9 \times V_{CC}$ | | | V |
| Internal RXD pull-up | | R_{RXD} | 400 | 500 | 600 | $\text{k}\Omega$ |
| Input voltage low (TXD, SD) | | V_{IL} | - 0.5 | | 0.5 | V |
| Input voltage high (TXD, SD) | | V_{IH} | $V_{CC} - 0.5$ | | $V_{CC} + 0.5$ | V |
| Input leakage current (TXD, SD) | | I_{ICH} | - 1 | 0.05 | + 1 | μA |
| Input capacitance (TXD, SD) | | C_I | | | 5 | pF |

^{*)} Standard illuminant A

^{**)} The typical threshold level is $0.5 \times V_{CC}$ ($V_{CC} = 3\text{ V}$). It is recommended to use the specified min/max values to avoid increased operating/shutdown currents.

Optoelectronic Characteristics

T_{amb} = 25 °C, V_{CC} = 2.4 V to 3.6 V unless otherwise noted.

Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

| Parameter | Test Conditions | Symbol | Min | Typ. | Max | Unit |
|--|--|----------------------|------------|-------------|-----------------|--|
| Receiver | | | | | | |
| Minimum irradiance E _e in angular range **) | 9.6 kbit/s to 115.2 kbit/s λ = 850 nm - 900 nm, V _{CC} = 2.4 V | E _e | | 50 (5) | 80 (8) | mW/m ² (μW/cm ²) |
| Minimum irradiance E _e in angular range MIR mode | 1.152 Mbit/s λ = 850 nm - 900 nm, V _{CC} = 2.4 V | E _e | | 100 (10) | | mW/m ² (μW/cm ²) |
| Minimum irradiance E _e in angular range FIR mode | 4 Mbit/s λ = 850 nm - 900 nm, V _{CC} = 2.4 V | E _e | | 120 (12) | 200 (20) | mW/m ² (μW/cm ²) |
| Maximum irradiance E _e in angular range ***) | λ = 850 nm - 900 nm | E _e | | 5 (500) | | kW/m ² (mW/cm ²) |
| No detection receiver Input Irradiance (fluorescent light noise suppression) | | E _e | 4 (0.4) | | | mW/m ² (μW/cm ²) |
| Rise time of output signal | 10 % to 90 %, C _L = 15 pF | t _r (RXD) | 10 | | 50 | ns |
| Fall time of output signal | 90 % to 10 %, C _L = 15 pF | t _f (RXD) | 10 | | 50 | ns |
| RXD pulse width of output signal, 50 %, SIR mode | Input pulse length 1.4 μs < P _{Wopt} < 25 μs | t _{PW} | 1.4 | 1.8 | 2.6 | μs |
| RXD pulse width of output signal, 50 %, MIR mode | Input pulse length P _{Wopt} = 217 ns, 1.152 Mbit/s | t _{PW} | 110 | 250 | 270 | ns |
| RXD pulse width of output signal, 50 %, FIR mode | Input pulse length P _{Wopt} = 125 ns, 4 Mbit/s | t _{PW} | 110 | | 140 | ns |
| RXD pulse width of output signal, 50 %, FIR mode | Input pulse length P _{Wopt} = 250 ns, 4 Mbit/s | t _{PW} | 225 | | 275 | ns |
| RXD output jitter, leading edge | Input irradiance = 150 mW/m ² , 4 Mbit/s 1.152 Mbit/s ≤ 115.2 kbit/s | | | | 20 40 350 | ns ns ns |
| Receiver start up time | After completion of shutdown programming sequence Power on delay | | | | 500 | μs |
| Latency ^{*)} | | t _L | | | 100 | μs |

Note: All timing data measured with 4 Mbit/s are measured using the IrDA® FIR transmission header. The data given here are valid 5 μs after starting the preamble.

^{*)} **IrDA latency definition:** Receiver **Latency** Allowance (milliseconds or microseconds) is the maximum time after a node ceases transmitting before the node's receiver recovers its specified sensitivity. During this period and also during the receiver start up time (after power on or shut down) the RXD output may be in an undefined state.

^{**) IrDA sensitivity definition: Minimum Irradiance E_e In Angular Range}, power per unit area. The receiver must meet the BER specification while the source is operating at the minimum intensity in angular range into the minimum half-angle range at the maximum Link Length

^{***) Maximum Irradiance E_e In Angular Range}, power per unit area. The optical delivered to the detector by a source operating at the maximum intensity in angular range at Minimum Link Length must not cause receiver overdrive distortion and possible related link errors. If placed at the Active Output Interface reference plane of the transmitter, the receiver must meet its bit error ratio (BER) specification.

For more definitions see the document "Symbols and Terminology" on the Vishay Website (<http://www.vishay.com/docs/82512/82512.pdf>).



Optoelectronic Characteristics, continued

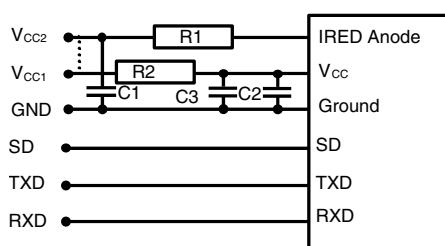
T_{amb} = 25 °C, V_{CC} = 2.4 V to 3.6 V unless otherwise noted.

Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

| Parameter | Test Conditions | Symbol | Min | Typ. | Max | Unit |
|--|--|--|-----|------|------|----------|
| IRED operating current, switched current control | For 3.3-V operation no external resistor is needed. | I _D | 330 | 440 | 600 | mA |
| Output leakage IRED current | V _{CC} = V _{IRED} = 3.3 V, TXD = Low | I _{IRED} | - 1 | | 1 | μA |
| Output radiant intensity, s. figure 3, recommended application circuit | V _{CC} = V _{IRED} = 3.3 V, α = 0° TXD = High, SD = Low, R ₁ = 1 Ω | I _e | 45 | 115 | 300 | mW/sr |
| Output radiant intensity, s. figure 3, recommended application circuit | V _{CC} = V _{IRED} = 3.3 V, α = 0°, 15° TXD = High, SD = Low, R ₁ = 1 Ω | I _e | 25 | 75 | 300 | mW/sr |
| Output radiant intensity | V _{CC1} = 3.6 V, α = 0°, 15° TXD = Low or SD = High (Receiver is inactive as long as SD = High) | I _e | | | 0.04 | mW/sr |
| Output radiant intensity, angle of half intensity | | α | | ± 24 | | ° |
| Peak - emission wavelength | | λ _p | 880 | | 900 | nm |
| Optical rise time, Optical fall time | | t _{ropt} , t _{fopt} | 10 | | 40 | ns |
| Optical output pulse duration | Input pulse width 217 ns, 1.152 Mbit/s | t _{opt} | 200 | 217 | 230 | ns |
| Optical output pulse duration | Input pulse width 125 ns, 4 Mbit/s | t _{opt} | 116 | 125 | 134 | ns |
| Optical output pulse duration | Input pulse width 250 ns, 4 Mbit/s | t _{opt} | 241 | 250 | 259 | ns |
| Optical output pulse duration | Input pulse width t < 80 μs Input pulse width t ≥ 80 μs | t _{opt} t _{opt} | 20 | t | 85 | μs μs |
| Optical overshoot | | | | | 25 | % |

Recommended Circuit Diagram

Operated at a clean low impedance power supply the TFBS6711 needs no additional external components. However, depending on the entire system design and board layout, additional components may be required (see figure 3).



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Figure 3. Recommended Application Circuit

The capacitor C1 is buffering the supply voltage and eliminates the inductance of the power supply line. This one should be a Tantalum or other fast capacitor to guarantee the fast rise time of the IRED current.

Vishay transceivers integrate a sensitive receiver and a built-in power driver. The combination of both needs a careful circuit board layout. The use of thin, long, resistive and inductive wiring should be avoided. The inputs (RXD, SD) and the output RXD should be directly (DC) coupled to the I/O circuit.

The capacitor C2 combined with the resistor R2 is the low pass filter for smoothing the supply voltage.

R2, C1 and C2 are optional and dependent on the quality of the supply voltages V_{CCx} and injected noise. An unstable power supply with dropping voltage during transmission may reduce the sensitivity (and transmission range) of the transceiver.

The placement of these parts is critical. It is strongly recommended to position C2 as close as possible to the transceiver power supply pins.

A Tantalum capacitor should be used for C1 while a ceramic capacitor is used for C2.

In addition, when connecting the described circuit to the power supply, low impedance wiring should be used.

When extended wiring is used the inductance of the power supply can cause dynamically a voltage drop at V_{CC2}. Often some power supplies are not able to follow the fast current rise time. In that case another 4.7 μF (type, see table under C1) at V_{CC2} will be helpful.

Keep in mind that basic RF-design rules for circuit design should be taken into account. Especially longer signal lines should not be used without termination. See e.g. "The Art of Electronics" Paul Horowitz, Winfield Hill, 1989, Cambridge University Press, ISBN: 0521370957.

Table 1. Recommended Application Circuit Components

| Component | Recommended Value |
|-----------|---|
| C1 | 4.7 μF, 16 V Vishay part#: 293D 475X9 016B |
| C2 | 0.1 μF, Ceramic Vishay part#: VJ1206 Y 104 J XXMT |
| R1 | 3.3 V supply voltage: no resistor is necessary, the internal controller is able to control the current |
| R2 | 4.7 Ω, 0.125 W |

I/O and Software

In the description, already different I/Os are mentioned. Different combinations are tested and the function verified with the special drivers available from the I/O suppliers. In special cases refer to the I/O manual, the Vishay application notes, or contact directly Vishay Sales, Marketing or Application.

Mode Switching

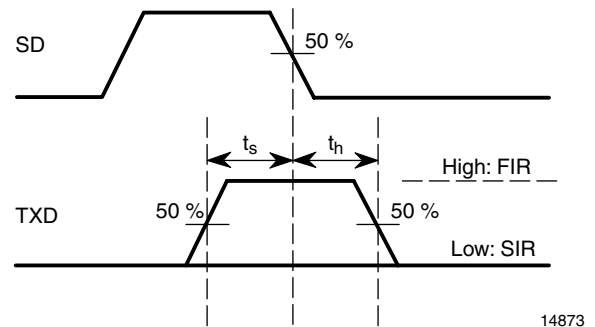
The TFBS6711 is in the SIR mode after power on as a default mode, therefore the FIR data transfer rate has to be set by a programming sequence using the TXD and SD inputs as described below. The low frequency mode covers speeds up to 115.2 kbit/s. Signals with higher data rates should be detected in the high frequency mode. Lower frequency data can also be received in the high frequency mode but with reduced sensitivity. To switch the transceivers from low frequency mode to the high frequency mode and vice versa, the programming sequences described below are required.

Setting to the High Bandwidth Mode (0.576 Mbit/s to 4 Mbit/s)

1. Set SD input to logic "HIGH".
2. Set TXD input to logic "HIGH". Wait $t_s \geq 200$ ns.
3. Set SD to logic "LOW" (this negative edge latches state of TXD, which determines speed setting).
4. After waiting $t_h \geq 200$ ns TXD can be set to logic "LOW". The hold time of TXD is limited by the maximum allowed pulse length. TXD is now enabled as normal TXD input for the high bandwidth mode.

Setting to the Lower Bandwidth Mode (2.4 kbit/s to 115.2 kbit/s)

1. Set SD input to logic "HIGH".
2. Set TXD input to logic "LOW". Wait $t_s \geq 200$ ns.
3. Set SD to logic "LOW" (this negative edge latches state of TXD, which determines speed setting).
4. TXD must be held for $t_h \geq 200$ ns. TXD is now enabled as normal TXD input for the lower bandwidth mode.



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Figure 4. Mode Switching Timing Diagram

Truth table

| Inputs | | | Outputs | |
|--------|-------------------------|--|--|-------------|
| SD | TXD | Input irradiance mW/m^2 | RXD | Transmitter |
| high | x | x | weakly pulled (500 $\text{k}\Omega$) high | 0 |
| low | high | x | low active (echo) | I_e |
| low | high > 80 μs | x | high | 0 |
| low | low | < 4 | high | 0 |
| low | low | > Min. irradiance E_e in angular range < Max. irradiance E_e in angular range | low (active) | 0 |
| low | low | > Max. irradiance E_e in angular range | x | 0 |

Recommended Solder Profiles

Solder Profile for Sn/Pb soldering

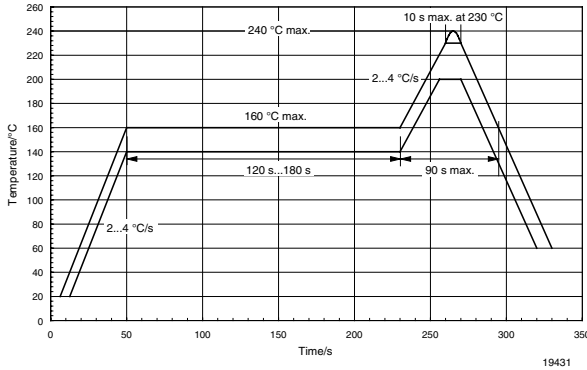


Figure 5. Recommended Solder Profile for Sn/Pb soldering

Lead (Pb)-Free, Recommended Solder Profile

The TFBS6711 is a lead (Pb)-free transistor and qualified for lead (Pb)-free processing. For lead (Pb)-free solder paste like Sn(3.0-4.0)Ag(0.5-0.9)Cu, there are two standard reflow profiles: Ramp-Soak-Spike (RSS) and Ramp-To-Spike (RTS). The Ramp-Soak-Spike profile was developed primarily for reflow ovens heated by infrared radiation. With widespread use of forced convection reflow ovens the Ramp-To-Spike profile is used increasingly. Shown below in figure 6 is VISHAY's recommended profiles for use with the TFBS6711 transistors. For more details please refer to Application note: SMD Assembly Instruction.

Wave Soldering

For TFDUxxxx and TFBSxxxx transistor devices wave soldering is not recommended.

Manual Soldering

Manual soldering is the standard method for lab use. However, for a production process it cannot be recommended because the risk of damage is highly dependent on the experience of the operator. Nevertheless, we added a chapter to the above mentioned application note, describing manual soldering and desoldering.

Storage

The storage and drying processes for all VISHAY transistors (TFDUxxxx and TFBSxxx) are equivalent to MSL4.

The data for the drying procedure is given on labels on the packing and also in the application note "Taping, Labeling, Storage and Packing" (<http://www.vishay.com/docs/82601/82601.pdf>).

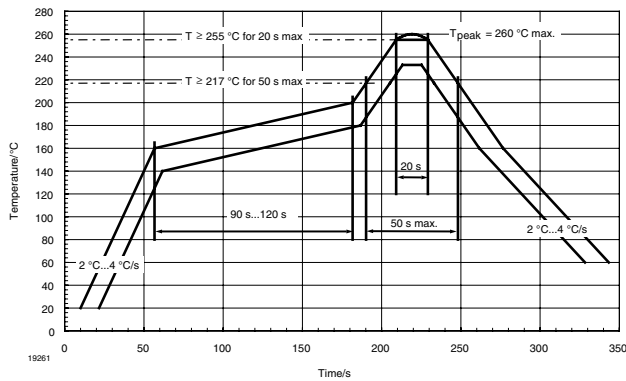


Figure 6. Solder Profile, RSS Recommendation

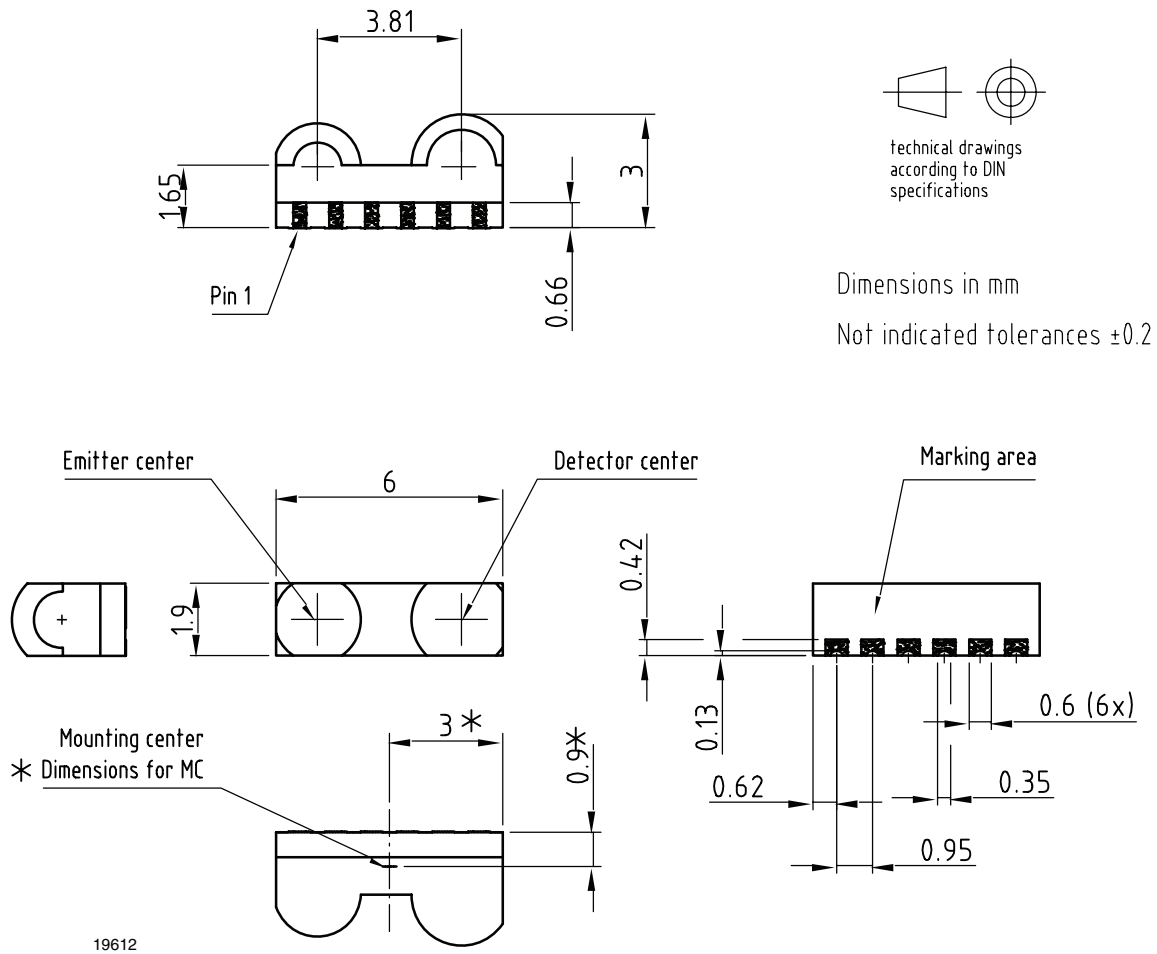
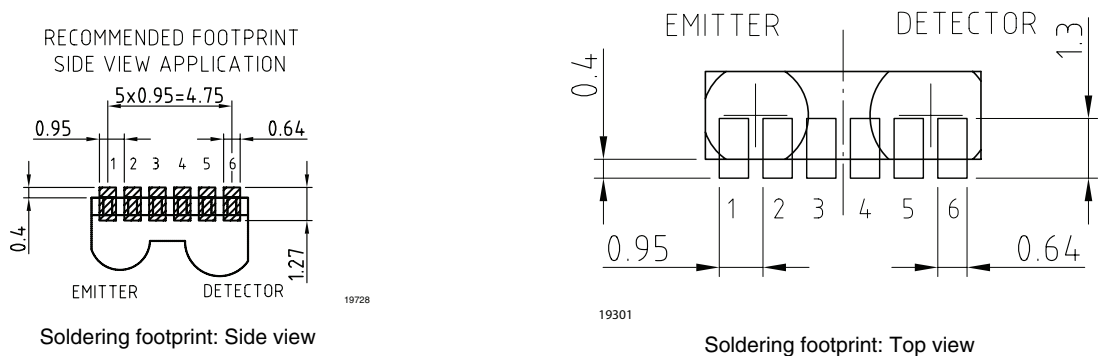
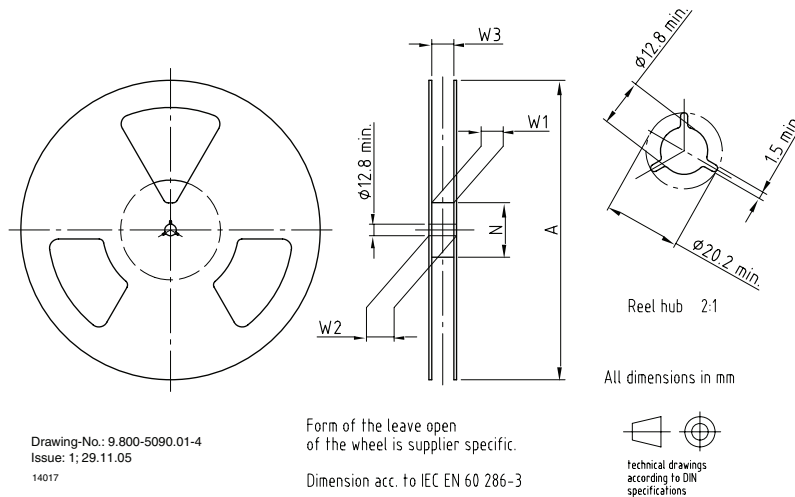
**TFBS4711, TFBS5711, TFBS6711, and TFBS6712 Package
(Mechanical Dimensions)**

 Figure 7. Package drawing, tolerances: Height + 0.1, - 0.2 mm, otherwise ± 0.2 mm if not indicated


Figure 8. Soldering footprints

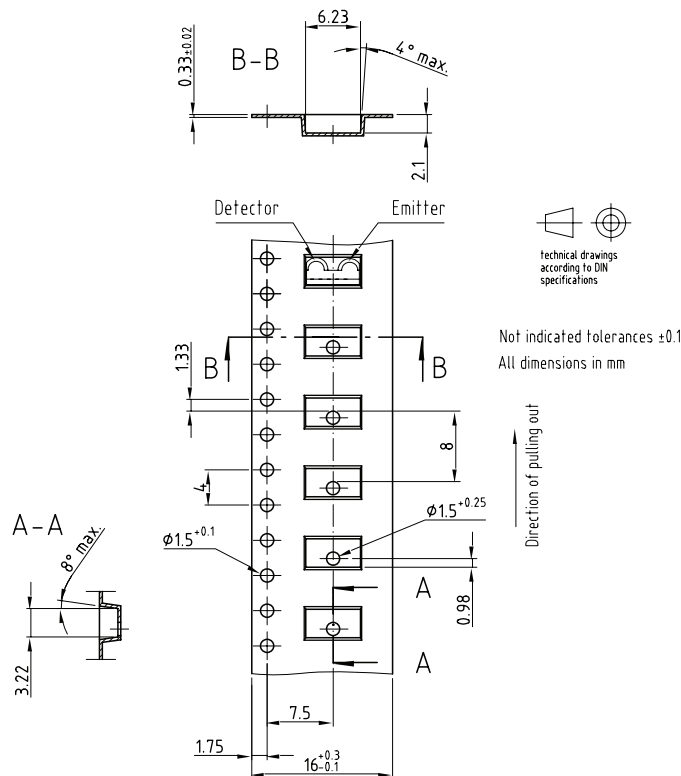
Design Rules for Optical Windows

 For optical windows see the application note on the web <http://www.vishay.com/docs/82506/82506.pdf>.



| Tape Width | A max. | N | W ₁ min. | W ₂ max. | W ₃ min. | W ₃ max. |
|------------|--------|----|---------------------|---------------------|---------------------|---------------------|
| mm | mm | mm | mm | mm | mm | mm |
| 16 | 330 | 50 | 16.4 | 22.4 | 15.9 | 19.4 |

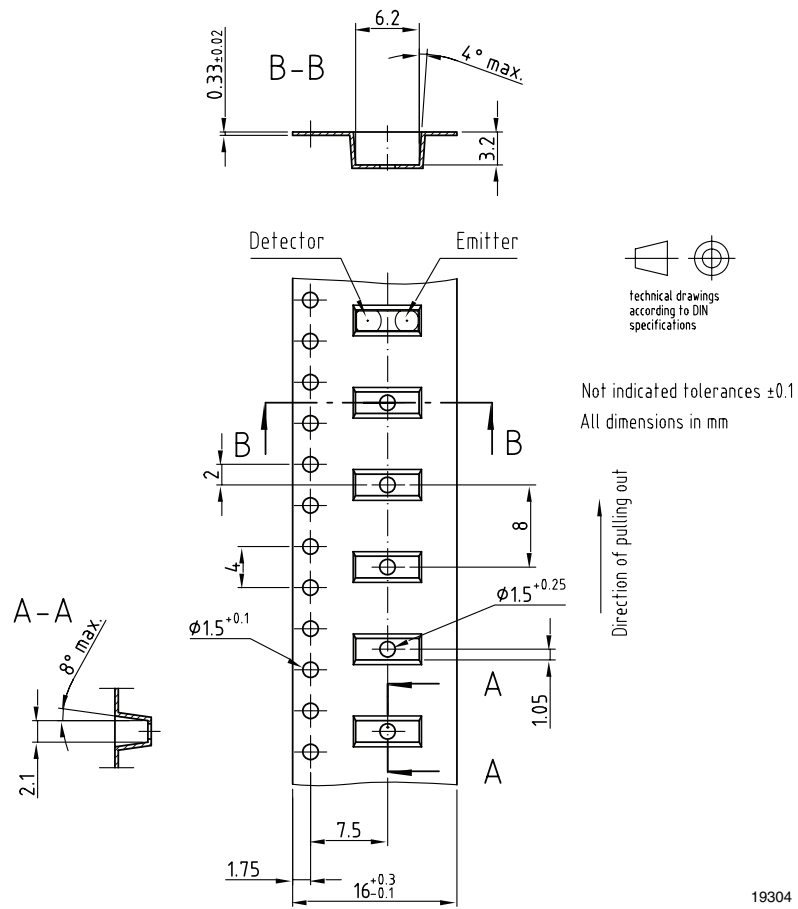
Figure 9. Reel dimensions [mm]



19303

Drawing-No.: 9.700-5294.01-4
Issue: prel. copy; 24.11.04

Figure 10. Tape dimensions [mm] TFBS6711-TT3



Drawing-No.: 9.700-5295.01-4
 Issue: prel. copy; 24.11.04

Figure 11. Tape dimensions [mm] TFBS6711-TR3

Ozone Depleting Substances Policy Statement

It is the policy of Vishay Semiconductor GmbH to

1. Meet all present and future national and international statutory requirements.
2. Regularly and continuously improve the performance of our products, processes, distribution and operating systems with respect to their impact on the health and safety of our employees and the public, as well as their impact on the environment.

It is particular concern to control or eliminate releases of those substances into the atmosphere which are known as ozone depleting substances (ODSs).

The Montreal Protocol (1987) and its London Amendments (1990) intend to severely restrict the use of ODSs and forbid their use within the next ten years. Various national and international initiatives are pressing for an earlier ban on these substances.

Vishay Semiconductor GmbH has been able to use its policy of continuous improvements to eliminate the use of ODSs listed in the following documents.

1. Annex A, B and list of transitional substances of the Montreal Protocol and the London Amendments respectively
2. Class I and II ozone depleting substances in the Clean Air Act Amendments of 1990 by the Environmental Protection Agency (EPA) in the USA
3. Council Decision 88/540/EEC and 91/690/EEC Annex A, B and C (transitional substances) respectively.

Vishay Semiconductor GmbH can certify that our semiconductors are not manufactured with ozone depleting substances and do not contain such substances.

We reserve the right to make changes to improve technical design
and may do so without further notice.

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