FAIRCHILD SEMICONDUCTOR®

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FSAM10SH60

Smart Power Module (SPM)

General Description

FSAM10SH60 is an advanced smart power module (SPM) that Fairchild has newly developed and designed to provide very compact and low cost, yet high performance ac motor drives mainly targeting high speed low-power inverter-driven application like washing machines. It combines optimized circuit protection and drive matched to low-loss IGBTs. Highly effective short-circuit current detection/ protection is realized through the use of advanced current sensing IGBT chips that allow continuous monitoring of the IGBTs current. System reliability is further enhanced by the built-in over-temperature and integrated under-voltage lock-out protection. The high speed built-in HVIC provides opto-coupler-less IGBT gate driving capability that further reduce the overall size of the inverter system design. In addition the incorporated HVIC facilitates the use of single-supply drive topology enabling the FSAM10SH60 to be driven by only one drive supply voltage without negative bias. Inverter current sensing application can be achieved due to the devided nagative dc terminals.

Features

- 600V-10A 3-phase IGBT inverter bridge including control ICs for gate driving and protection
- Divided negative dc-link terminals for inverter current sensing applications
- Single-grounded power supply due to built-in HVIC
- Typical switching frequency of 15kHz
- Built-in thermistor for over-temperature monitoring
- Inverter power rating of 0.4kW / 100~253 Vac
- Isolation rating of 2500Vrms/min.
- Very low leakage current due to using ceramic substrate
- Adjustable current protection level by varying series resistor value with sense-IGBTs

Applications

- AC 100V ~ 253V three-phase inverter drive for small power (0.4kW) ac motor drives
- Home appliances applications requiring high switching frequency operation like washing machines drive system
- Application ratings:
  - Power : 0.4 kW / 100~253 Vac
  - Switching frequency : Typical 15kHz (PWM Control)
  - 100% load current : 3.0A (Irms)
  - 150% load current : 4.5A (Irms) for 1 minute

External View

Top View **Bottom View**

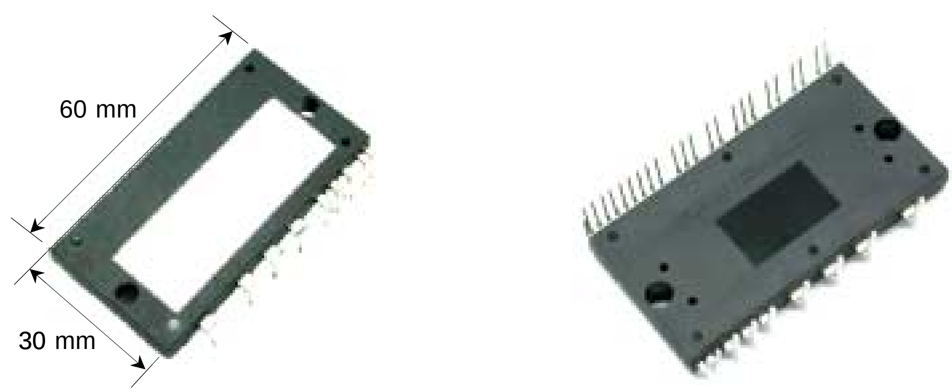


Fig. 1.

Integrated Power Functions

- 600V-10A IGBT inverter for three-phase DC/AC power conversion (Please refer to Fig. 3)

Integrated Drive, Protection and System Control Functions

- For inverter high-side IGBTs: Gate drive circuit, High voltage isolated high-speed level shifting
  Control circuit under-voltage (UV) protection
  Note) Available bootstrap circuit example is given in Figs. 7, 12 and 13.
- For inverter low-side IGBTs: Gate drive circuit, Short circuit protection (SC)
  Control supply circuit under-voltage (UV) protection
- Temperature Monitoring: System over-temperature monitoring using built-in thermistor
  Note) Available temperature monitoring circuit is given in Fig. 13.
- Fault signaling: Corresponding to a SC fault (Low-side IGBTs) or a UV fault (Low-side supply)
- Input interface: 5V CMOS/LSTTL compatible, Schmitt trigger input

Pin Configuration

Top View

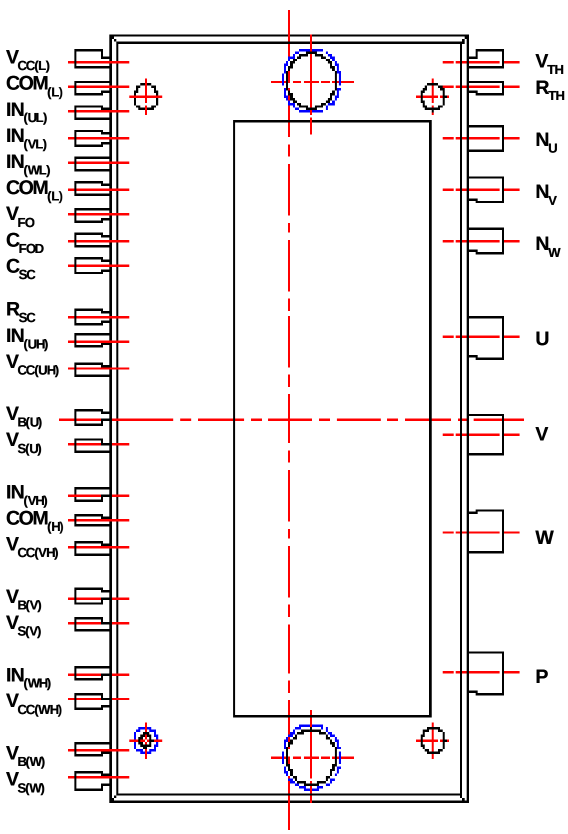


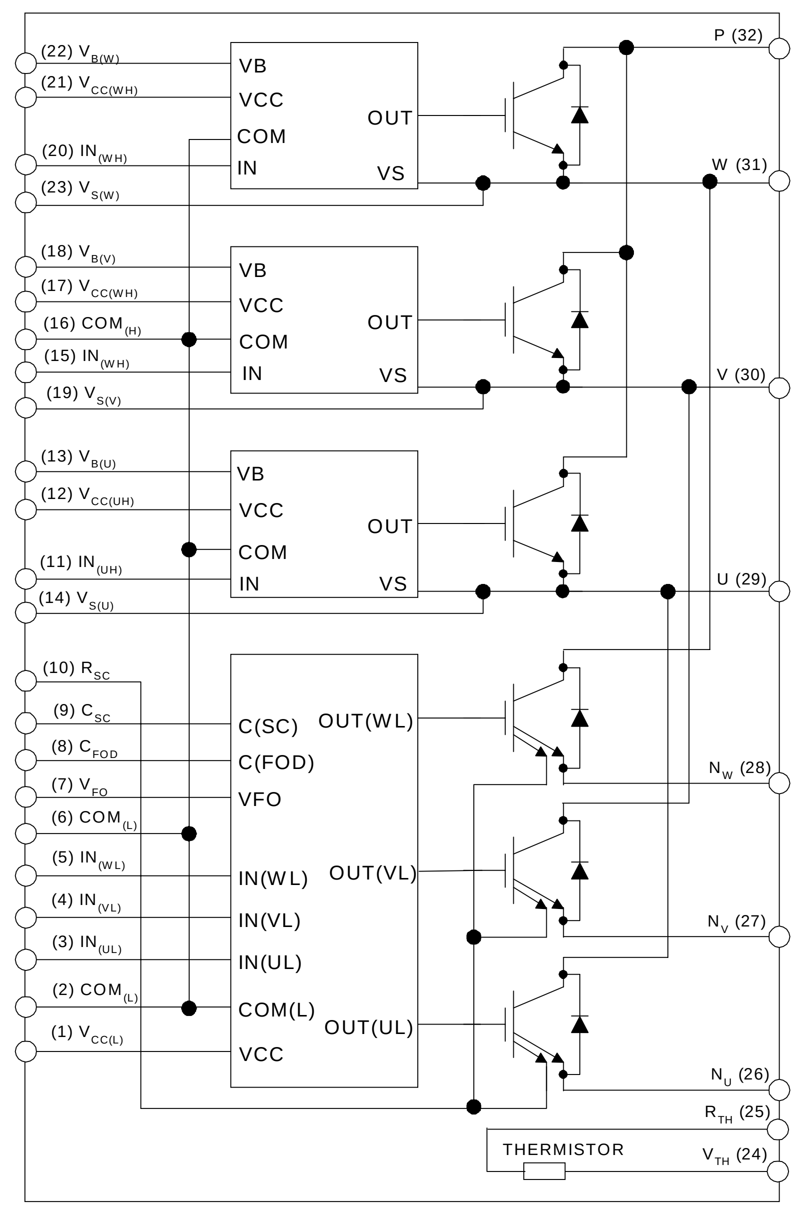
Fig. 2.

Pin Descriptions

Pin Number	Pin Name	Pin Description
1	$V_{CC(L)}$	Low-side Common Bias Voltage for IC and IGBTs Driving
2	$COM_{(L)}$	Low-side Common Supply Ground
3	$IN_{(UL)}$	Signal Input Terminal for Low-side U Phase
4	$IN_{(VL)}$	Signal Input Terminal for Low-side V Phase
5	$IN_{(WL)}$	Signal Input Terminal for Low-side W Phase
6	$COM_{(L)}$	Low-side Common Supply Ground
7	V_{FO}	Fault Output Terminal
8	C_{FOD}	Capacitor for Fault Output Duration Time Selection
9	C_{SC}	Capacitor (Low-pass Filter) for Short-current Detection Input
10	R_{SC}	Resistor for Short-circuit Current Detection
11	$IN_{(UH)}$	Signal Input Terminal for High-side U Phase
12	$V_{CC(UH)}$	High-side Bias Voltage for U Phase IC
13	$V_{B(U)}$	High-side Bias Voltage for U Phase IGBT Driving
14	$V_{S(U)}$	High-side Bias Voltage Ground for U Phase IGBT Driving
15	$IN_{(VH)}$	Signal Input Terminal for High-side V Phase
16	$COM_{(H)}$	High-side Common Supply Ground
17	$V_{CC(VH)}$	High-side Bias Voltage for V Phase IC
18	$V_{B(V)}$	High-side Bias Voltage for V Phase IGBT Driving
19	$V_{S(V)}$	High-side Bias Voltage Ground for V Phase IGBT Driving
20	$IN_{(WH)}$	Signal Input Terminal for High-side W Phase
21	$V_{CC(WH)}$	High-side Bias Voltage for W Phase IC
22	$V_{B(W)}$	High-side Bias Voltage for W Phase IGBT Driving
23	$V_{S(W)}$	High-side Bias Voltage Ground for W Phase IGBT Driving
24	V_{TH}	Thermistor Bias Voltage
25	R_{TH}	Series Resistor for the Use of Thermistor (Temperature Detection)
26	N_U	Negative DC–Link Input Terminal for U Phase
27	N_V	Negative DC–Link Input Terminal for V Phase
28	N_W	Negative DC–Link Input Terminal for W Phase
29	U	Output Terminal for U Phase
30	V	Output Terminal for V Phase
31	W	Output Terminal for W Phase
32	P	Positive DC–Link Input Terminal

Internal Equivalent Circuit and Input/Output Pins

Bottom View



Note

1. Inverter low-side is composed of three sense-IGBTs including freewheeling diodes for each IGBT and one control IC which has gate driving, current sensing and protection functions.
2. Inverter power side is composed of four inverter dc-link input terminals and three inverter output terminals.
3. Inverter high-side is composed of three normal-IGBTs including freewheeling diodes and three drive ICs for each IGBT.

Fig. 3.

Absolute Maximum Ratings

Inverter Part (T_C = 25°C, Unless Otherwise Specified)

Item	Symbol	Condition	Rating	Unit
Supply Voltage	V_{DC}	Applied to DC - Link	450	V
Supply Voltage (Surge)	$V_{PN(Surge)}$	Applied between P- N	500	V
Collector-emitter Voltage	V_{CES}		600	V
Each IGBT Collector Current	$\pm I_C$	T_C = 25°C	10	A
Each IGBT Collector Current	$\pm I_C$	T_C = 100°C	8	A
Each IGBT Collector Current (Peak)	$\pm I_{CP}$	T_C = 25°C	20	A
Collector Dissipation	P_C	T_C = 25°C per One Chip	-	W
Operating Junction Temperature	T_J	(Note 1)	-55 ~ 150	°C

Note

1. It would be recommended that the average junction temperature should be limited to $T_J \le 125°C$ (@$T_C \le 100°C$) in order to guarantee safe operation.

Control Part (T_C = 25°C, Unless Otherwise Specified)

Item	Symbol	Condition	Rating	Unit
Control Supply Voltage	V_{CC}	Applied between $V_{CC(H)}$ - $COM_{(H)}$, $V_{CC(L)}$ - $COM_{(L)}$	18	V
High-side Control Bias Voltage	V_{BS}	Applied between $V_{B(U)}$ - $V_{S(U)}$, $V_{B(V)}$ - $V_{S(V)}$, $V_{B(W)}$ - $V_{S(W)}$	20	V
Input Signal Voltage	V_{IN}	Applied between $IN_{(UH)}$, $IN_{(VH)}$, $IN_{(WH)}$ - $COM_{(H)}$ $IN_{(UL)}$, $IN_{(VL)}$, $IN_{(WL)}$ - $COM_{(L)}$	-0.3 ~ 6.0	V
Fault Output Supply Voltage	V_{FO}	Applied between V_{FO} - $COM_{(L)}$	-0.3~V_{CC}+0.5	V
Fault Output Current	I_{FO}	Sink Current at V_{FO} Pin	5	mA
Current Sensing Input Voltage	V_{SC}	Applied between C_{SC} - $COM_{(L)}$	-0.3~V_{CC}+0.5	V

Total System

Item	Symbol	Condition	Rating	Unit
Self Protection Supply Voltage Limit (Short Circuit Protection Capability)	$V_{PN(PROT)}$	Applied to DC - Link, $V_{CC} = V_{BS}$ = 13.5 ~ 16.5V T_J = 125°C, Non-repetitive, less than 6μs	400	V
Module Case Operation Temperature	T_C		-	°C
Storage Temperature	T_{STG}		-	°C
Isolation Voltage	V_{ISO}	60Hz, Sinusoidal, AC 1 minute, Connection Pins to Heat-sink Plate	2500	V_{rms}

Absolute Maximum Ratings

Thermal Resistance

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Junction to Case Thermal Resistance	$R_{th(j-c)Q}$	Each IGBT under Inverter Operating Condition	-	-	-	°C/W
	$R_{th(j-c)F}$	Each FWDi under Inverter Operating Condition	-	-	-	°C/W
Contact Thermal Resistance	$R_{th(c-f)}$	Ceramic Substrate (per 1 Module) Thermal Grease Applied	-	-	-	°C/W

Electrical Characteristics

Inverter Part (T_j = 25°C, Unless Otherwise Specified)

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Collector - emitter Saturation Voltage	$V_{CE(SAT)}$	$V_{CC} = V_{BS}$ = 15V V_{IN} = 0V	I_C = 10A, T_j = 25°C	-	-	2.8	V
			I_C = 10A, T_j = 125°C	-	-	2.9	V
FWDi Forward Voltage	V_{FM}	V_{IN} = 5V	I_C = 10A, T_j = 25°C	-	-	2.3	V
			I_C = 10A, T_j = 125°C	-	-	2.1	V
Switching Times	t_{ON}	V_{PN} = 300V, $V_{CC} = V_{BS}$ = 15V I_C = 10A, T_j = 25°C V_{IN} = 5V ↔ 0V, Inductive Load (High-Low Side) (Note 2)		-	0.37	-	us
	$t_{C(ON)}$			-	0.12	-	us
	t_{OFF}			-	0.53	-	us
	$t_{C(OFF)}$			-	0.2	-	us
	t_{rr}			-	0.1	-	us
Collector - emitter Leakage Current	I_{CES}	$V_{CE} = V_{CES}$, T_j = 25°C		-	-	250	uA

Note

2. t_{ON} and t_{OFF} include the propagation delay time of the internal drive IC. $t_{C(ON)}$ and $t_{C(OFF)}$ are the switching time of IGBT itself under the given gate driving condition internally. For the detailed information, please see Fig. 4.

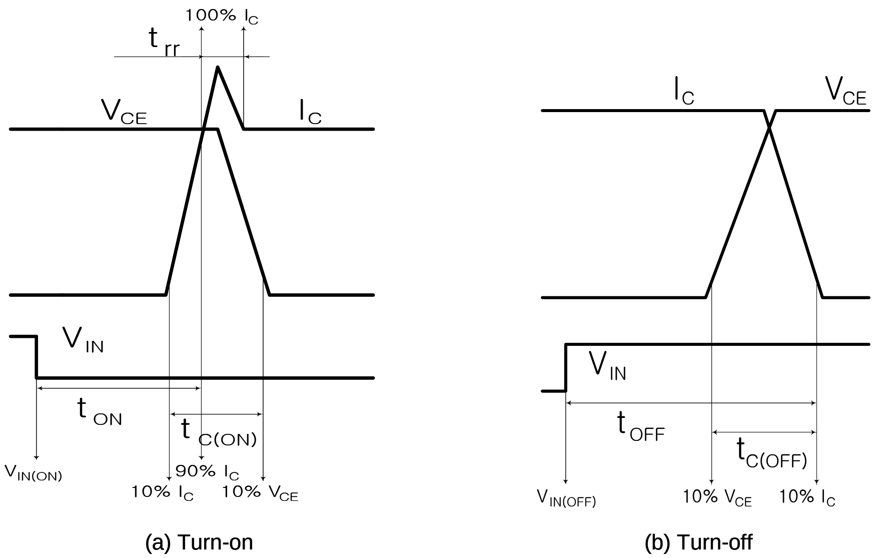


Fig. 4. Switching Time Definition

Electrical Characteristics

Control Part (T_j = 25°C, Unless Otherwise Specified)

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Control Supply Voltage	V_{CC}	Applied between $V_{CC(H)}$,$V_{CC(L)}$ - COM		13.5	15	16.5	V
High-side Bias Voltage	V_{BS}	Applied between $V_{B(U)}$ - $V_{S(U)}$, $V_{B(V)}$ - $V_{S(V)}$, $V_{B(W)}$ - $V_{S(W)}$		13.5	15	16.5	V
Quiescent V_{CC} Supply Current	I_{QCCL}	V_{CC} = 15V $IN_{(UL, VL, WL)}$ = 5V	$V_{CC(L)}$ - $COM_{(L)}$	-	-	26	mA
	I_{QCCH}	V_{CC} = 15V $IN_{(UH, VH, WH)}$ = 5V	$V_{CC(U)}$, $V_{CC(V)}$, $V_{CC(W)}$ - $COM_{(H)}$	-	-	130	uA
Quiescent V_{BS} Supply Current	I_{QBS}	V_{BS} = 15V $IN_{(UH, VH, WH)}$ = 5V	$V_{B(U)}$ - $V_{S(U)}$, $V_{B(V)}$ -$V_{S(V)}$, $V_{B(W)}$ - $V_{S(W)}$	-	-	420	uA
Fault Output Voltage	V_{FOH}	V_{SC} = 0V, V_{FO} Circuit: 4.7kΩ to 5V Pull-up		4.5	-	-	V
	V_{FOL}	V_{SC} = 1V, V_{FO} Circuit: 4.7kΩ to 5V Pull-up		-	-	1.1	V
PWM Input Frequency	f_{PWM}	$T_C \le 100°C$, $T_J \le 125°C$		-	15	-	kHz
Allowable Input Signal Blanking Time considering Leg Arm-short	t_{dead}	$-20°C \le T_C \le 100°C$		1	-	-	us
Short Circuit Trip Level	$V_{SC(ref)}$	T_J = 25°C, V_{CC} = 15V (Note 3)		0.45	0.51	0.56	V
Sensing Voltage of IGBT Current	V_{SEN}	$-20°C \le T_C \le 100°C$, @ R_{SC} = 82 Ω, $R_{SU} = R_{SV} = R_{SW}$ = 0 Ω and I_C = 10A (Note Fig. 13)		0.37	0.45	0.56	V
Supply Circuit Under-Voltage Protection	UV_{CCD}	$T_J \le 125°C$	Detection Level	11.5	12	12.5	V
	UV_{CCR}		Reset Level	12	12.5	13	V
	UV_{BSD}		Detection Level	7.3	9.0	10.8	V
	UV_{BSR}		Reset Level	8.6	10.3	12	V
Fault-out Pulse Width	t_{FOD}	C_{FOD} = 33nF (Note 4)		1.4	1.8	2.0	ms
ON Threshold Voltage	$V_{IN(ON)}$	High-Side	Applied between $IN_{(UH)}$, $IN_{(VH)}$, $IN_{(WH)}$ - $COM_{(H)}$	-	-	0.8	V
OFF Threshold Voltage	$V_{IN(OFF)}$			3.0	-	-	V
ON Threshold Voltage	$V_{IN(ON)}$	Low-Side	Applied between $IN_{(UL)}$, $IN_{(VL)}$, $IN_{(WL)}$ - $COM_{(L)}$	-	-	0.8	V
OFF Threshold Voltage	$V_{IN(OFF)}$			3.0	-	-	V
Resistance of Thermistor	R_{TH}	@ T_C = 25°C (Note Fig. 5)		-	50	-	kΩ
		@ T_C = 80°C (Note Fig. 5)		-	6.3	-	kΩ

Note

3. Short-circuit current protection is functioning only at the low-sides. It would be recommended that the value of the external sensing resistor (R_{SC}) should be selected around 56 Ω in order to make the SC trip-level of about 15A at the shunt resistors (R_{SU},R_{SV},R_{SW}) of 0Ω . For the detailed information about the relationship between the external sensing resistor (R_{SC}) and the shunt resistors (R_{SU},R_{SV},R_{SW}), please see Fig. 6.
4. The fault-out pulse width t_{FOD} depends on the capacitance value of C_{FOD} according to the following approximate equation : $C_{FOD} = 18.3 \times 10^{-6} \times t_{FOD}$[F]

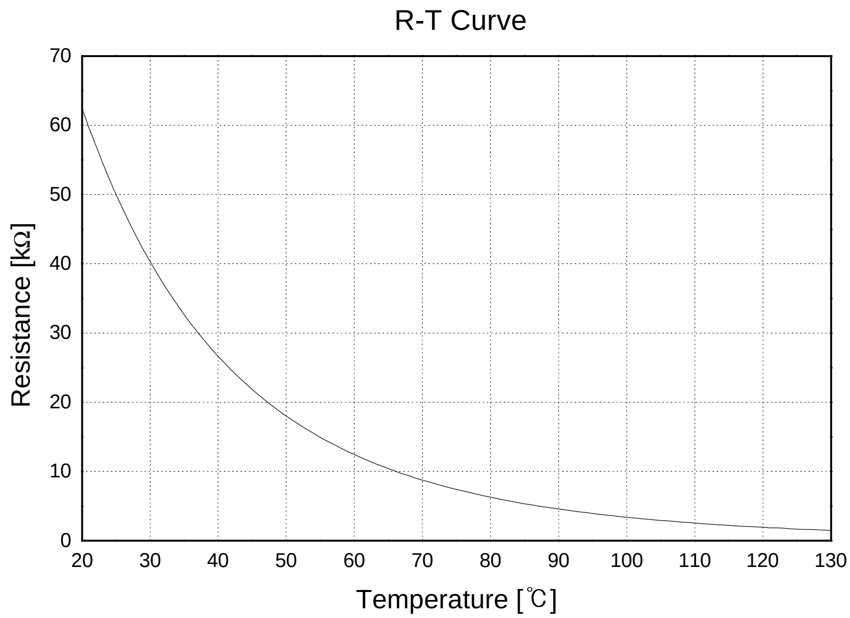


Fig. 5. R-T Curve of The Built-in Thermistor

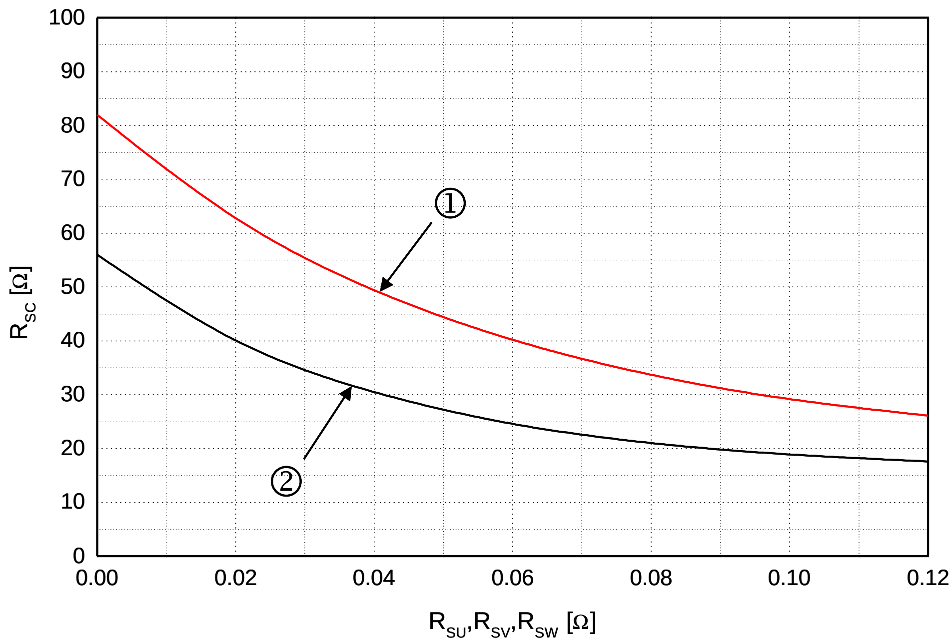


Fig. 6. R_{SC} Variation by change of Shunt Resistors (R_{SU}, R_{SV}, R_{SW}) for Short-Circuit Protection
① @ around 100% Rated Current Trip(Ic ≒ 10A),
② @ around 150% Rated Current Trip(Ic ≒ 15A)

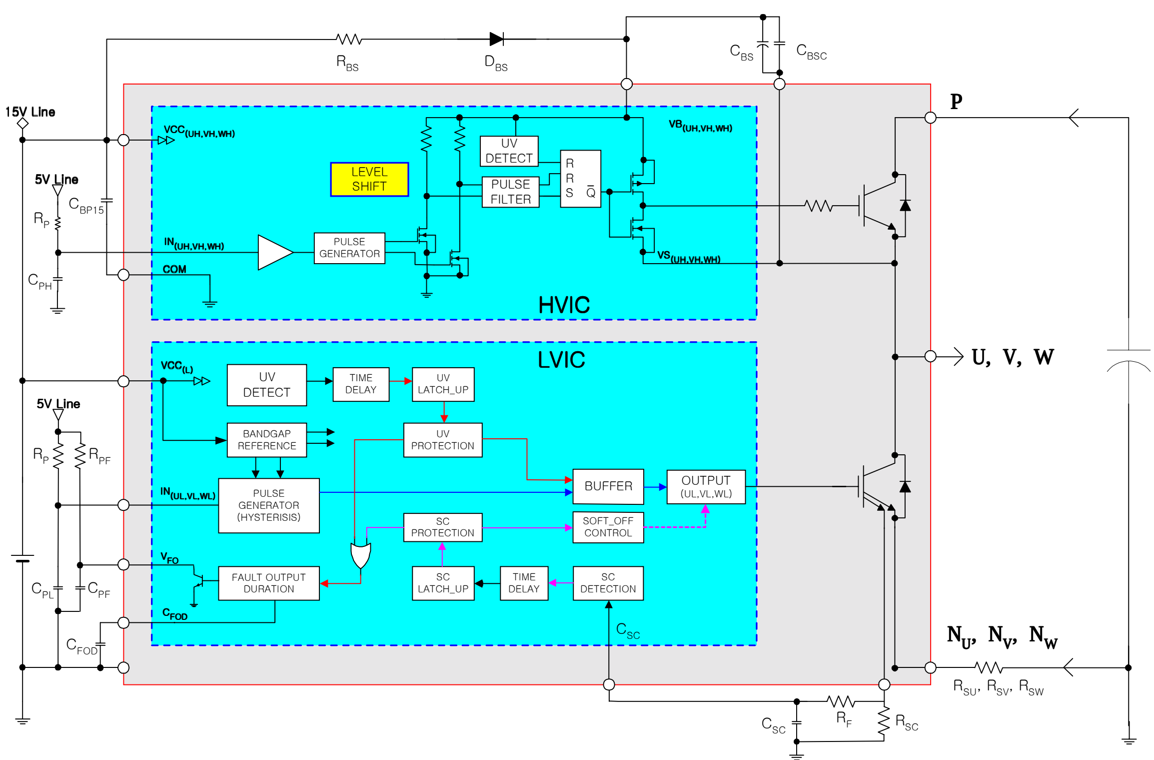
Mechanical Characteristics and Ratings

Item	Condition		Limits			Units
			Min.	Typ.	Max.	
Mounting Torque	Mounting Screw: M3	Recommended 15.3Kg•cm	-	15.3	-	Kg•cm
		Recommended 1.5N•m	-	1.5	-	N•m
Ceramic Flatness			-	-	-	um
Weight			-	-	-	g

Recommended Operating Conditions

Item	Symbol	Condition	Value			Unit
			Min.	Typ.	Max.	
Supply Voltage	V_{PN}	Applied between P - N	-	300	400	V
Control Supply Voltage	V_{CC}	Applied between $V_{CC(H)}$ - COM, $V_{CC(L)}$ - COM	13.5	15	16.5	V
High-side Bias Voltage	V_{BS}	Applied between $V_{B(U)}$ - $V_{S(U)}$, $V_{B(V)}$ - $V_{S(V)}$, $V_{B(W)}$ - $V_{S(W)}$	13.5	15	16.5	V
Blanking Time for Preventing Arm-short	t_{dead}	For Each Input Signal	1	-	-	us
PWM Input Signal	f_{PWM}	$T_C \le 100°C$, $T_J \le 125°C$	-	15	-	kHz
Input ON Threshold Voltage	$V_{IN(ON)}$	Applied between U_{IN},V_{IN}, W_{IN} - COM		0 ~ 0.65		V
Input OFF Threshold Voltage	$V_{IN(OFF)}$	Applied between U_{IN},V_{IN}, W_{IN} - COM		4 ~ 5.5		V

ICs Internal Structure and Input/Output Conditions

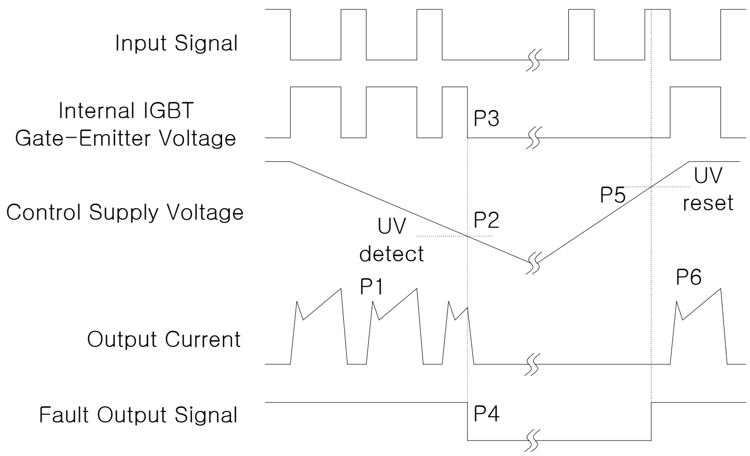


Note

1. One LVIC drives three Sense-IGBTs and can do short-circuit current protection also. Three sense emitters are commonly connected to R_{SC} terminal to detect short-circuit current. Low-side part of the inverter consists of three sense-IGBTs
2. One HVIC drives one normal-IGBT. High-side part of the inverter consists of three normal-IGBTs
3. Each IC has under voltage detection and protection function.
4. The logic input is compatible with standard CMOS or LSTTL outputs.
5. R_PC_P coupling at each input/output is recommended in order to prevent the gating input/output signals oscillation and it should be as close as possible to each SPM gating input pin.
6. It would be recommended that the bootstrap diode, D_{BS}, has soft and fast recovery characteristics.

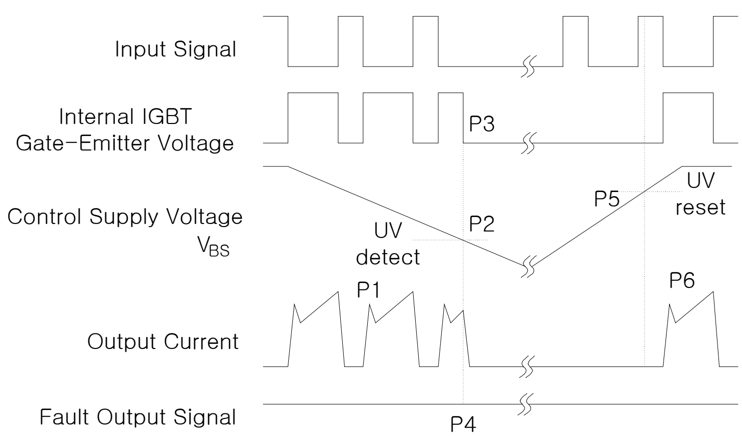
Fig. 7.

Time Charts of SPMs Protective Function



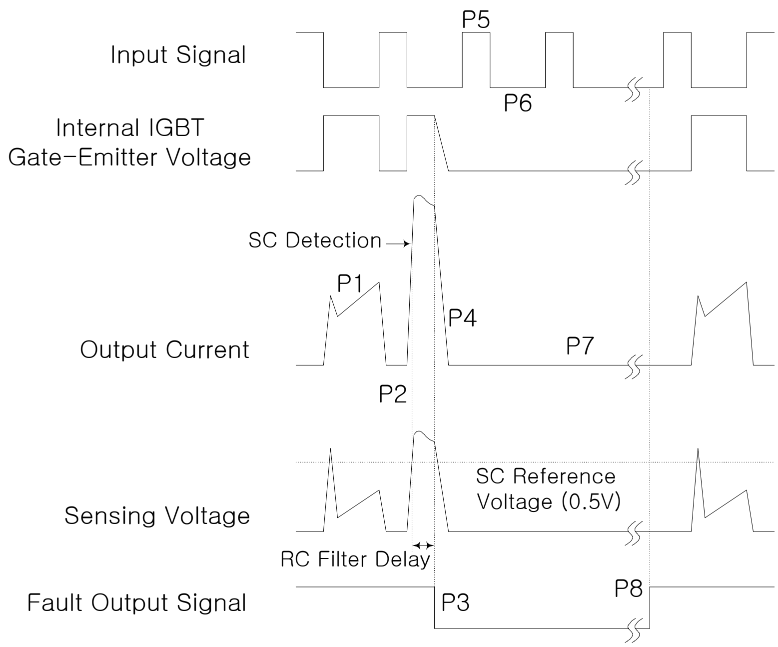
P1 : Normal operation - IGBT ON and conducting current
P2 : Under voltage detection
P3 : IGBT gate interrupt
P4 : Fault signal generation
P5 : Under voltage reset
P6 : Normal operation - IGBT ON and conducting current

Fig. 8. Under-Voltage Protection (Low-side)



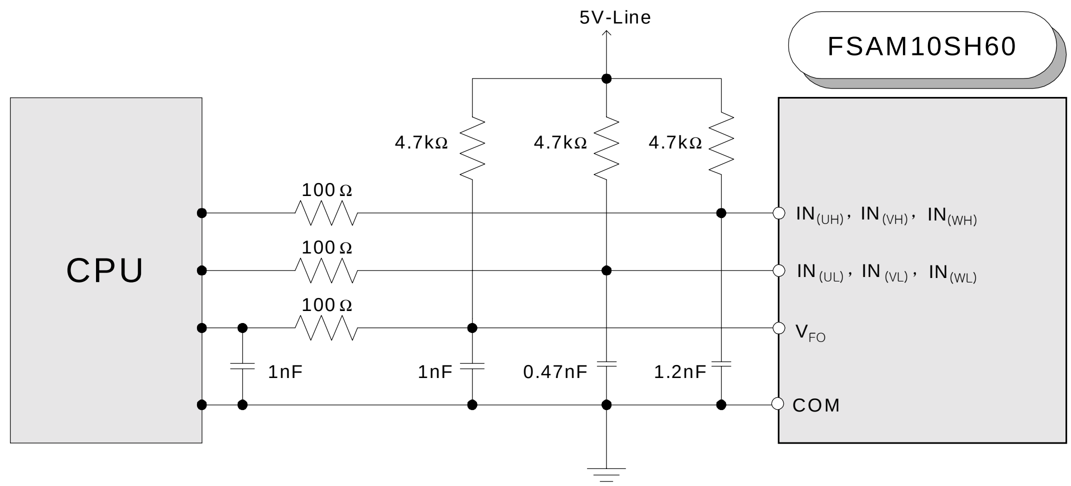
P1 : Normal operation - IGBT ON and conducting current
P2 : Under voltage detection
P3 : IGBT gate interrupt
P4 : No fault signal
P5 : Under voltage reset
P6 : Normal operation - IGBT ON and conducting current

Fig. 9. Under-Voltage Protection (High-side)



P1 : Normal operation - IGBT ON and conducting currents
P2 : Short-circuit current detection
P3 : IGBT gate interrupt / Fault signal generation
P4 : IGBT is slowly turned off
P5 : IGBT OFF signal
P6 : IGBT ON signal - but IGBT cannot be turned on during the fault-output activation
P7 : IGBT OFF state
P8 : Fault-output reset and normal operation start

Fig. 10. Short-circuit Current Protection (Low-side Operation only)



Note

It would be recommended that by-pass capacitors for the gating input signals, $IN_{(XX)}$ should be placed on the SPM pins and on the both sides of CPU and SPM for the fault output signal, V_{FO}, as close as possible.

Fig. 11. Recommended CPU I/O Interface Circuit

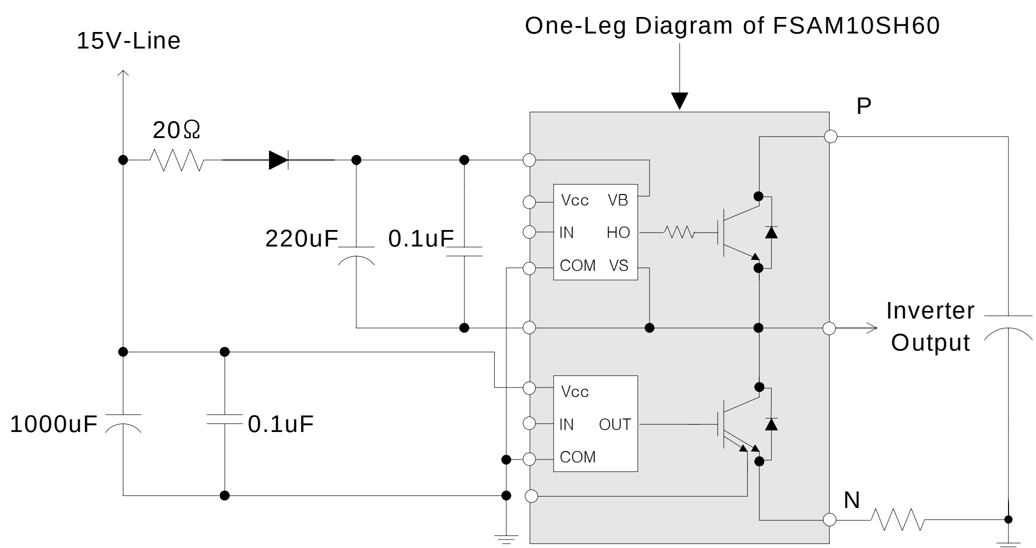
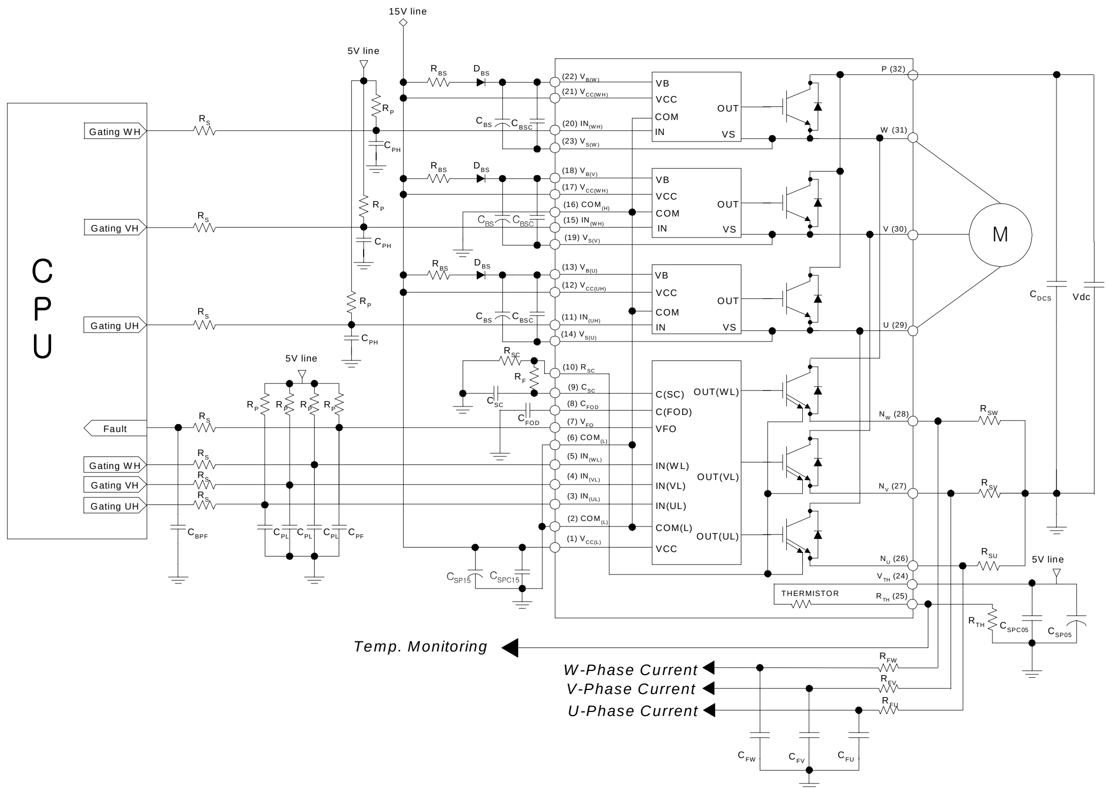


Fig. 12. Recommended Bootstrap Operation Circuit and Parameters

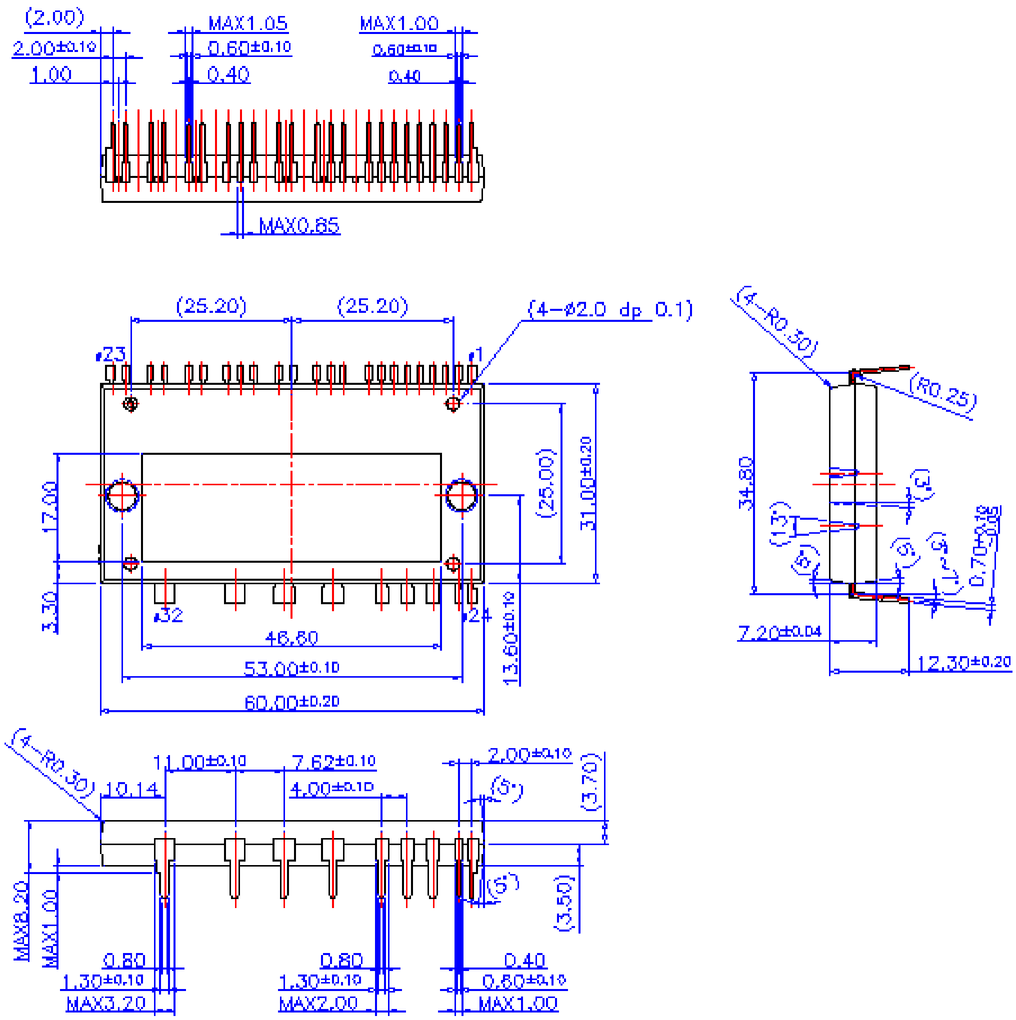


Note

1. R_PC_{PL}/R_PC_{PH} coupling at each SPM input is recommended in order to prevent input signals' oscillation and it should be as close as possible to each SPM input pin.
2. By virtue of integrating an application specific type HVIC inside the SPM, direct coupling to CPU terminals without any opto-coupler or transformer isolation is possible.
3. V_{FO} output is open collector type. This signal line should be pulled up to the positive side of the 5V power supply with approximately 4.7kΩ resistance. Please refer to Fig. 13.
4. C_{SP15} of around 7 times larger than bootstrap capacitor C_{BS} is recommended.
5. V_{FO} output pulse width should be determined by connecting an external capacitor(C_{FOD}) between C_{FOD}(pin8-) and $COM_{(L)}$(pin2). (Example : if C_{FOD} = 5.6 nF, then t_{FO} = 300 µs (typ.)) Please refer to the note 5 for calculation method.
6. Each input signal line should be pulled up to the 5V power supply with approximately 4.7kΩ resistance (other RC coupling circuits at each input may be needed depending on the PWM control scheme used and on the wiring impedance of the system's printed circuit board). Approximately a 0.22~2nF by-pass capacitor should be used across each power supply connection terminals.
7. To prevent errors of the protection function, the wiring around R_{SC}, R_F and C_{SC} should be as short as possible.
8. In the short-circuit protection circuit, please select the R_FC_{SC} time constant in the range 3~4 µs. R_F should be at least 30 times larger than R_{SC}. (Recommended Example: R_{SC} = 56 Ω, R_F = 3.9kΩ, C_{SC} = 1nF and R_{SU} = R_{SV} = R_{SW} = 0Ω)
9. For the use of shunt resistors (R_{SU}, R_{SV}, R_{SW}), please see Fig. 6 in order to select the proper R_{SC}.
10. Each capacitor should be mounted as close to the pins of the SPM as possible.
11. To prevent surge destruction, the wiring between the smoothing capacitor and the P&N pins should be as short as possible. The use of a high frequency non-inductive capacitor of around 0.1~0.22 uF between the P&N pins is recommended.
12. Relays are used at almost every systems of electrical equipments of home appliances. In these cases, there should be sufficient distance between the CPU and the relays. It is recommended that the distance be 5cm at least

Fig. 13. Application Circuit

Detailed Package Outline Drawings



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DOME™	ISOPLANAR™	QT Optoelectronics™	UHC™
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E^2CMOS™	MicroFET™	SLIENT SWITCHER®	VCX™
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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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Definition of Terms

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Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
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