ISG4042-T

5 V CATV MODEM RF TUNER AND TRANSMITTER

FEATURES

- **TWO WAY DOCSIS BASED DESIGN:**
  91-857 MHz Downstream
  5-42 MHz Upstream

- **SINGLE SUPPLY 5 V OPERATION:**
  With Built in Linear Regulation

- **SINGLE AGC CONTROL**
  Simplifies Modem Calibration

- **ULTRA SMALL SIZE:**
  1.9 x 2.0 x 0.5 in., 1.9 in^3
  46.2 x 49.0 x 12.5 mm., 28.5 cc.

- **DIGITAL LINEAR RF TRANSMITTER:**
  All Harmonics meets DOCSIS @ 58 dBmV (see note 2)
  $\geq$ 56 dB Gain Range (0.5 dB steps)

- **INTERFACES DIRECTLY WITH QAM MOD/DEMOD IC's:**
  (see note 3)

DESCRIPTION AND APPLICATIONS

The ISG4042-T is an RF tuner/transmitter designed for use in DOCSIS cable modem applications. It is a complete solution that interfaces directly with QAM Mod/Demod IC's. The tuner/transmitter integrates a diplex filter, dual conversion receiver, transmit AGC amplifier, and other RF filtering (see Figure 1). The diplex filter provides over 40 dB of isolation between the Tx band and the Rx band. The receiver channel selects and converts QAM signals in the Rx band down to the IF sampling frequency. It also provides the necessary gain control to adjust the input power to the DSP chip. The RF transmitter section provides $\geq$ 56 dB of digitally controlled range while maintaining excellent linearity performance.

ELECTRICAL CHARACTERISTICS (V_{CC} = 5 V, ±2 %, T_A = 25°C) (see note 4)

SYMBOLS	PARAMETERS	UNITS	MIN	TYP	MAX
RF Performance (Rx)					
f_{OP}	Operating Frequency Range (Center to Center)	MHz	91		857
	Input Signal Level	dBmV	-15		15
	Maximum Voltage Gain	dB		57	
	Automatic Voltage Gain Control Range	dB	45		
V_{AGC}	IF Automatic Voltage Gain Control	V	0		3.3
NF_{MAX}	Noise Figure (at Max Voltage Gain)	dB		8	10
	Phase Noise at 10 kHz Offset	dBc/Hz		-85	-82
	LO Radiation at RF Input	dBm		-40	
	Resolution	kHz		31.25	
	Lock Time (end to end channel)	msec.		18	
	Input Impedance (Nominal)	ohms		75	
RL_{IN}	Input Return Loss	dB	6		
	Channel Bandwidth USA	MHz		6	
	Output Frequency	MHz		43.75	
	Passband Ripple over 5.36 MHz Bandwidth	dB		1	2
	Image Rejection	dB	50		
	Inband Group Delay	ns			100
	CSO[1]	dBc	45	50	
	CTB[1]	dBc	45	50	
	Output Frequency Offset	kHz	-35		+35
	Output IF Voltage Level	V$_{PP}$		1	
	Output IF Load	KΩ		1	

Notes:
1. 110 Channels at +15 dBmV/tone.
2. 160K Symbol rate; under DOCSIS PHY - 17 high condition.
3. Application specification for TI 4040/4042.
4. Specifications apply to test conditions listed.
* PHY 7/17/18 Data available upon request.

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ELECTRICAL CHARACTERISTICS (V_{CC} = 5 V, ±2%, T_A = 25°C) (see note 2)

SYMBOLS	PARAMETERS	UNITS	MIN	TYP	MAX
RF Performance (Tx)					
f_{OP}	Operating Frequency Range	MHz	5		42
	G_{MAX} (Gain Word = 255)	dB	26	27	
	G_{MIN} (Gain Word =48)	dB		-27	-26
	Output Step Size	dB		0.5	
	Flatness (5 to 42 MHz)	dB		1.7	2.5
	Amplitude Ripple Over 1.28 MHz	dB			0.6
	2nd Harmonic Level (F_{IN} = 65 MHz, P_{OUT} = +58 dBmV)[1]	dBmV		-48	-45
	3rd Harmonic Level (F_{IN} = 65 MHz, P_{OUT} = +58 dBmV)[1]	dBmV		-48	-45
	Input Impedance	Ω		300	
RL_{OUT}	Output Return Loss	dB	6		
T_X ON/OFF	On/Off Setting Time	μs		3.2	5
	Group Delay (5-42 MHz)	ns			100
	Tx Transient Spurs	mV			7
	Tx Transient Duration	μs		3.2	5
Power Requirements					
	Supply Voltage V1 Rx	V	4.75	5	5.25
	Supply Voltage V1 Tx	V	4.75	5	5.25
	Supply Ripple Voltage V1 Rx	mV			100
Supply Current					
I_{CC1} (Rx)	Supply Current 1 (Rx)	mA		310	
I_{CC1} (Tx)	Supply Current 1 (Tx) T_{XEN} = High	mA		120	150
	Supply Current 1 (Tx) T_{XEN} = Low	mA		8	12
Physical Interface					
	To the CATV Network			Female F-Connector	
	To the Motherboard			16 Pin Header	

Notes:
1. 160K Symbol rate; under DOCSIS PHY - 17 high condition.
2. Specifications apply to test conditions listed.

ABSOLUTE MAXIMUM RATINGS

(T_C = 25°C unless otherwise noted)

| SYMBOLS	PARAMETERS	UNITS	RATINGS
V_{IN}	RF Input Voltage	dBmV	60
V_{CC1} (Rx)	Supply Voltage (Rx)	V	+6.5
V_{CC} (Tx)	Supply Voltage (Tx)	V	+5.5
T_{OP}	Operating Temperature	°C	-40 to 75
T_{STG}	Storage Temperature	°C	-40 to 75
T_{SOL}	Soldering Temperature	°C	260
t_{SOL}	Soldering Time	sec.	4

Note:
1. Operation in excess of any one of these parameters may result in permanent damage.
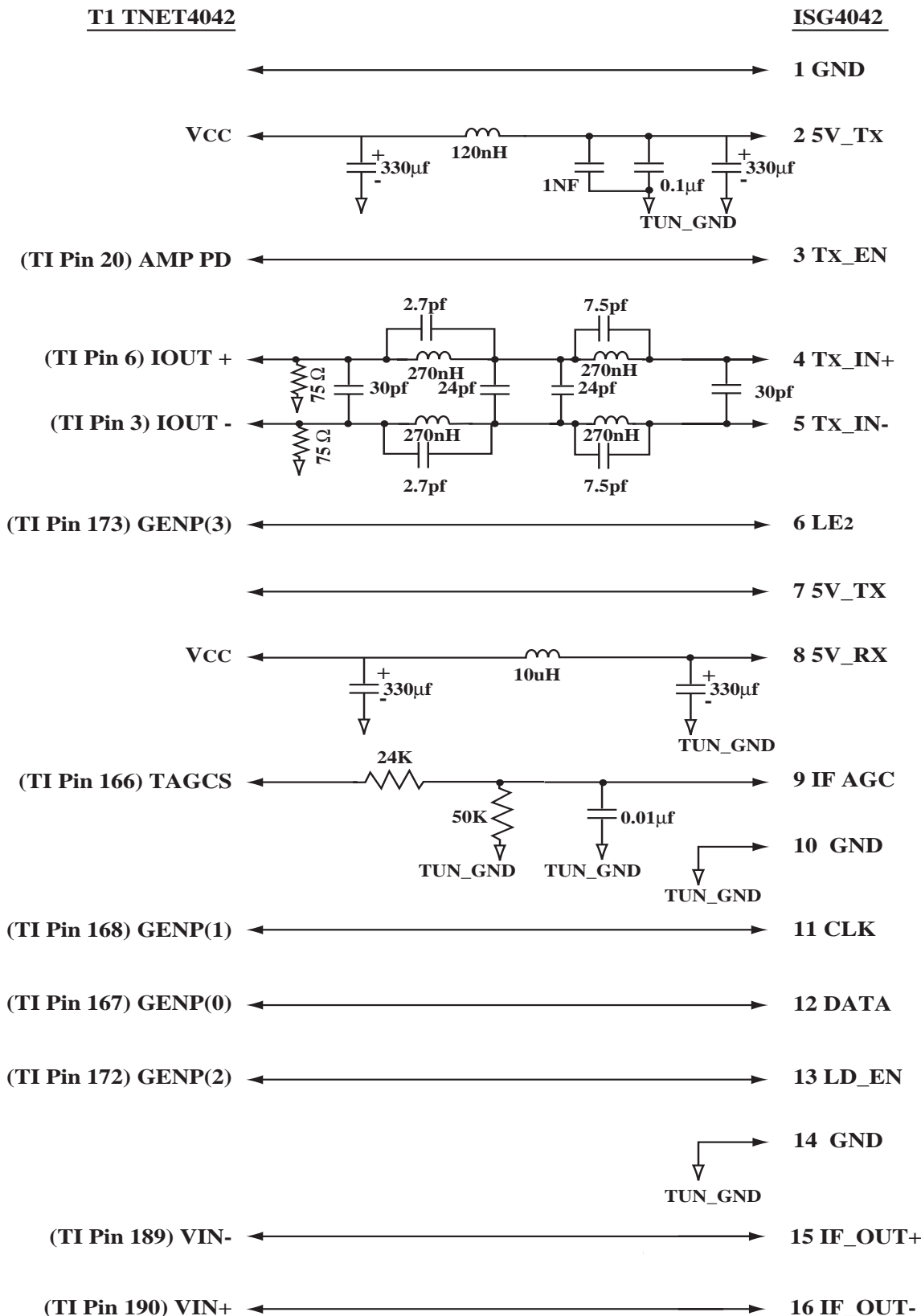
PIN FUNCTIONS

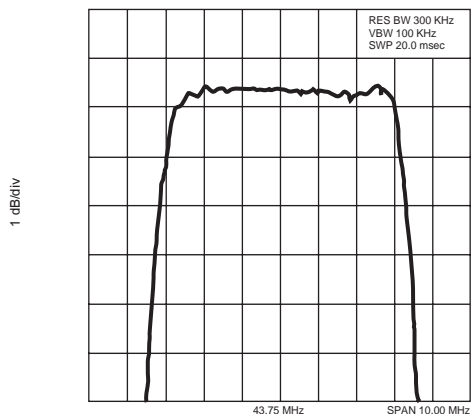| PIN NO.	PIN NAME	DESCRIPTION
1	GND	Ground. Provides low inductance to ground plane.
2	5V_Tx	Supply pin for the transmitter.
3	T_{XEN}	Enable pin for the power amplifier. The amplifier is shutdown when this pin is set low.
4	T_{XIN+}	Non-inverted TX input.
5	T_{XIN-}	Inverted TX input.
6	LD_Tx	Latch enable pin for the transmitter serial interface. TTL-compatible inputs.
7	NC	No Connection
8	5V_Rx	Supply pin for the receiver.
9	IF_{AGC}	The AGC pin is used to adjust gain in the IF amplifier. The pin has a positive gain vs. voltage slope. 45 dB of gain control is available by the varying the voltage from 0 to 3.3 V.
10	GND	Ground. Provides low inductance to ground plane.
11	CLOCK	Clock pin. High impedance CMOS input.
12	DATA	Serial data pin. High impedance CMOS input. MSB entered first.
13	LD_Rx	Latch enable pin for the dual P_{LL}. High impedance CMOS input. When LE goes HIGH, data stored in the shift registers is loaded into one of the 4 latches determined by the 2 control bits.
14	GND	Ground. Provides low inductance to ground plane.
15	IF-	Inverted final IF output.
16	IF+	Non-inverted final IF output.

FIGURE 1
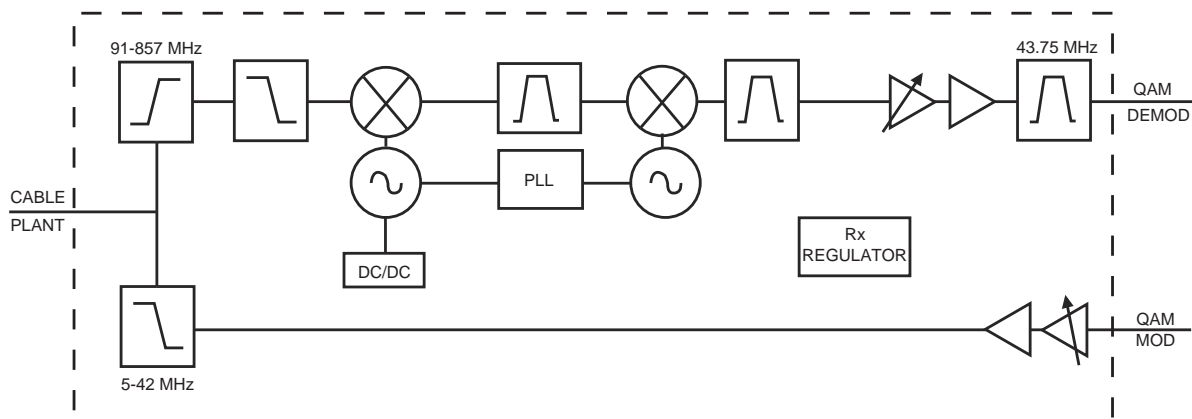
APPLICATION INTERFACE CIRCUIT

ISG4042/ TEXAS INSTRUMENTS TNET 4042

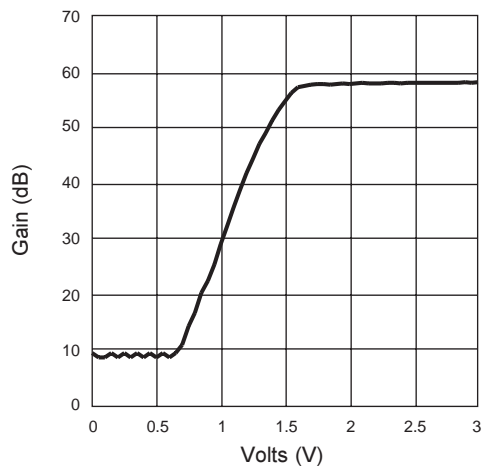**T1 TNET4042**   **ISG4042**

TYPICAL PERFORMANCE CURVES

PASSBAND AMPLITUDE RIPPLE

RES BW 300 KHz
VBW 100 KHz
SWP 20.0 msec

1 dB/div

43.75 MHz   SPAN 10.00 MHz

AGC RANGE

Gain (dB)

Volts (V)

PHASE NOISE (Narrowband)

REF = -15.00 dBm

RES BW 1.0 KHz
VBW 1 KHz
SWP 275 msec
P$_{NOISE}$ @ 10 KHz
= 85 dBc/Hz
MKR Δ = -54.71 dB

10 dB/div

43.75 MHz   SPAN 25 KHz

PHASE NOISE (Broadband)

REF = -22.00 dBm

RES BW 1.0 KHz
VBW 1 KHz
SWP 625 msec
P$_{NOISE}$ @ 100 KHz
= 109 dBc/Hz
MKR Δ = -79.31 dB

10 dB/div

43.75 MHz   SPAN 250 KHz
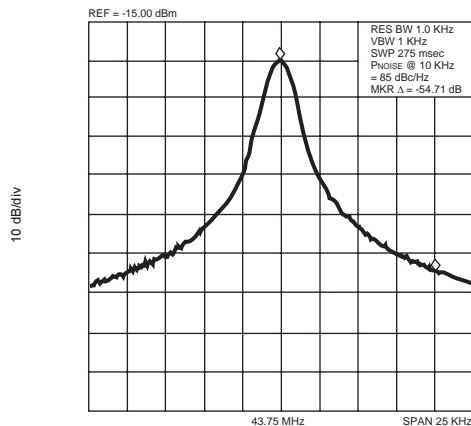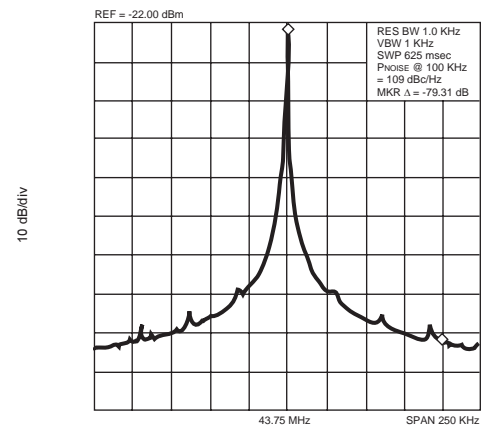
TX DIPLEXER RESPONSE

Gain (dB)
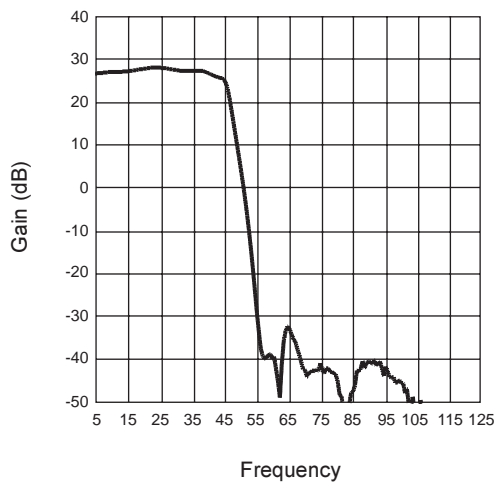
Frequency

CONVERSION vs. FREQUENCY

Conversion Gain (dB)

25º C

70º C

Frequency (MHz)
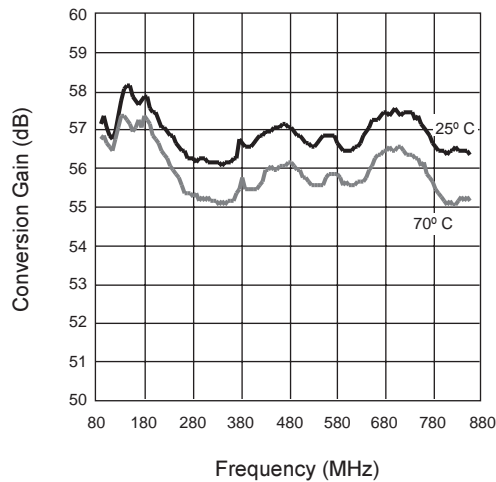
OUTLINE DIMENSIONS (Units in mm)
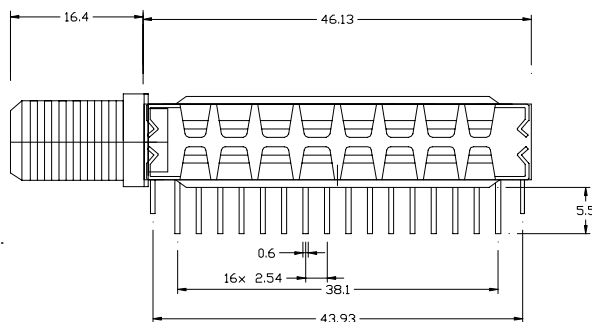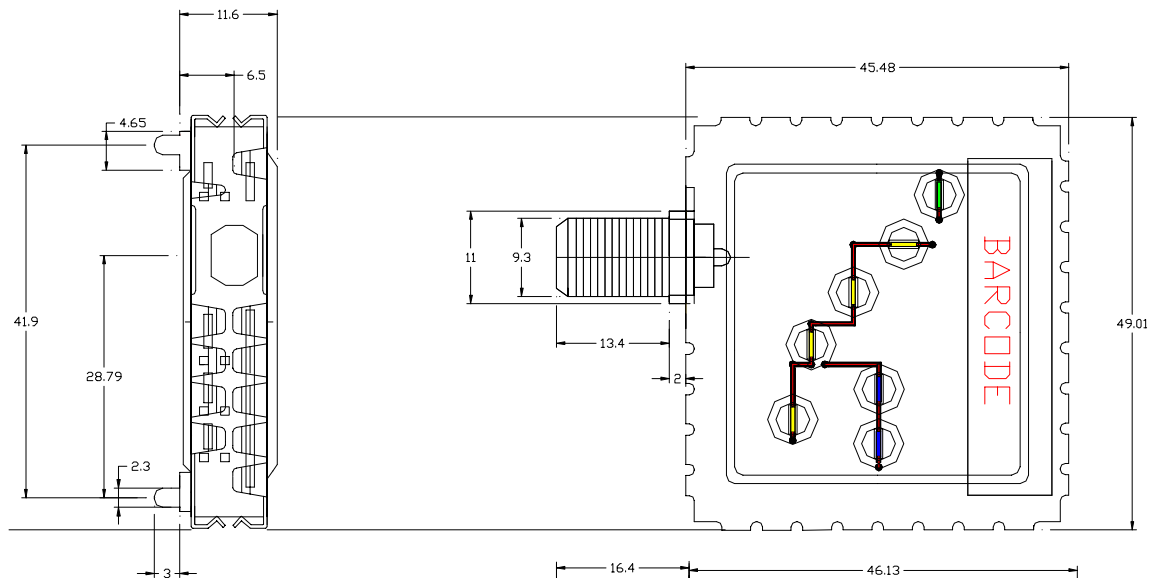
Notes:
1. All tolerance ±0.50 mm unless otherwise specified.

BARCODE

RECOMMENDED PAD LAYOUT

Ø3.0[Ø.1180] 4 PLS

Ø1.0[Ø0.0395] 16PLS

PIN1

2.54 16PLS
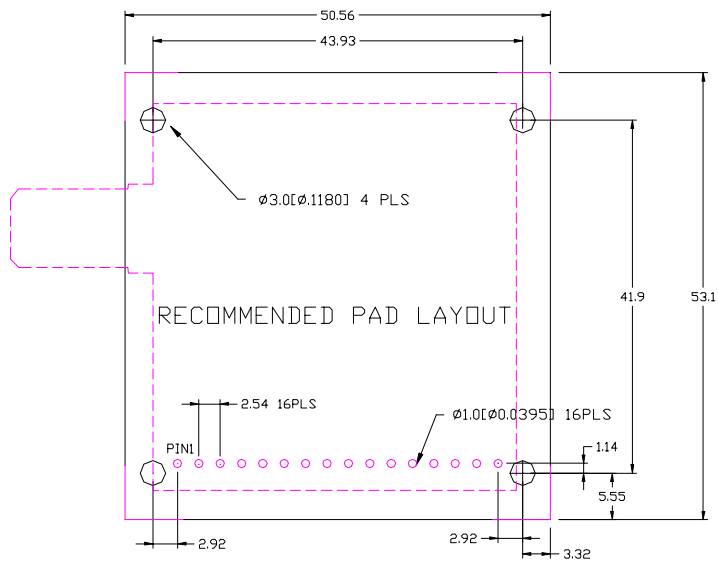
PROGRAMMING INFORMATION FOR RX

There are four 22-bit words needed to program the RX. PLL2 has the following words.

LSB   MSB

| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | R2 |

| 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | N2 |

PLL1 has the following words.

LSB   MSB

| 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | R1 |

| 1 | 1 | A | A | A | A | A | A | B | B | B | B | B | B | B | B | B | B | B | B | 0 | 0 | N1 |

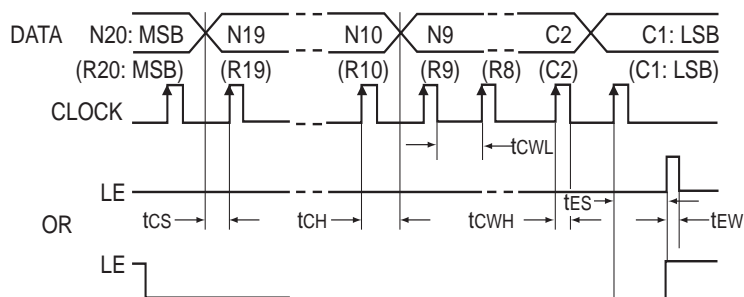Where $N = \left[\dfrac{\text{Tune Frequency (MHz)} + 1100}{0.25} \right]$

and

$B = \dfrac{N}{64} - \text{Mod} \left[\dfrac{N}{64} \right]$

$A = N - 64\,(B)$

They should be entered using the serial data input timing diagram below.

Serial Data Input Timing

Rx Timing Characteristics

SYMBOLS	PARAMETERS	VALUE			UNITS
		MIN	TYP	MAX	
V_{OH}	High-Level Output Voltage	4.1			V
V_{OL}	Low-Level Output Voltage			0.4	V
t_{CS}	Data to Clock Set Up Time	50			ns
t_{CH}	Data to Clock Hold Time	10			ns
t_{CWH}	Clock Pulse Width High	50			ns
t_{CWL}	Clock Pulse Width Low	50			ns
t_{ES}	Clock to Load Enable Set Up Time	50			ns
t_{EW}	Load Enable Pulse Width	50			ns

Notes:
1. Parenthesis data indicates programmable reference divider data.
2. Data shifted into register on clock rising edge.
3. Data is shifted in MSB first.
4. Pin 6 LD_TX held high.
Test Conditions:
The Serial Data Input Timing is tested using a symmetrical waveform around Vcc/2. The test waveform has an edge rate of 0.6V/ns with amplitudes of 2.2 V @ Vcc = 2.7 V and 2.6 V @ Vcc = 5.5 V.

PROGRAMMING INFORMATION FOR TX

Serial Interface

The serial interface has an active-low enable (LD_TX) to bracket the data, with data clocked in MSB first on the rising edge of CLK. Data is stored in the storage latch on the rising edge of LD_TX. The serial interface controls the state of the transmitter. Table 1 and 2 show the register format. Serial-interface timing is shown in Figure 2. LD_RX must not be toggled.

Functional Modes

There are three functional modes controlled through the serial interface or external pins (Table 2): transmit mode, transmit disable mode, and software shutdown mode.

Transmit Mode

Transmit mode is the normal active mode. The TXEN pin must be held high in this mode.

Transmit-Disable Mode

When in transmit-disable mode, the power amplifier is completely shut off. This mode is activated by taking TXEN low. This mode is typically used between bursts in TDMA systems. Transients are controlled by the action of the transformer balance.

High Power and Low Noise Modes

The upstream has two transmit modes, high power (HP) and low noise (LN) Each of these modes is actuated by the high-order bit D7 of the 8 bit programming word. When D7 is a logic 0, LN mode is enabled.

Each of these modes is characterized by activation of a distinct output stage. In HP mode, the output stage exhibits 15 dB higher gain than LN mode. The lower gain of the LN output stage allows for significantly lower output noise and lower transmit-disable transients.

The full range of gain codes (D6-D0) may be used in either mode. For DOCSIS applications, HP mode is recommended for output levels at or above +42 dBmV (D7 = 1, gain code = 87), LN mode when the output level is below +42 dBmV (D7 = 0, gain code = 115).

Figure 2. Serial-Interface Timing Diagram.

A. t_{SENS}
B. t_{SDAS}
C. t_{SDAH}
D. t_{SCKL}
E. t_{SCKH}
F. t_{SENH}
G. t_{DATAH}/t_{DATAL}

Tx Timing Characteristics

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
SEN to SCLK Setup Time	t_{SENS}	20			ns
SEN to SCLK Hold Time	t_{SENH}	10			ns
SDA to SCLK Setup Time	t_{SDAS}	10			ns
SDA to SCLK Hold Time	t_{SDAH}	20			ns
SDA Pulse Width High	t_{DATAH}	50			ns
SDA Pulse Width Low	t_{DATAL}	50			ns
SCLK Pulse Width High	t_{SLKH}	50			ns
SCLK Pulse Width Low	t_{SLKL}	50			ns

Table 1. Serial-Interface Control Word

BIT	MNEMONIC	DESCRIPTION
MSB 7	D7	High-power/low-noise mode select
6	D6	Gain Control, Bit 6
5	D5	Gain Control, Bit 5
4	D4	Gain Control, Bit 4
3	D3	Gain Control, Bit 3
2	D2	Gain Control, Bit 2
1	D1	Gain Control, Bit 1
LSB 0	D0	Gain Control, Bit 0

Table 2. Chip-State Control Bits

TXEN	D7	D6	D5	D4	D3	D2	D1	D0	GAIN STATE (DECIMAL)	GAIN (DB)	STATES
X	X	X	X	X	X	X	X	X			Shutdown Mode
0	X	X	X	X	X	X	X	X			Transmit-Disable Mode
1	1	X	X	X	X	X	X	X			Transmit Mode-Enable Mode, High Power
1	0	X	X	X	X	X	X	X			Transmit Mode-Enable Mode, Low Noise
1	0	0	1	1	0	0	0	0	48	-26	
1	0	1	0	1	0	0	0	0	80	-10	
1	0	1	1	1	0	0	1	1	115	8	
1	1	1	0	1	0	1	1	1	87	9	
1	1	1	1	0	1	1	1	0	110	20	
1	1	1	1	1	1	1	0	1	125	28	

* Typical gain at +25°C and V_{CC} = +5 V.