

# ISG4042EU-T

## 5 V CATV MODEM RF TUNER AND TRANSMITTER



### FEATURES

- **TOWAY EURO DOCSIS BASED DESIGN:**  
112-858 MHz Downstream  
5-65 MHz Upstream
- **SINGLE SUPPLY 5 V OPERATION:**  
With Built-in Linear Regulation
- **SINGLE AGC CONTROL**  
Simplifies Modem Calibration
- **ULTRA SMALL SIZE:**  
1.9 x 2.0 x 0.5 in., 1.9 in<sup>3</sup>  
46.2 x 49.0 x 12.5 mm., 28.5 cc.
- **DIGITAL LINEAR RF TRANSMITTER:**  
All Harmonics -55 dBc @ 58 dBmV (see note 2)  
≥ 56 dB Gain Range (0.5 dB steps)
- **INTERFACES DIRECTLY WITH QAM MOD/DEMOCIC's:**  
(see note 3)

### DESCRIPTION AND APPLICATIONS

The ISG4042EU-T is an RF tuner/transmitter designed for use in EURO DOCSIS cable modem applications. It is a complete solution that interfaces directly with QAM Mod/Demod IC's. The tuner/transmitter integrates a diplex filter, dual conversion receiver, transmit AGC amplifier, and other RF filtering (see Figure 1). The diplex filter provides over 40 dB of isolation between the Tx band and the Rx band. The receiver channel selects and converts QAM signals in the Rx band down to the IF sampling frequency. It also provides the necessary gain control to adjust the input power to the DSP chip. The RF transmitter section provides ≥ 56 dB of digitally controlled range while maintaining excellent linearity performance.

### ELECTRICAL CHARACTERISTICS (V<sub>CC</sub> = 5 V, ±2 %, T<sub>A</sub> = 25°C) (see note 4)

SYMBOLS	PARAMETERS	UNITS	MIN	TYP	MAX
<b>RF Performance (Rx)</b>					
fOP	Operating Frequency Range (Center to Center)	MHz	112		858
	Input Signal Level	dBmV	-15		15
	Maximum Voltage Gain	dB		57	
	Automatic Voltage Gain Control Range	dB	45		
VAGC	IF Automatic Voltage Gain Control	V	0		3.3
NFMAX	Noise Figure (at Max Voltage Gain)	dB		8	10
	Phase Noise at 10 kHz Offset	dBc/Hz		-85	-82
	LO Radiation at RF Input	dBm		-40	
	Resolution	kHz		62.5	
	Lock Time (end to end channel)	msec.		18	
	Input Impedance (Nominal)	ohms		75	
RLIN	Input Return Loss	dB	6		
	Channel Bandwidth	MHz		8	
	Output Frequency	MHz		36.125	
	Passband Ripple over 6.952 MHz Bandwidth	dB		1	2
	Image Rejection	dB	50		
	Inband Group Delay	ns			100
	CSO <sup>1</sup>	dBc	45	50	
	CTB <sup>1</sup>	dBc	45	50	
	Output Frequency Offset	kHz	-35		+35
	Output IF Voltage Level	VPP		1	
	Output IF Load	KΩ		1	

#### Notes:

1. 110 Channels at +15 dBmV/tone.
  2. 160K Symbol rate; under DOCSIS PHY - 17 high condition.
  3. Application specification for TI 4040/4042.
  4. Specifications apply to test conditions listed.
- \* PHY 7/17/18 Data available upon request.

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**ELECTRICAL CHARACTERISTICS** ( $V_{CC} = 5\text{ V}$ ,  $\pm 2\%$ ,  $T_A = 25^\circ\text{C}$ ) (see note 2)

SYMBOLS	PARAMETERS	UNITS	MIN	TYP	MAX
<b>RF Performance (Tx)</b>					
fOP	Operating Frequency Range	MHz	5		65
	G <sub>MAX</sub> (Gain Word = 255)	dB	26	27	
	G <sub>MIN</sub> (Gain Word = 48)	dB		-27	-26
	Output Step Size	dB		0.5	
	Flatness (5 to 65 MHz)	dB		1.7	2.5
	Amplitude Ripple Over 1.28 MHz	dB			0.6
	2nd Harmonic Level (F <sub>IN</sub> = 65 MHz, P <sub>OUT</sub> = +58 dBmV) <sup>1</sup>	dBmV		-48	-45
	3rd Harmonic Level (F <sub>IN</sub> = 65 MHz, P <sub>OUT</sub> = +58 dBmV) <sup>1</sup>	dBmV		-48	-45
	Input Impedance	Ω		300	
RL <sub>OUT</sub>	Output Return Loss	dB	6.0		
TX ON/OFF	On/Off Setting Time	μs		3.2	5
	Group Delay (5-65 MHz)	ns			100
	Tx Transient Spurs	mV			7
	Tx Transient Duration	μs		3.2	5
<b>Power Requirements</b>					
	Supply Voltage V1 Rx	V	4.75	5	5.25
	Supply Voltage V1 Tx	V	4.75	5	5.25
	Supply Ripple Voltage V1 Rx	mV			100
<b>Supply Current</b>					
I <sub>CC1</sub> (Rx)	Supply Current 1 (Rx)	mA		310	
I <sub>CC1</sub> (Tx)	Supply Current 1 (Tx) TXEN = High	mA		120	150
	Supply Current 1 (Tx) TXEN = Low	mA		8	12
<b>Physical Interface</b>					
	To the CATV Network			Female F-Connector	
	To the Motherboard			16 Pin Header	

## Notes:

- 160K Symbol rate; under DOCSIS PHY - 17 high condition.
- Specifications apply to test conditions listed.

**ABSOLUTE MAXIMUM RATINGS**(T<sub>c</sub> = 25°C unless otherwise noted)

SYMBOLS	PARAMETERS	UNITS	RATINGS
V <sub>IN</sub>	RF Input Voltage	dBmV	60
V <sub>CC1</sub> (Rx)	Supply Voltage (Rx)	V	+6.5
V <sub>CC</sub> (Tx)	Supply Voltage (Tx)	V	+5.5
T <sub>OP</sub>	Operating Temperature	°C	-40 to 75
T <sub>STG</sub>	Storage Temperature	°C	-40 to 75
T <sub>SOL</sub>	Soldering Temperature	°C	260
t <sub>SOL</sub>	Soldering Time	sec.	4

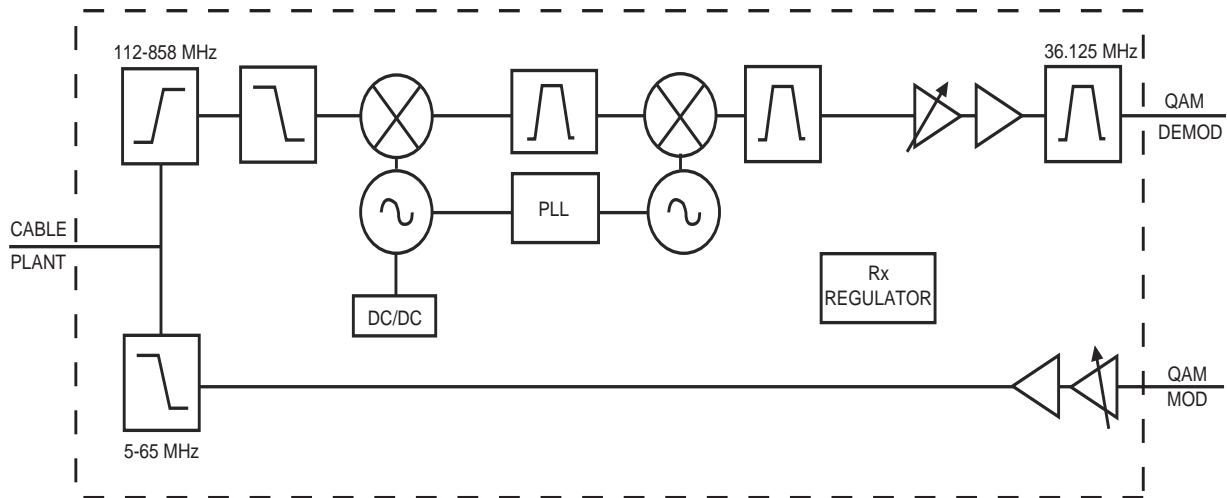
## Note:

- Operation in excess of any one of these parameters may result in permanent damage.

**PIN FUNCTIONS**

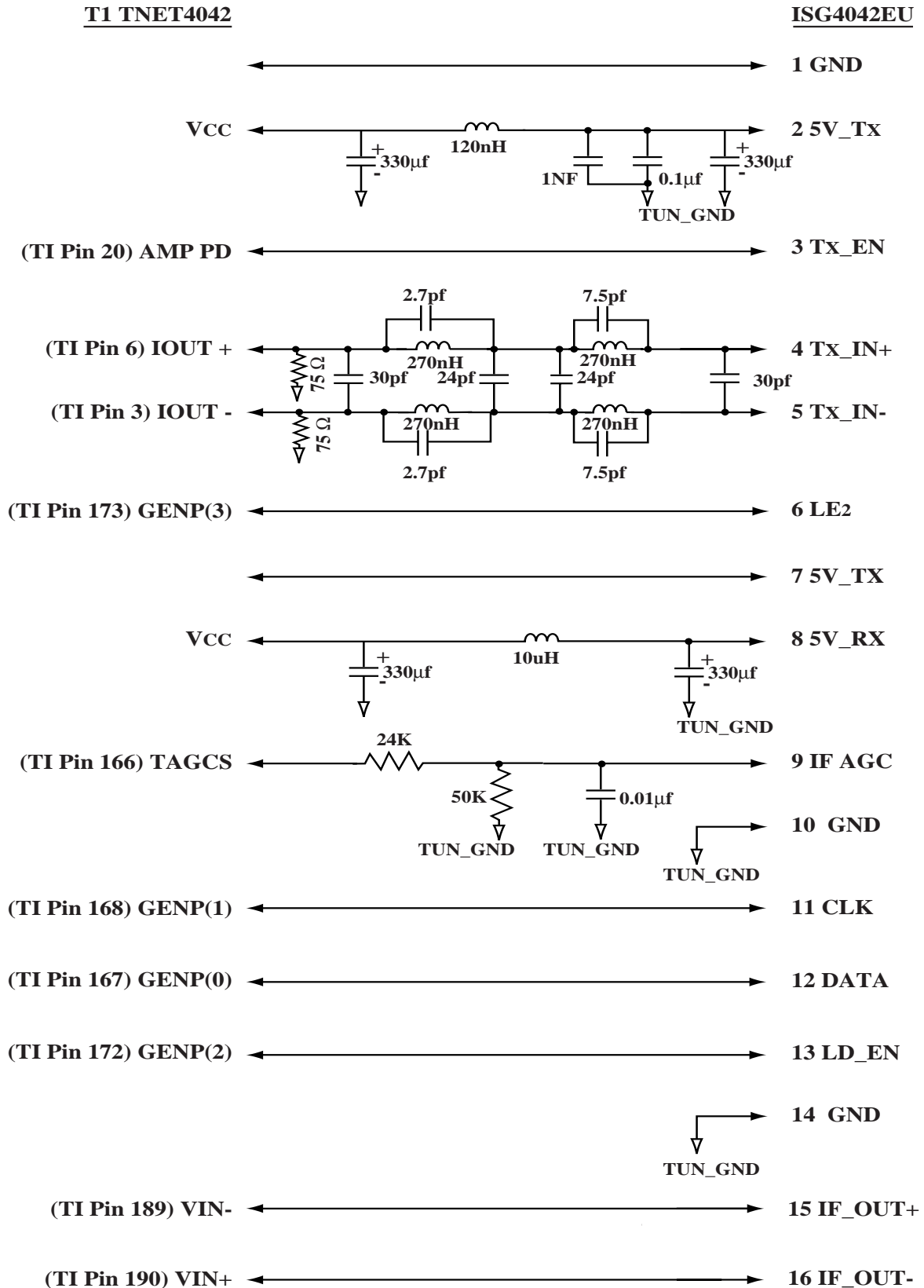
PIN NO.	PIN NAME	DESCRIPTION
1	GND	Ground. Provides low inductance to ground plane.
2	5V_Tx	Supply pin for the transmitter.
3	TXEN	Enable pin for the power amplifier. The amplifier is shutdown when this pin is set low.
4	TXIN+	Non-inverted TX input.
5	TXIN-	Inverted TX input.
6	LD_Tx	Latch enable pin for the transmitter serial interface. TTL-compatible inputs.
7	NC	No Connection
8	5V_Rx	Supply pin for the receiver.
9	IFAGC	The AGC pin is used to adjust gain in the IF amplifier. The pin has a positive gain vs. voltage slope. 45 dB of gain control is available by the varying the voltage from 0 to 3.3 V.
10	GND	Ground. Provides low inductance to ground plane.
11	CLOCK	Clock pin . High impedance CMOS input.
12	DATA	Serial data pin. High impedance CMOS input. MSB entered first.
13	LD_Rx	Latch enable pin for the dual PLL. High impedance CMOS input. When LE goes HIGH, data stored in the shift registers is loaded into one of the 4 latches determined by the 2 control bits.
14	GND	Ground. Provides low inductance to ground plane.
15	IF-	Inverted final IF output.
16	IF+	Non-inverted final IF output.

**FIGURE 1**



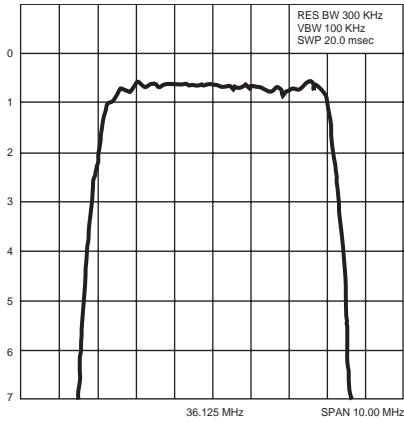
**APPLICATION INTERFACE CIRCUIT**

**ISG4042/ TEXAS INSTRUMENTS TNET 4042**

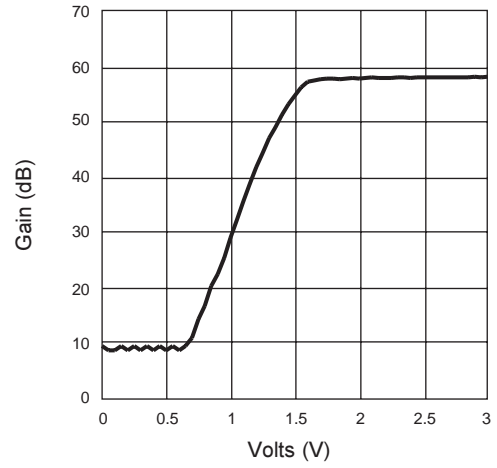


TYPICAL PERFORMANCE CURVES

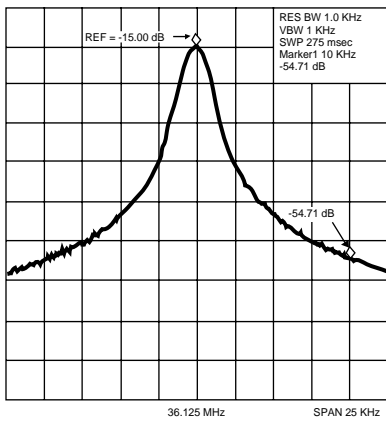
PASSBAND AMPLITUDE RIPPLE



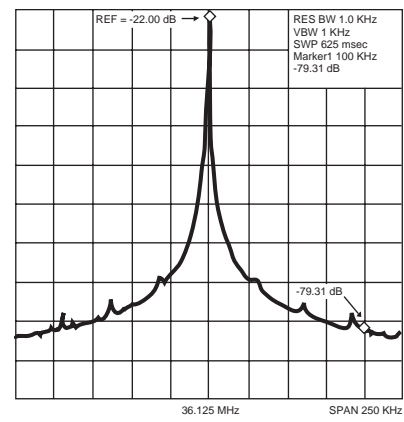
AGC RANGE



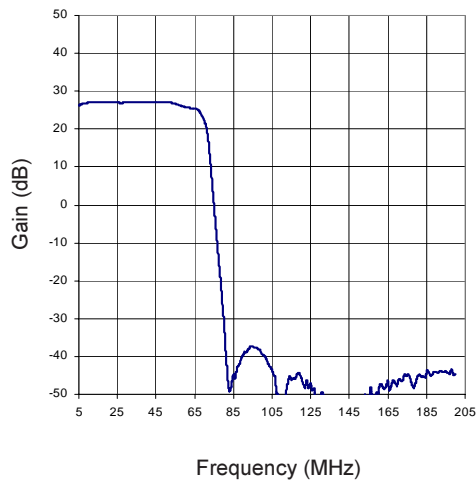
PHASE NOISE



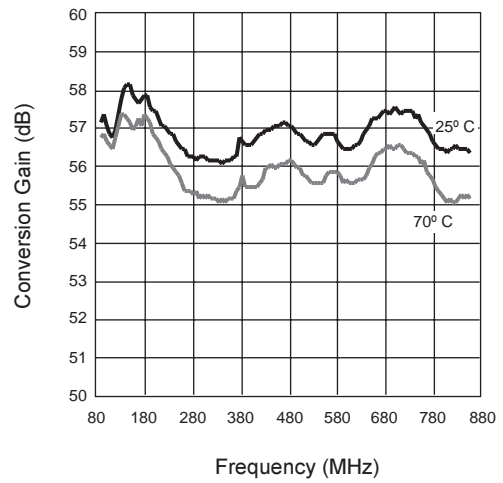
PHASE NOISE



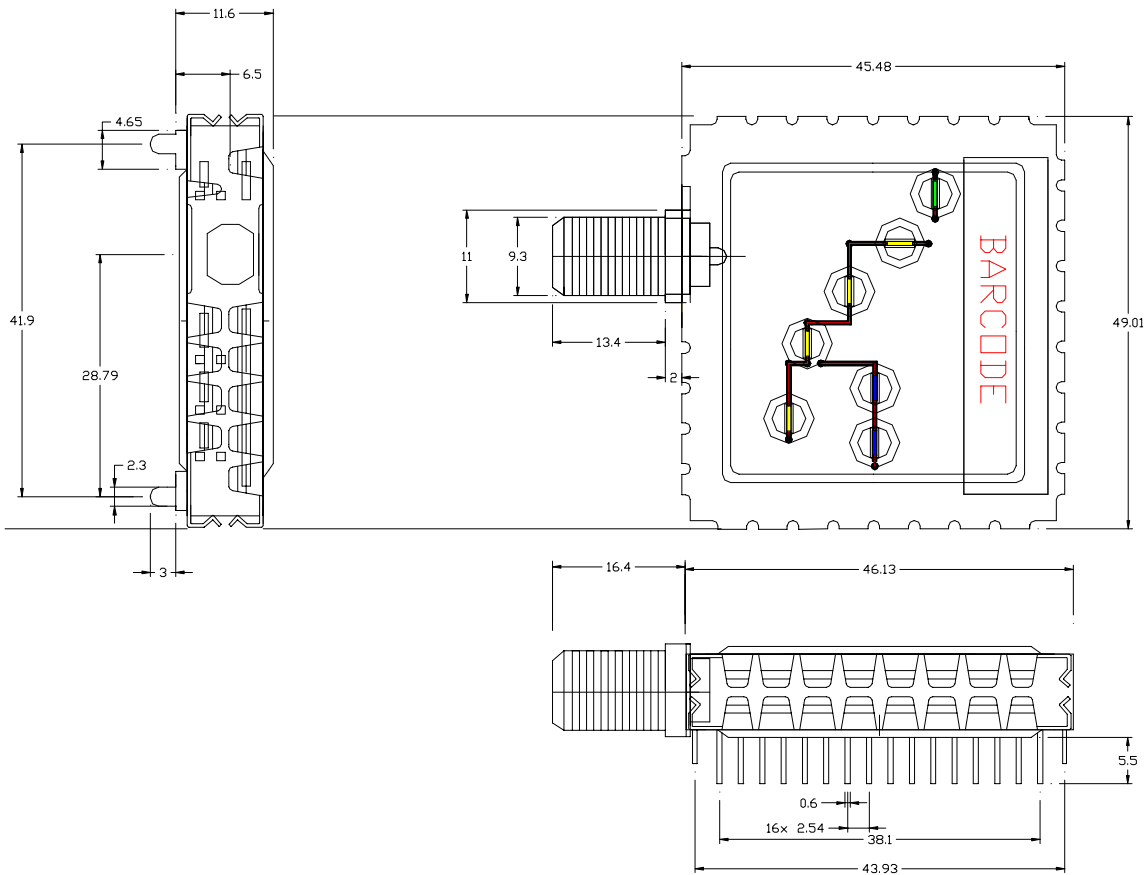
TX DIPLEXER RESPONSE



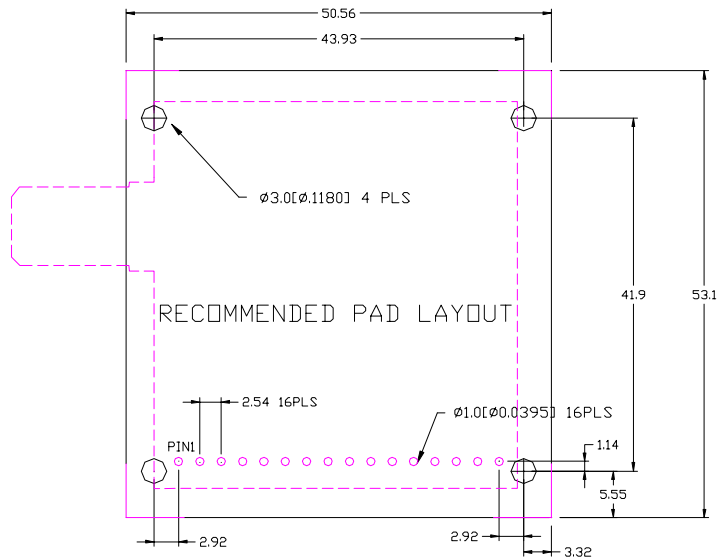
CONVERSION vs. FREQUENCY



**OUTLINE DIMENSIONS** (Units in mm)



Notes:  
 1. All tolerance  $\pm 0.50$  mm unless otherwise specified.



## PROGRAMMING INFORMATION FOR RX

There are four 22-bit words needed to program the RX. PLL2 has the following words.

LSB	MSB
0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 1 1 0 0	R2
1 0 0 0 0 1 0 0 0 0 0 0 0 1 0 0 0 0 1 0 0 1	N2

PLL1 has the following words.

LSB	MSB
0 1 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	R1
1 1 A A A A A A A A B B B B B B B B B B 0 0	N1

$$\text{Where } N = \left\lceil \frac{\text{Tune Frequency (MHz)} + 1100}{0.25} \right\rceil$$

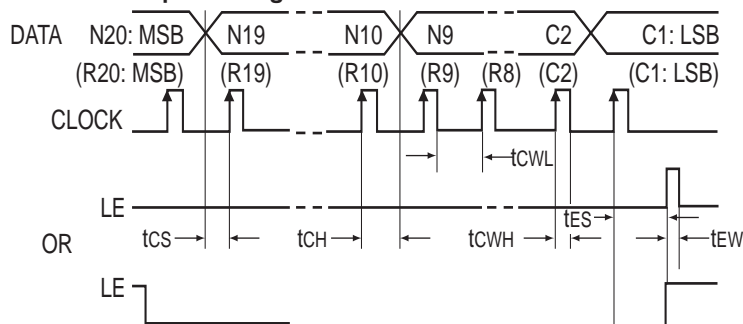
and

$$B = \frac{N}{64} - \text{Mod} \left\lceil \frac{N}{64} \right\rceil$$

$$A = N - 64 (B)$$

They should be entered using the serial data input timing diagram below.

### Serial Data Input Timing



### Rx Timing Characteristics

SYMBOLS	PARAMETERS	VALUE			UNITS
		MIN	TYP	MAX	
V <sub>OH</sub>	High-Level Output Voltage	4.1			V
V <sub>OL</sub>	Low-Level Output Voltage			0.4	V
t <sub>CS</sub>	Data to Clock Set Up Time	50			ns
t <sub>CH</sub>	Data to Clock Hold Time	10			ns
t <sub>CWH</sub>	Clock Pulse Width High	50			ns
t <sub>CWL</sub>	Clock Pulse Width Low	50			ns
t <sub>ES</sub>	Clock to Load Enable Set Up Time	50			ns
t <sub>EW</sub>	Load Enable Pulse Width	50			ns

Notes:

1. Parenthesis data indicates programmable reference divider data.
2. Data shifted into register on clock rising edge.
3. Data is shifted in MSB first.
4. Pin 6 LD\_TX held high.

Test Conditions:

The Serial Data Input Timing is tested using a symmetrical waveform around V<sub>CC</sub>/2. The test waveform has an edge rate of 0.6V/ns with amplitudes of 2.2 V @ V<sub>CC</sub> = 2.7 V and 2.6 V @ V<sub>CC</sub> = 5.5 V.

## PROGRAMMING INFORMATION FOR TX

### Serial Interface

The serial interface has an active-low enable (LD\_TX) to bracket the data, with data clocked in MSB first on the rising edge of CLK. Data is stored in the storage latch on the rising edge of LD\_TX. The serial interface controls the state of the transmitter. Table 1 and 2 show the register format. Serial-interface timing is shown in Figure 2. LD\_RX must not be toggled.

### Functional Modes

There are three functional modes controlled through the serial interface or external pins (Table 2): transmit mode, transmit disable mode, and software shutdown mode.

### Transmit Mode

Transmit mode is the normal active mode. The TXEN pin must be held high in this mode.

### Transmit-Disable Mode

When in transmit-disable mode, the power amplifier is completely shut off. This mode is activated by taking TXEN low. This mode is typically used between bursts in TDMA systems. Transients are controlled by the action of the transmitter balance.

### High Power and Low Noise Modes

The upstream has two transmit modes, high power (HP) and low noise (LN). Each of these modes is actuated by the high-order bit D7 of the 8 bit programming word. When D7 is a logic 0, LN mode is enabled.

Each of these modes is characterized by activation of a distinct output stage. In HP mode, the output stage exhibits 15 dB higher gain than LN mode. The lower gain of the LN output stage allows for significantly lower output noise and lower transmit-disable transients.

The full range of gain codes (D6-D0) may be used in either mode. For DOCSIS applications, HP mode is recommended for output levels at or above +42 dBmV (D7 = 1, gain code = 87), LN mode when the output level is below +42 dBmV (D7 = 0, gain code = 115).

Table 2. Chip-State Control Bits

TXEN	D7	D6	D5	D4	D3	D2	D1	D0	GAIN STATE (DECIMAL)	GAIN (DB)	STATES
X	X	X	X	X	X	X	X	X			Shutdown Mode
0	X	X	X	X	X	X	X	X			Transmit-Disable Mode
1	1	X	X	X	X	X	X	X			Transmit Mode-Enable Mode, High Power
1	0	X	X	X	X	X	X	X			Transmit Mode-Enable Mode, Low Noise
1	0	0	1	1	0	0	0	0	48	-26	
1	0	1	0	1	0	0	0	0	80	-10	
1	0	1	1	1	0	0	1	1	115	8	
1	1	1	0	1	0	1	1	1	87	9	
1	1	1	1	0	1	1	1	0	110	20	
1	1	1	1	1	1	1	0	1	125	28	

\* Typical gain at +25°C and V<sub>cc</sub> = +5 V.

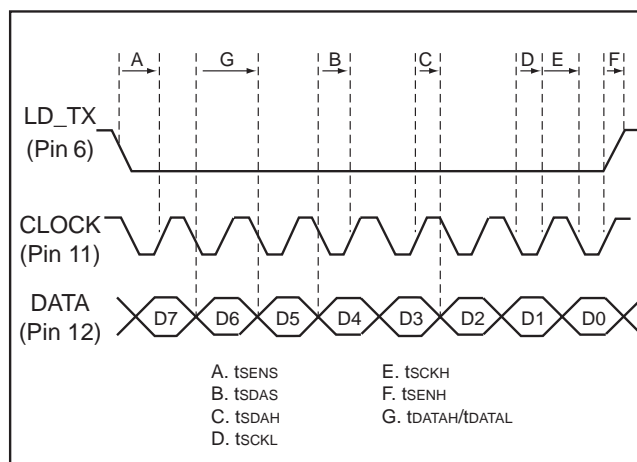


Figure 2. Serial-Interface Timing Diagram.

### Tx Timing Characteristics

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
SEN to SCLK Setup Time	tSENS	20			ns
SEN to SCLK Hold Time	tSENH	10			ns
SDA to SCLK Setup Time	tSDAS	10			ns
SDA to SCLK Hold Time	tSDAH	20			ns
SDA Pulse Width High	tDATAH	50			ns
SDA Pulse Width Low	tDATAL	50			ns
SCLK Pulse Width High	tSLKH	50			ns
SCLK Pulse Width Low	tSLKL	50			ns

Table 1. Serial-Interface Control Word

BIT	MNEMONIC	DESCRIPTION
MSB 7	D7	High-power/low-noise mode select
6	D6	Gain Control, Bit 6
5	D5	Gain Control, Bit 5
4	D4	Gain Control, Bit 4
3	D3	Gain Control, Bit 3
2	D2	Gain Control, Bit 2
1	D1	Gain Control, Bit 1
LSB 0	D0	Gain Control, Bit 0