MC100EP809

3.3V 1:9 Differential HSTL/PECL to HSTL Clock Driver with LVTTL Clock Select and Enable

The MC100EP809 is a low skew 1–to–9 differential clock driver, designed with clock distribution in mind, accepting two clock sources into an input multiplexer. The part is designed for use in low voltage applications which require a large number of outputs to drive precisely aligned low skew signals to their destination. The two clock inputs are differential HSTL or PECL and they are selected by the CLK_SEL pin which is LVTTL. To avoid generation of a runt clock pulse when the device is enabled/disabled, the Output Enable (OE), which is LVTTL, is synchronous ensuring the outputs will only be enabled/disabled when they are already in LOW state (See Figure 8).

The MC100EP809 guarantees low output–to–output skew. The optimal design, layout, and processing minimize skew within a device and from lot to lot. The MC100EP809 output structure uses open emitter architecture and will be terminated with 50 Ω to ground instead of a standard HSTL configuration (See Figure 6). To ensure the tight skew specification is realized, both sides of the differential output need to be terminated identically into 50 Ω even if only one output is being used. If an output pair is unused, both outputs may be left open (unterminated) without affecting skew.

Designers can take advantage of the EP809's performance to distribute low skew clocks across the backplane of the board. HSTL clock inputs may be driven single–end by biasing the non–driven pin in an input pair (see Figure 7).

- 100 ps Typical Device–to–Device Skew
- 15 ps Typical Within Device Skew
- HSTL Compatible Outputs Drive 50 Ω to Ground with no Offset Voltage
- Maximum Frequency > 750 MHz
- 850 ps Typical Propagation Delay
- Fully Compatible with Micrel SY89809L
- PECL and HSTL Mode Operating Range: V_{CCI} = 3 V to 3.6 V with GND = 0 V, V_{CCO} = 1.6 V to 2.0 V
- Open Input Default State

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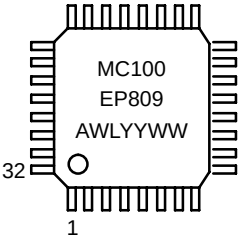
MARKING DIAGRAM*

32–LEAD LQFP
FA SUFFIX
CASE 873A

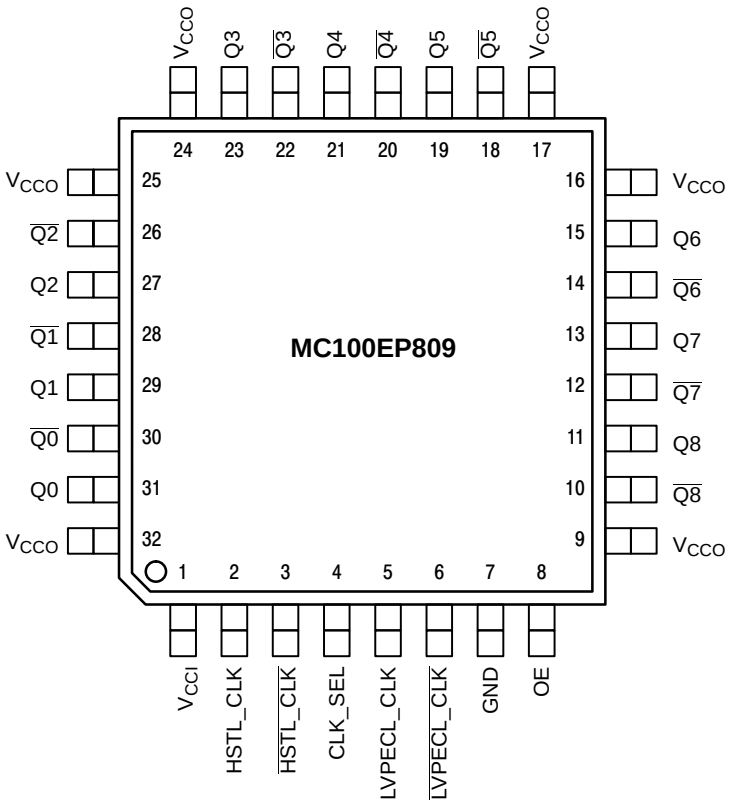


A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

*For additional information, see Application Note AND8002/D

ORDERING INFORMATION

Device	Package	Shipping
MC100EP809FA	LQFP–32	250 Units/Tray
MC100EP809FAR2	LQFP–32	2000/Tape & Reel



All V_{CCI}, V_{CCO}, and GND pins must be externally connected to appropriate Power Supply to guarantee proper operation ($V_{CCI} \neq V_{CCO}$).

Figure 1. 32–Lead LQFP Pinout (Top View)

PIN DESCRIPTION

PIN	FUNCTION
HSTL_CLK*, $\overline{\text{HSTL\_CLK}}$**	HSTL or LVDS Differential Inputs
LVPECL_CLK*, $\overline{\text{LVPECL\_CLK}}$**	LVPECL Differential Inputs
CLK_SEL**	LVCMOS/LVTTL Input CLK Select
OE**	LVCMOS/LVTTL Output Enable
Q0–Q8, $\overline{\text{Q0–Q8}}$	HSTL Differential Outputs
V_{CCI}	Positive Supply_Core (3.0 V – 3.6 V)
V_{CCO}	Positive Supply_HSTL Outputs (1.6 V – 2.0 V)
GND	Ground

* Pins will default LOW when left open.
** Pins will default HIGH when left open.

FUNCTION TABLE

OE*	CLK_SEL	Q0–Q8	$\overline{\text{Q0–Q8}}$
L	L	L	H
L	H	L	H
H	L	HSTL_CLK	$\overline{\text{HSTL\_CLK}}$
H	H	LVPECL_CLK	$\overline{\text{LVPECL\_CLK}}$

* The OE (Output Enable) signal is synchronized with the rising edge of the HSTL_CLK and LVPECL_CLK signal.

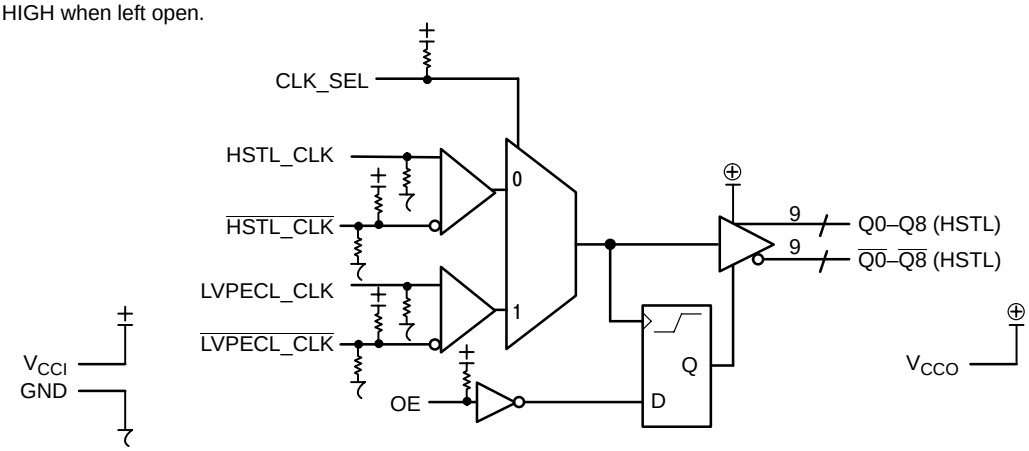


Figure 2. Logic Diagram

ATTRIBUTES

Characteristics		Value
Internal Input Pulldown Resistor		75 kΩ
Internal Input Pullup Resistor		37.5 kΩ
ESD Protection	Human Body Model Machine Model Charged Device Model	> 2 kV > 200 V > 2 kV
Moisture Sensitivity (Note 1)		Level 2
Flammability Rating	Oxygen Index: 28 to 34	UL 94 V–0 @ 0.125 in
Transistor Count		478 Devices
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test		

1. For additional information, refer to Application Note AND8003/D.

MAXIMUM RATINGS (Note 2)

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V_{CCI}	Core Power Supply	GND= 0 V	V_{CCO}= 1.8 V	4	V
V_{CCO}	HSTL Output Power Supply	GND= 0 V	V_{CCI} = 3.3 V	4	V
V_I	PECL Mode Input Voltage	GND = 0 V	$V_I \le V_{CCI}$	6	V
I_{out}	Output Current	Continuous Surge		50 100	mA mA
T_A	Operating Temperature Range			0 to +85	°C
T_{stg}	Storage Temperature Range			–65 to +150	°C
θ_{JA}	Thermal Resistance (Junction–to–Ambient)	0 LFPM 500 LFPM	32 LQFP 32 LQFP	80 55	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction–to–Case)	std bd	32 LQFP	12 to 17	°C/W
T_{sol}	Wave Solder	< 2 to 3 sec @ 248°C		265	°C

2. Maximum Ratings are those values beyond which device damage may occur.

LVPECL DC CHARACTERISTICS V_{CCI} = 3.0 V to 3.6 V; V_{CCO} = 1.6 V to 2.0 V, GND = 0 V

		0°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{CC}	Core Power Supply Current	75	95	115	75	95	115	75	95	115	mA
V_{IH}	Input HIGH Voltage (Single–Ended)	V_{CCI}– 1.165		V_{CCI} –0.88	V_{CCI}– 1.165		V_{CCI} –0.88	V_{CCI}– 1.165		V_{CCI} –0.88	V
V_{IL}	Input LOW Voltage (Single–Ended)	V_{CCI}– 1.945		V_{CCI} –1.6	V_{CCI}– 1.945		V_{CCI} –1.6	V_{CCI}– 1.945		V_{CCI} –1.6	V
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 3) (Figure 4) LVPECL_CLK/$\overline{\text{LVPECL\_CLK}}$	1.2		V_{CCI}	1.2		V_{CCI}	1.2		V_{CCI}	V
I_{IH}	Input HIGH Current	–150		150	–150		150	–150		150	μA
I_{IL}	Input LOW Current	–150		150	–150		150	–150		150	μA

NOTE: 100EP circuits are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

3. V_{IHCMR} max varies 1:1 with V_{CCI}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

LVTTL/LVCMOS DC CHARACTERISTICS V_{CCI} = 3.0 V to 3.6 V; V_{CCO} = 1.6 V to 2.0 V, GND = 0 V

Symbol	Characteristic	0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{IH}	Input HIGH Voltage	2.0			2.0			2.0			V
V_{IL}	Input LOW Voltage			0.8			0.8			0.8	V
I_{IH}	Input HIGH Current	–150		150	–150		150	–150		150	μA
I_{IL}	Input LOW Current	–300		300	–300		300	–300		300	μA

NOTE: 100EP circuits are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

HSTL DC CHARACTERISTICS V_{CCI} = 3.0 V to 3.6 V; V_{CCO} = 1.6 V to 2.0 V, GND = 0 V

Symbol	Characteristic	0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OH}	Output HIGH Voltage (Note 4)	1.0		1.2	1.0		1.2	1.0		1.2	V
V_{OL}	Output LOW Voltage (Note 4)	0.1		0.4	0.1		0.4	0.1		0.4	V
V_{IH}	Input HIGH Voltage (Figure 5)	V_X+0.1	–	1.6	V_X+0.1	–	1.6	V_X+0.1	–	1.6	V
V_{IL}	Input LOW Voltage (Figure 5)	–0.3	–	V_X–0.1	–0.3	–	V_X–0.1	–0.3	–	V_X–0.1	V
V_X	HSTL Input Crossover Voltage	0.68	–	0.9	0.68	–	0.9	0.68	–	0.9	V
I_{IH}	Input HIGH Current	–150		150	–150		150	–150		150	μA
I_{IL}	Input LOW Current	–300		300	–300		300	–300		300	μA
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 5) HSTL_CLK/$\overline{\text{HSTL\_CLK}}$	0.6		V_{CCI} –1.2	0.6		V_{CCI} –1.2	0.6		V_{CCI} –1.2	V V

NOTE: 100EP circuits are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

4. All outputs loaded with 50 Ω to GND (See Figure 6).
5. V_{IHCMR} max varies 1:1 with V_{CCI}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

AC CHARACTERISTICS V_{CCI} = 3.0 V to 3.6 V; V_{CCO} = 1.6 V to 2.0 V, GND = 0 V (Note 6)

Symbol	Characteristic	0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{Opp}	Differential Output Voltage (Figure 3) f_{out} < 100 MHz f_{out} < 500 MHz f_{out} < 750 MHz	600 600 450	850 750 575		600 600 450	850 750 575		600 600 450	850 750 575		mV mV
t_{PLH} t_{PHL}	Propagation Delay (Differential) LVPECL_CLK to Q HSTL_CLK to Q	 680 690	 800 830	 930 990	 700 700	 820 850	 950 1000	 780 790	 920 950	 1070 1110	 ps ps
t_{skew}	Within–Device Skew (Note 7) Device–to–Device Skew (Note 8)		15 100	50 200		15 100	50 200		15 100	50 200	ps ps
t_{JITTER}	Random Clock Jitter (Figure 3) (RMS)		1.4	3.0		1.4	3.0		1.4	3.0	ps
V_{PP}	Input Swing (Differential Mode) (Note 10) (Figure 4) LVPECL HSTL	200 200			200 200			200 200			mV mV
t_S	OE Set Up Time (Note 9)	0.5			0.5			0.5			ns
t_H	OE Hold Time	0.5			0.5			0.5			ns
t_r/t_f	Output Rise/Fall Time (20%–80%)	350		600	350	450	600	350		600	ps

6. Measured with 750 mV (LVPECL) source or 1 V (HSTL) source, 50% duty cycle clock source. All outputs loaded with 50 Ω to Ground (See Figure 6).
7. Skew is measured between outputs under identical transitions and conditions on any one device.
8. Device–to–Device skew for identical transitions and conditions.
9. OE Set Up Time is defined with respect to the rising edge of the clock. OE High–to–Low transition ensures outputs remain disabled during the next clock cycle. OE Low–to–High transition enables normal operation of the next input clock (See Figure 8).
10. V_{PP} is the Differential Input Voltage swing required to maintain AC characteristics listed herein.

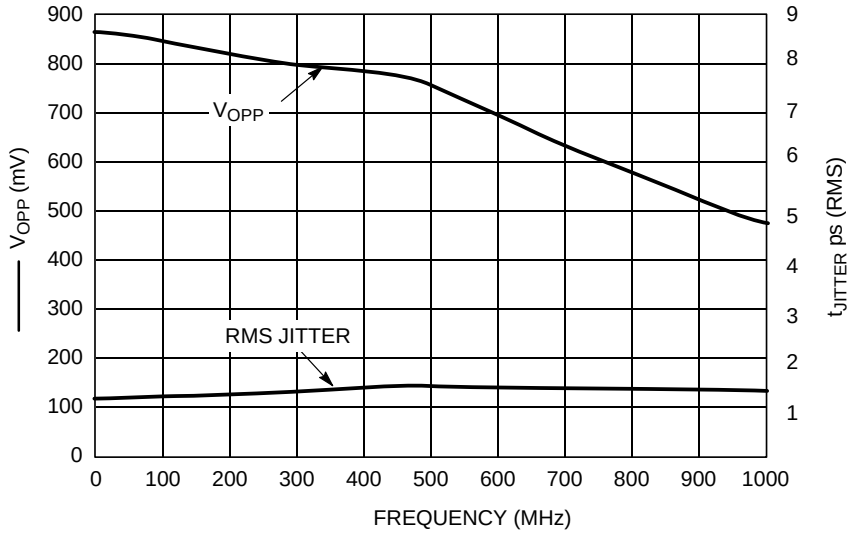


Figure 3. Output Frequency (F_{OUT}) versus Output Voltage (V_{OPP}) and Random Clock Jitter (t_{JITTER})

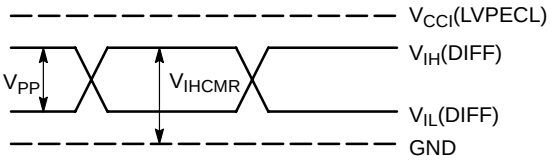


Figure 4. LVPECL Differential Input Levels

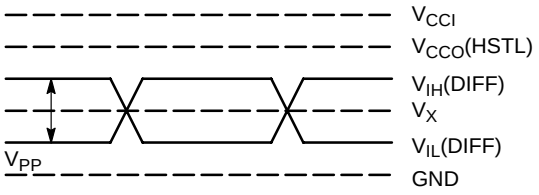


Figure 5. HSTL Differential Input Levels

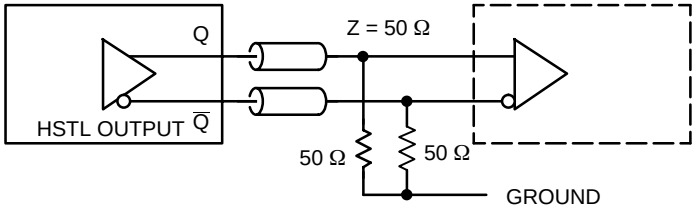
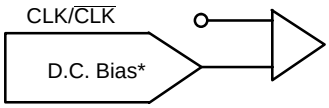


Figure 6. HSTL Output Termination and AC Test Reference



*Must fall within 680 to 900 mV (Preferably (V_{IH} + V_{IL})/2).

Figure 7. HSTL Single–Ended Input Configuration

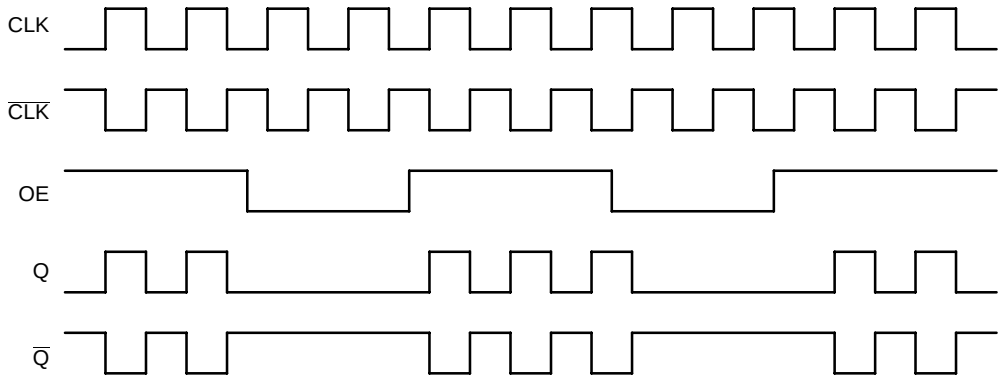


Figure 8. Output Enable (OE) Timing Diagram

Resource Reference of Application Notes

AN1405 – ECL Clock Distribution Techniques

AN1406 – Designing with PECL (ECL at +5.0 V)

AND8002 – Marking and Date Codes

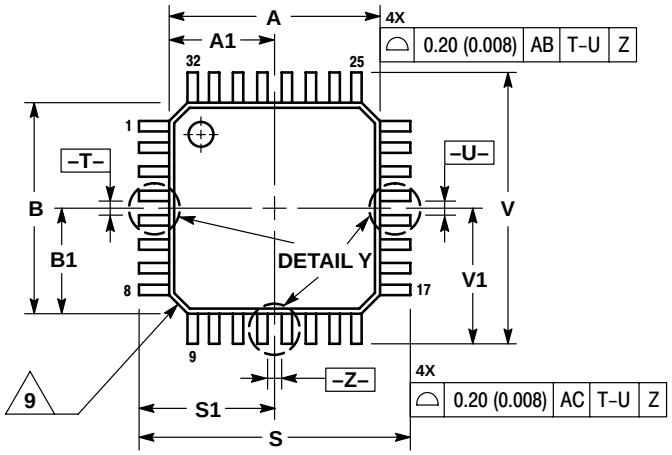
AND8009 – ECLinPS Plus Spice I/O Model Kit

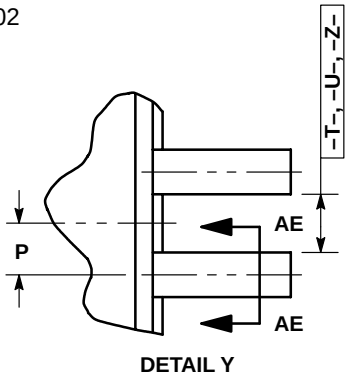
AND8020 – Termination of ECL Logic Devices

For an updated list of Application Notes, please see our website at http://onsemi.com.

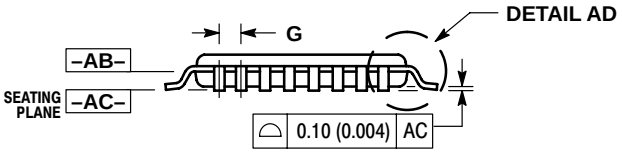
PACKAGE DIMENSIONS

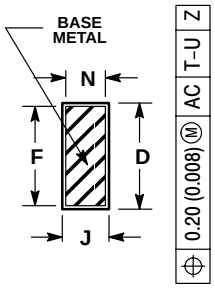
LQFP
FA SUFFIX
32–LEAD PLASTIC PACKAGE
CASE 873A–02
ISSUE A



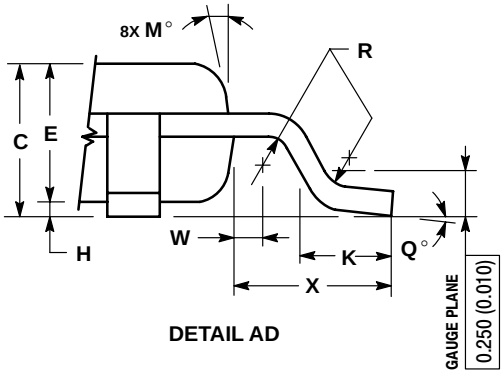


DETAIL Y





SECTION AE–AE



DETAIL AD

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE –AB– IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS –T–, –U–, AND –Z– TO BE DETERMINED AT DATUM PLANE –AB–.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE –AC–.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.250 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE –AB–.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE D DIMENSION TO EXCEED 0.520 (0.020).
8. MINIMUM SOLDER PLATE THICKNESS SHALL BE 0.0076 (0.0003).
9. EXACT SHAPE OF EACH CORNER MAY VARY FROM DEPICTION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	7.000 BSC		0.276 BSC	
A1	3.500 BSC		0.138 BSC	
B	7.000 BSC		0.276 BSC	
B1	3.500 BSC		0.138 BSC	
C	1.400	1.600	0.055	0.063
D	0.300	0.450	0.012	0.018
E	1.350	1.450	0.053	0.057
F	0.300	0.400	0.012	0.016
G	0.800 BSC		0.031 BSC	
H	0.050	0.150	0.002	0.006
J	0.090	0.200	0.004	0.008
K	0.500	0.700	0.020	0.028
M	12° REF		12° REF	
N	0.090	0.160	0.004	0.006
P	0.400 BSC		0.016 BSC	
Q	1°	5°	1°	5°
R	0.150	0.250	0.006	0.010
S	9.000 BSC		0.354 BSC	
S1	4.500 BSC		0.177 BSC	
V	9.000 BSC		0.354 BSC	
V1	4.500 BSC		0.177 BSC	
W	0.200 REF		0.008 REF	
X	1.000 REF		0.039 REF	

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