

# MC100EPT622

## 3.3V LVTTTL/LVCMOS to LVPECL Translator

The MC100EPT622 is a 10-Bit LVTTTL/LVCMOS to LVPECL translator. Because LVPECL (Positive ECL) levels are used only +3.3 V and ground are required. The device has an OR-ed enable input which can accept either LVPECL (ENPECL) or TTL/LVCMOS inputs (ENTTL). If the inputs are left open, they will default to the enable state. The device design has been optimized for low channel-to-channel skew

### Features

- 450 ps Typical Propagation Delay
- Maximum Frequency > 1.5 GHz Typical
- PECL Mode
- Operating Range:  $V_{CC} = 3.0\text{ V}$  to  $3.8\text{ V}$  with  $V_{EE} = 0\text{ V}$
- PNP LVTTTL Inputs for Minimal Loading
- Q Output Will Default HIGH with Inputs Open
- The 100 Series Contains Temperature Compensation.
- Pb-Free Packages are Available\*



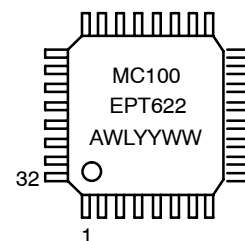
ON Semiconductor®

<http://onsemi.com>

### MARKING DIAGRAM\*



LQFP-32  
FA SUFFIX  
CASE 873A



A = Assembly Location  
WL = Wafer Lot  
YY = Year  
WW = Work Week

\*For additional marking information, refer to Application Note AND8002/D.

Table 1. TRUTH TABLE

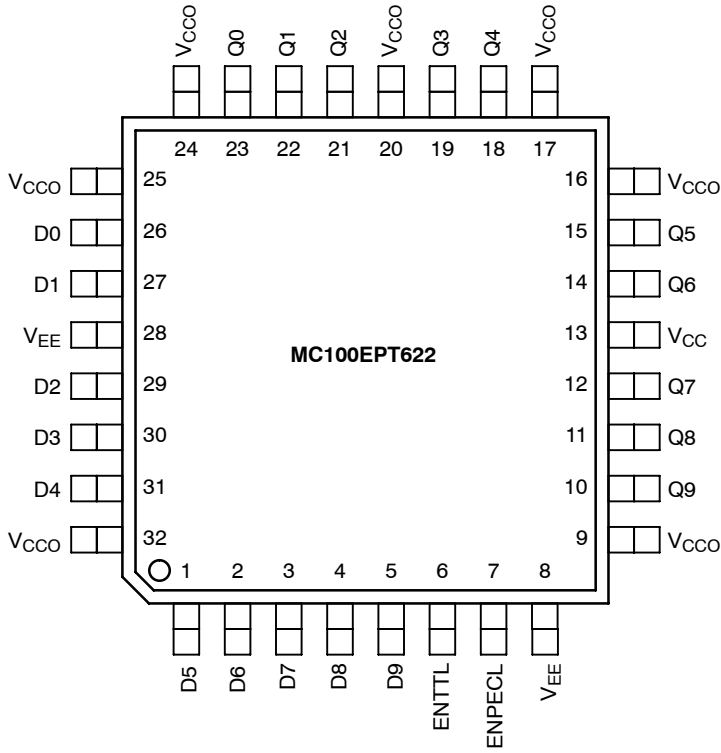
ENPECL	ENTTL	D	Q
H	X	H	H
H	X	L	L
X	H	H	H
X	H	L	L
L	L	X	L

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 6 of this data sheet.

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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Warning: All  $V_{CC}$ ,  $V_{CC0}$ , and  $V_{EE}$  pins must be externally connected to Power Supply to guarantee proper operation.

Figure 1. 32-Lead LQFP Pinout (Top View)

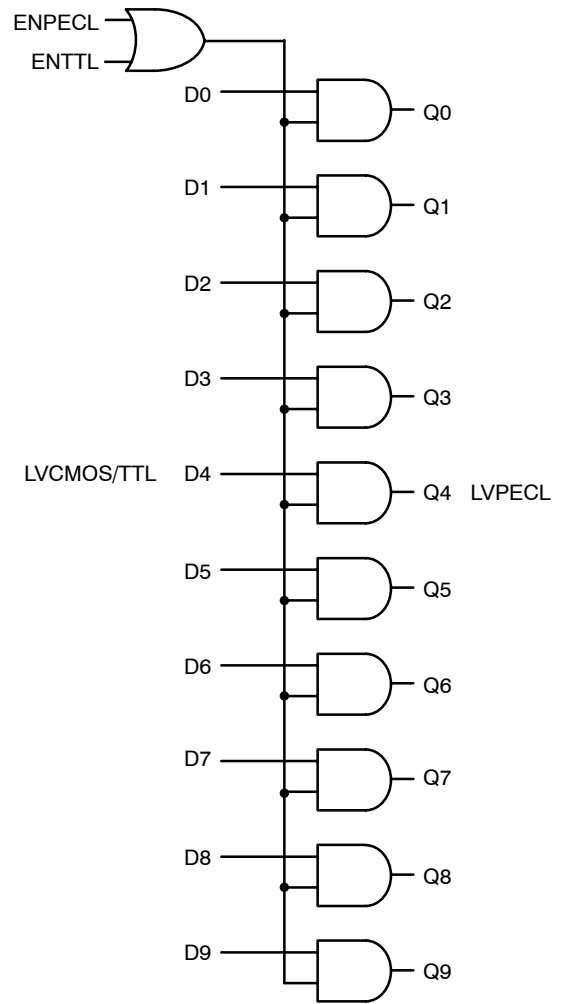


Figure 2. Logic Symbol

Table 1. PIN DESCRIPTION

Pin	Function
D0:9	Data Input (TTL)
Q0:9	Data Outputs (PECL)
ENTTL	Enable Control (TTL)
ENPECL	Enable Control (PECL)
$V_{CC}$ , $V_{CC0}$	Positive Supply
$V_{EE}$	Ground

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**Table 2. ATTRIBUTES**

Characteristics		Value
Internal Input Pulldown Resistor		N/A
Internal Input Pullup Resistor		N/A
ESD Protection	Human Body Model	> 2 kV
	Machine Model	> 150 V
	Charged Device Model	> 2 kV
Moisture Sensitivity, Indefinite Time Out of Drypack		Level 2
Flammability Rating	Oxygen Index: 28 to 34	UL 94 V-0 @ 0.125 in
Transistor Count		596 Devices
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test		

**Table 3. MAXIMUM RATINGS**

Symbol	Parameter	Condition 1	Condition 2	Rating	Unit
V <sub>CC</sub>	Power Supply	V <sub>EE</sub> = 0 V		5	V
V <sub>I</sub>	Input Voltage	V <sub>EE</sub> = 0 V	V <sub>I</sub> ≤ V <sub>CC</sub>	5 to 0	V
I <sub>out</sub>	Output Current	Continuous Surge		50 100	mA mA
T <sub>A</sub>	Operating Temperature Range			-40 to +85	°C
T <sub>stg</sub>	Storage Temperature Range			-65 to +150	°C
θ <sub>JA</sub>	Thermal Resistance (Junction-to-Ambient)	0 lfpm 500 lfpm	32 LQFP 32 LQFP	80 55	°C/W °C/W
θ <sub>JC</sub>	Thermal Resistance (Junction-to-Case)	Standard Board	32 LQFP	12 to 17	°C/W
T <sub>sol</sub>	Wave Solder	<2 to 3 sec @ 248°C		265	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

**Table 4. TTL INPUT DC CHARACTERISTICS** V<sub>CC</sub> = 3.3 V, GND = 0.0 V, T<sub>A</sub> = -40°C to 85°C

Symbol	Characteristic	Condition	Min	Typ	Max	Unit
I <sub>IH</sub>	Input HIGH Current	V <sub>IN</sub> = 2.7 V			25	μA
I <sub>IHH</sub>	Input HIGH Current MAX	V <sub>IN</sub> = V <sub>CC</sub>			100	μA
I <sub>IL</sub>	Input LOW Current	V <sub>IN</sub> = 0.5 V			-0.6	mA
V <sub>IK</sub>	Input Clamp Voltage	I <sub>IN</sub> = -18 mA	-1.2	-0.9		V
V <sub>IH</sub>	Input HIGH Voltage		2.0			V
V <sub>IL</sub>	Input LOW Voltage				0.8	V

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

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**Table 5. PECL INPUT DC CHARACTERISTICS**  $V_{CC} = 3.3\text{ V}$ ,  $GND = 0.0\text{ V}$ ,  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$

Symbol	Characteristic	Condition	Min	Typ	Max	Unit
$I_{IH}$	Input HIGH Current	$V_{IN} = 2420\text{ mV}$			150	$\mu\text{A}$
$I_{IL}$	Input LOW Current	$V_{IN} = 1490\text{ mV}$			200	$\mu\text{A}$
$V_{IH}$	Input HIGH Voltage		2075		2420	mV
$V_{IL}$	Input LOW Voltage		1490		1675	mV

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

**Table 6. PECL OUTPUT DC CHARACTERISTICS**  $V_{CC} = 3.3\text{ V}$ ,  $GND = 0.0\text{ V}$  (Note 1)

Symbol	Characteristic	$-40^\circ\text{C}$			$25^\circ\text{C}$			$85^\circ\text{C}$			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$I_{EE}$	Power Supply Current	85	115	145	90	120	155	95	130	155	mA
$V_{OH}$	Input High Voltage (Note 2)	2155	2280	2405	2155	2280	2405	2155	2280	2405	mV
$V_{OL}$	Input Low Current (Note 2)	1355	1520	1700	1355	1520	1700	1355	1520	1700	mV

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

1. Input and output parameters vary 1:1 with  $V_{CC}$ .
2. All loading with  $50\ \Omega$  to  $V_{CC} - 2.0\text{ V}$ .

**Table 7. AC CHARACTERISTICS**  $V_{CC} = 3.0\text{ V}$  to  $3.8\text{ V}$  (Note 3)

Symbol	Characteristic	$-40^\circ\text{C}$			$25^\circ\text{C}$			$85^\circ\text{C}$			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$f_{max}$	Maximum Frequency (See Figure 3)	1.0	1.5		1.0	1.5		1.0	1.5		GHz
$t_{PLH}$ , $t_{PHL}$	Propagation Delay to Output (Figure 4, Note 4) D to Q ENPECL to Q ENTTL to Q	100 150 300	450 500 450	800 875 800	100 150 300	500 500 500	875 875 800	100 200 300	500 550 500	800 925 800	ps
$t_{JITTER}$	Random Clock Jitter (RMS) (See Figure 3)		0.7	3.0		0.7	3.0		0.7	3.0	ps
$t_r / t_f$	Output Rise/Fall Times (20% – 80%)	100	200	450	100	200	250	100	200	300	ps
$T_{SKEW}$	Duty Cycle Skew (Note 5) D to Q Channel 0–7 Channel 8–9 ENPECL to Q ENTTL to Q		120 200 120 100	375 775 400 275		120 200 120 100	375 775 400 275		120 200 120 100	375 775 400 275	ps

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

3. Measured using a 2.4 V source, 50% duty cycle clock source. All loading with  $50\ \Omega$  to  $V_{CC} - 2.0\text{ V}$ .
4. 1.5 V to 50% point of the output.
5. Duty cycle skew  $|t_{PLH} - t_{PHL}|$  on the specific path.

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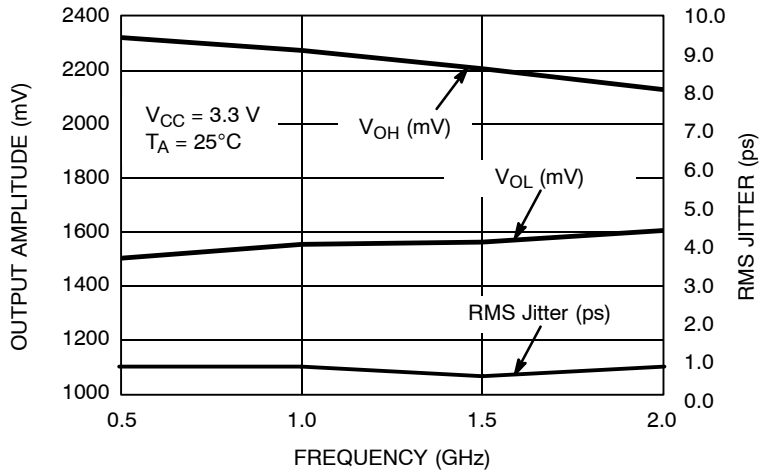


Figure 3. Average Output Amplitude/Jitter (3.3 V, 25°C)

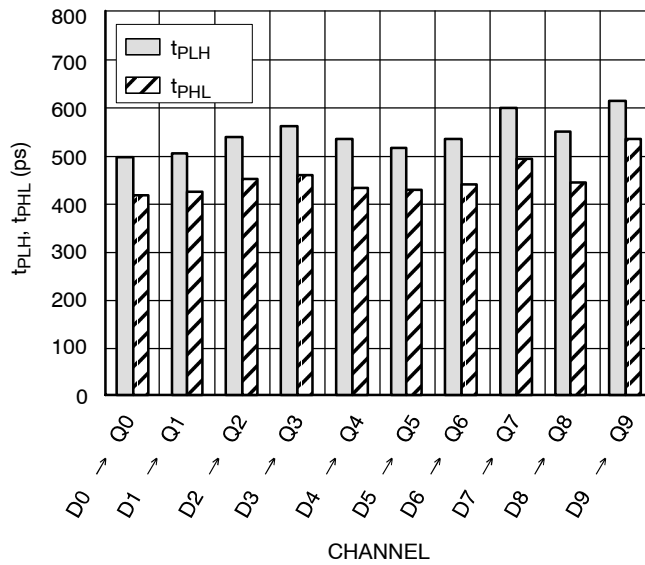


Figure 4. Average Propagation Delay (3.3 V, 25°C)

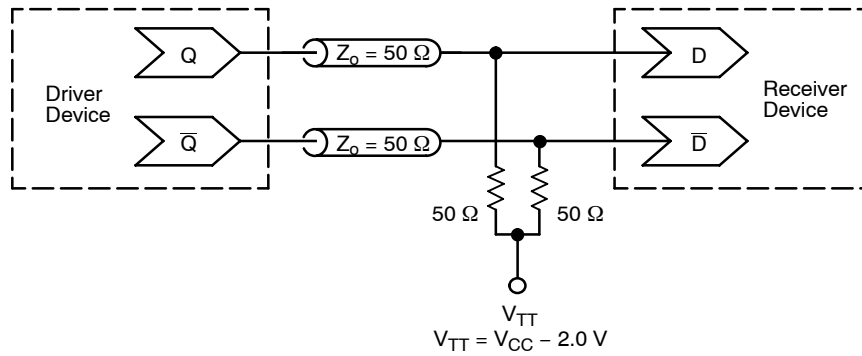


Figure 5. Typical Termination for Output Driver and Device Evaluation (See Application Note AND8020/D – Termination of ECL Logic Devices.)

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## ORDERING INFORMATION

Device	Package	Shipping†
MC100EPT622FA	LQFP-32	250 Units / Tray
MC100EPT622FAG	LQFP-32 (Pb-Free)	250 Units / Tray
MC100EPT622FAR2	LQFP-32	2000 / Tape & Reel
MC100EPT622FAR2G	LQFP-32 (Pb-Free)	2000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

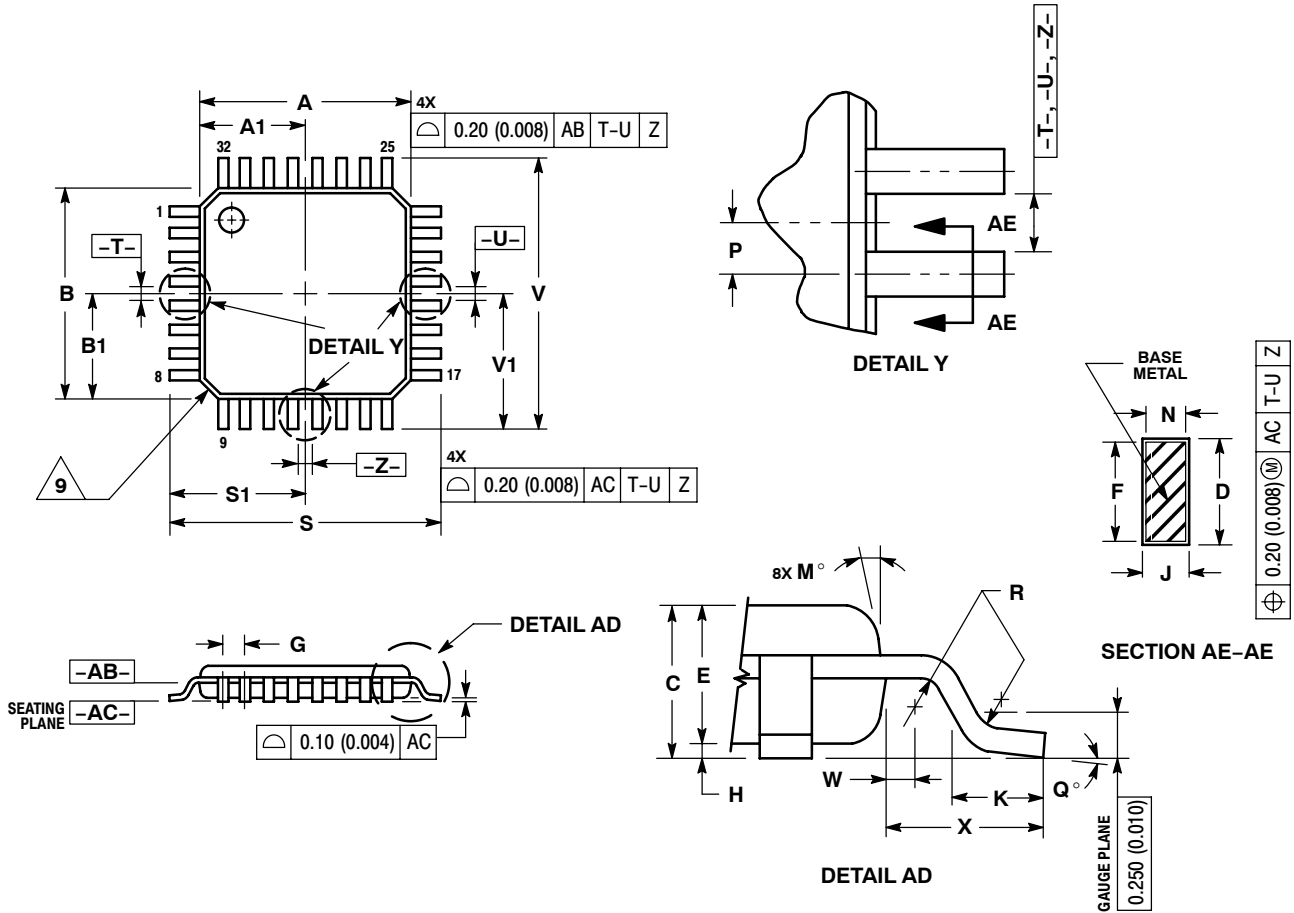
### Resource Reference of Application Notes

- AN1405/D** - ECL Clock Distribution Techniques
- AN1406/D** - Designing with PECL (ECL at +5.0 V)
- AN1503/D** - ECLinPS™ I/O SPICE Modeling Kit
- AN1504/D** - Metastability and the ECLinPS Family
- AN1568/D** - Interfacing Between LVDS and ECL
- AN1672/D** - The ECL Translator Guide
- AND8001/D** - Odd Number Counters Design
- AND8002/D** - Marking and Date Codes
- AND8020/D** - Termination of ECL Logic Devices
- AND8066/D** - Interfacing with ECLinPS
- AND8090/D** - AC Characteristics of ECL Devices


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## PACKAGE DIMENSIONS

32 LEAD LQFP  
CASE 873A-02  
ISSUE C



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