MT91600

Programmable SLIC

Data Sheet

February 2005

Features

- Transformerless 2 W to 4 W conversion
- Controls battery feed to line
- Programmable line impedance
- Programmable network balance impedance
- Off-hook and dial pulse detection
- Ring ground over-current protection
- Programmable gain
- Programmable constant current feed
- -22 V to -72 V battery operation

Applications

Line interface for:

- PABX/ONS
- Intercoms
- Key Telephone Systems
- Control Systems

Ordering Information

MT91600AN	28 Pin SSOP	Tubes
MT91600ANR	28 Pin SSOP	Tape & Reel
MT91600AN1	28 Pin SSOP*	Tubes
MT91600ANR1	28 Pin SSOP*	Tape & Reel

*Pb Free Matte Tin

-40°C to +85°C

Description

The Zarlink MT91600 provides an interface between a switching system and a subscriber loop, mainly for short loop SLIC applications. The functions provided by the MT91600 include battery feed, programmable constant current, 2 W to 4 W conversion, off-hook and dial pulse detection, user definable line and network balance impedance's and the capability of programming the audio gain externally. The device is fabricated as a CMOS circuit in a 28 pin SSOP package.

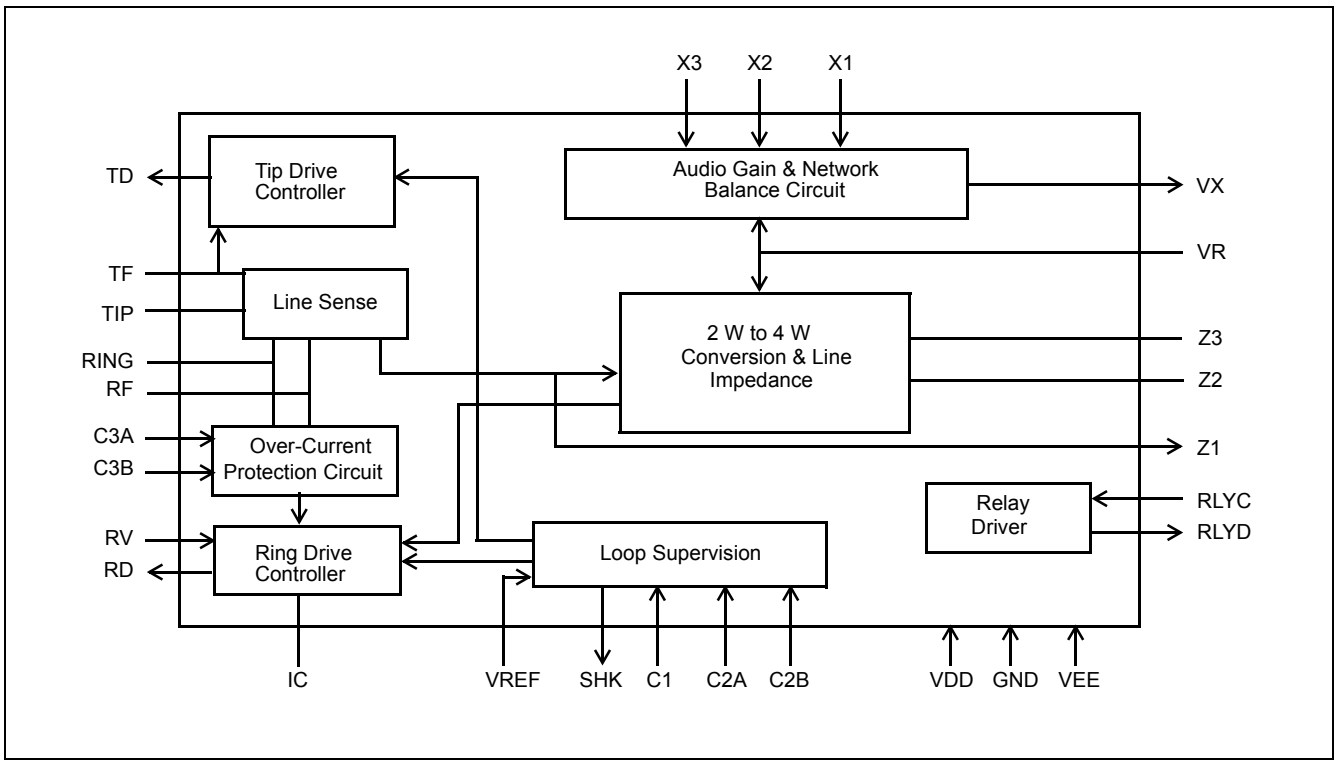


Figure 1 - Functional Block Diagram

Change Summary

Page	Item	Change
10	Figure 5	Updated Application Diagram

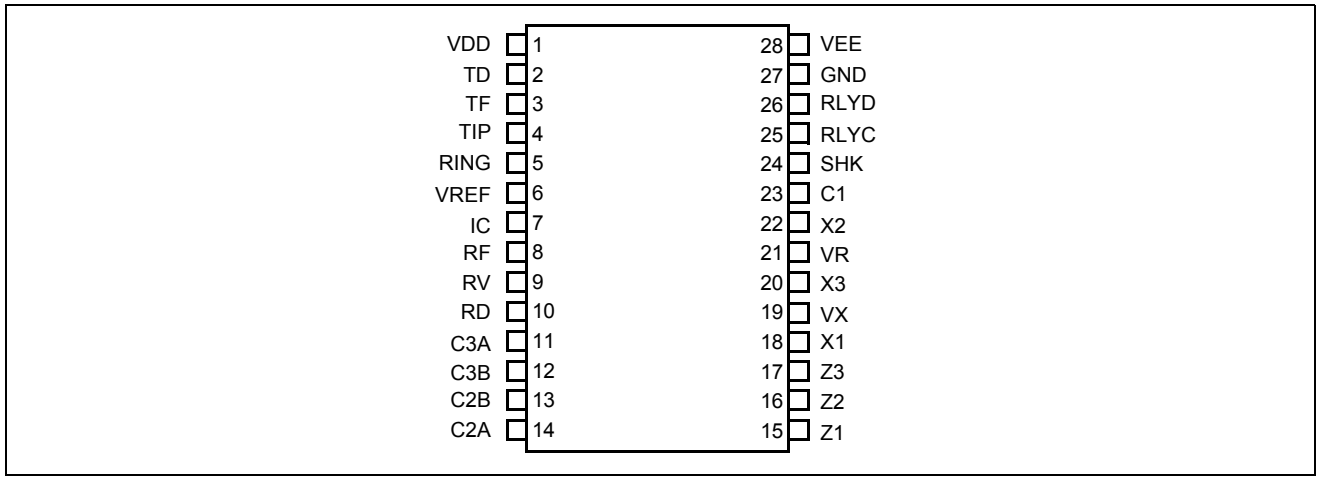


Figure 2 - Pin Connections

Pin Description

Pin #	Name	Description
1	VDD	Positive supply rail, +5 V.
2	TD	**Tip Drive (Output).** Controls the Tip transistor.
3	TF	**Tip Feed.** Connects to the Tip transistor and to the TIP lead via the Tip feed resistor.
4	TIP	**Tip.** Connects to the TIP lead of the telephone line.
5	RING	**Ring.** Connects to the RING lead of the telephone line.
6	VREF	**Reference Voltage (Input).** This pin is used to set the subscribers loop constant current. Changing the input voltage sets the current to any desired value within the working limits. VREF is related to VLC.
7	IC	**Internal Connection (Input).** This pin must be connected to GND for normal operation.
8	RF	**Ring Feed.** Connects to the RING lead via the Ring feed resistor.
9	RV	**Ring Voltage and Audio Feed.** Connects directly to the Ring drive transistor and also to Ring Feed via a relay.
10	RD	**Ring Drive (Output).** Controls the Ring transistor.
11	C3A	A filter capacitor for over-current protection is connected between this pin and GND.
12	C3B	A filter capacitor for over-current protection is connected between this pin and GND.
13	C2B	A capacitor for loop current stability is connected between this pin and C2A.
14	C2A	A capacitor for loop current stability is connected between this pin and C2B.
15	Z1	**Line Impedance Node 1**. A resistor of scaled value "k" is connected between Z1 and Z2. This connection can not be left open circuit.

Pin Description (continued)

Pin #	Name	Description
16	Z2	**Line Impedance Node 2**. This is the common connection node between Z1 and Z3.
17	Z3	**Line Impedance Node 3**. A network either resistive or complex of scaled value "k" is connected between Z3 and Z2. This connection can not be left open circuit.
18	X1	**Gain Node 1**. This is the common node between Z3 and VX where resistors are connected to set the 2 W to 4 W gain.
19	VX	**Transmit Audio (Output)**. This is the 4 W analog signal to the SLIC.
20	X3	**Gain Node 3**. This is the common node between VR and the audio input from the CODEC or switching network where resistors are fitted to sets the 4 W to 2 W gain
21	VR	**Receive Audio (Input)**. This is the 4 W analog signal to the SLIC.
22	X2	**Gain Node 2.** Networks, either resistive or complex, are connected between this node, VR and GND to set the Network Balance Impedance for the SLIC.
23	C1	A filter capacitor for ring trip is connected between this pin and GND.
24	SHK	**Switch Hook (Output).** This pin indicates the line state of the subscribers telephone. The output can also be used for dial pulse monitoring. SHK is high in off-hook state.
25	RLYC	**Relay Control (Input).** An active high on this pin will switch RLYD low.
26	RLYD	**Inverted Output of RLYC.** It is used to drive the bipolar transistor that drives the relay (see Figure 5.)
27	GND	**Ground. Return path for +5 V and -5 V.** This should also be connected back to the return path for the loop battery, LGND and relay drive ground RLYGND.
28	VEE	Negative supply rail, -5 V.

Functional Description

The MT91600 is the analog SLIC for use in a 4 Wire switched system. The SLIC performs all of the normal interface functions between the CODEC or switching system and the analog telephone line such as 2 W to 4 W conversion, constant current feed, ringing and ring trip detection, current limiting, switch hook indication and line and network balance impedance setting using minimal external components.

Refer to Figure 5 for MT91600 components designation.

2 Wire to 4 Wire Conversion

The hybrid performs 2 wire to 4 wire conversion by taking the 4 wire signal from an analog switch or voice CODEC, a.c. coupled to VRIN, and converting it to a 2 wire differential signal at tip and ring. The 2 wire signal applied to tip and ring by the telephone is converted to a 4 wire signal and should be a.c. coupled to Vx which is the output from the SLIC to the analog switch or voice CODEC input.

Gain Control

It is possible to set the Transmit and Receive gains by the selection of the appropriate external components.

The gains can be calculated by the formulae:

2W to 4W gain:
Gain 2 - 4 = 20*Log [R13 / R12]
4W to 2W gain:
Gain 4 - 2 = 20*Log [0.891 * (R14 / R15)]

Impedance Programming

The MT91600 allows the designer to set the device's impedance across TIP and RING, (Z_{TR}), and network balance impedance, (Z_{NB}), separately with external low cost components.

For a resistive load, the impedance (Z_{TR}) is set by R11 and R18. For a complex load, the impedance (Z_{TR}) is set by R11, R18, R19 & C8 (see Figure 5.)

The network balance, (Z_{NB}), is set by R16, R17 & C3 (see Figure 5.)

The network balance impedance should be calculated once the 2W - 4W gain has been set.

Line Impedance

For optimum performance, the characteristic impedance of the line, (Z_o), and the device's impedance across TIP and RING, (Z_{TR}), should match. Therefore:

$Z_o = Z_{TR}$

The relationship between Z_o and the components that set Z_{TR} is given by the formula:

$Z_o / (R1+R2) = kZ_o / R11$
where $kZ_o = Z_{LZ}$

Z_{LZ} = R18, for a resistive load.
Z_{LZ} = [R18 + (R19 // C8)], for a complex load.

The value of k can be set by the designer to be any value between 20 and 250. Three rules to ensure the correct operation of the circuit:

(A) R18 + R19 > 50kΩ
(B) R1 = R2.
(C) R11 > =50kΩ

It is advisable to place these components as close as possible to the SLIC.

Network Balance Impedance

The network balance impedance, (Z_{NB}), will set the transhybrid loss performance for the circuit. The balance of the circuit is independent of the 4 - 2 Wire gain but is a function of the 2 - 4 Wire gain.

The method of setting the values for R16 and R17 is given by the formula:

$$\frac{R17}{R17 + R16} = \frac{[1.782 * Z_o / (Z_o+Z_{NB}) * (R13 / R12)]}{[1 + R13 / R12]}$$

where Z_{NB} is the network balance impedance of the SLIC and Z_o is the line impedance.

(R16 + R17) >= 50kΩ

It is advisable to place these components as close as possible to the SLIC.

Loop Supervision & Dial Pulse Detection

The Loop Supervision circuit monitors the state of the phone line and when the phone goes "Off Hook" the SHK pin goes high to indicate this state. This pin reverts to a low state when the phone goes back "On Hook" or if the loop resistance is too high for the circuit to continue to support a constant current.

The SHK output can also be monitored for dialing information when used in a dial pulse system.

Constant Current Control

The SLIC employs a feedback circuit to supply a constant feed current to the line. This is done by sensing the sum of the voltages across the feed resistors, R1 and R2, and comparing it to the input reference voltage, Vref, that determines the constant current feed current.

The MT91600's programmable current range is between 18 mA to 32 mA.

Line Drivers & Overcurrent Protection

The Line Drivers control the external Battery Feed circuit which provide power to the line and allows bi-directional audio transmission.

The loop supervision circuitry provides bias to the line drivers to feed a constant current while the over-current protection circuitry prevents the ring driver from causing the ring transistor to overload.

The line impedance presented by the Line Driver circuitry is determined by the external network, which may be purely resistive or complex, allowing the circuit to be configured for use in any application. The impedance can also be fixed to one value and modified to look like a different value by reflecting an impedance through the SLIC from an intelligent CODEC or DSP module.

There is long term protection on the RING output against accidental short circuits that may be applied either across TIP/RING to GND or RING to GND. This high current will be sensed and limited to a value that will protect the circuit.

In situations where an accidental short circuit occurs either across TIP/RING to GND or RING to GND, an excessive amount of current will flow through the ring drive transistor, Q3. Although the MT91600 will sense this high current and limit it, if the power rating of Q3 is not high enough, it may suffer permanent damage. In this case, a power sharing resistor, R23, can be inserted (see Figure 5) to dissipate some of the power. Capacitor C13 is inserted to provide an a.c. ground point. The criteria for selecting a value for the power sharing resistor R23 can be found in the application section of this data sheet.

Ringing and Ring Trip Detection

Ringing is applied to the line by disconnecting pin 8, RF, from pin 9, RV, and connecting it to a ringing source which is battery backed. This may be done by use of an electro-mechanical relay. The SLIC is capable of detecting an Off Hook condition during ringing by filtering out the large A.C. component by use of the external components connected to pin 23. This filter allows an Off Hook condition to be monitored at SHK, pin 24.

When using DTMF signalling only i.e., pulse dialling is not used, the capacitor, C7, can be permanently connected to ground and does not require to be switched out during dialling.

Power up Sequence

The circuit should be powered up in the following order: AGND, VEE, VDD, $V_{BAT.}$

Application

The following Application section is intended to demonstrate to the user the methods used in calculating and selecting the external programming components in implementing the MT91600 as an analog line interface in a communication system. The programming component values calculated below results in the optimum performance of the device.

Refer to Figure 5 for MT91600 components designation.

Component Selection

Feed Resistors (R1, R2)

The selection of feed resistors, R1 and R2, can significantly affect the performance of the MT91600. It is recommended that their values fall in the range of:

$$200\Omega <= R1 <= 250\Omega$$

where, R1 = R2

The resistors should have a tolerance of 1% (0.15% matched) and a power rating of 1 Watt.

Loop Current Setting (R3, R4, C9)

By using a resistive divider network, (Figure 3), it is possible to maintain the required voltage at Vref to set I_{LOOP}. The loop current programming is based on the following relationship:

$$I_{LOOP} = - \frac{[F * V_{LC} + G * V_{BAT}] * K_o * H}{(R1 + R2)}$$

where, F = R4 / (R4 + R3)
G = R3 / (R4 +R3)
K_o = 200000 / (200000 + (R4//R3))
H = 1.07
I_{LOOP} is in Ampere

From Figure 3 with R1 = R2 = 220Ω

For I_{LOOP} = 25mA, V_{LC} = 0V, Vbat=-48V

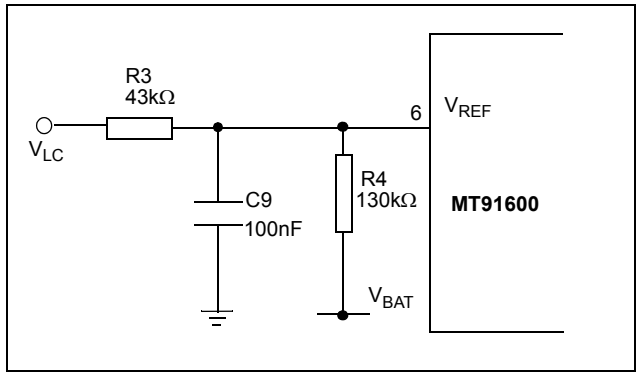


Figure 3 - Resistor Divider

C9 is inserted to ensure pin 6, Vref, remains at a.c. ground. 100 nF is recommended.

I_{LOOP} can also be set by directly driving Vref with a low impedance voltage source. (See Figure 4). It is recommended that a small resistor be placed in series with the Vref pin. In this case:

$$I_{LOOP} = \frac{1.07 * Vs}{(R1 + R2)} \qquad \text{where, } Vs < 0$$

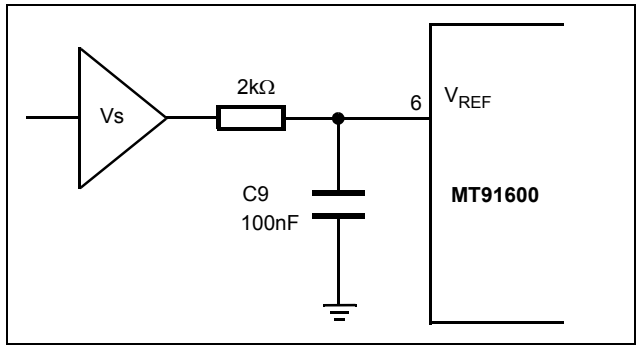


Figure 4 - Direct Voltage

Calculating Component Values For AC Transmission

There are five parameters a designer should know before starting the component calculations. These five parameters are:

1) characteristic impedance of the line Z_o
2) network balance impedance Z_{NB}
3) value of the feed resistors (R1 and R2)
4) 2 W to 4 W transmit gain
5) 4 W to 2 W receive gain

The following example will outline a step by step procedure for calculating component values. Given:

$Z_o = 600\Omega$, $Z_{NB} = 600\Omega$, R1=R2= 220Ω
Gain 2 - 4 = -1dB, Gain 4 - 2 = -1dB

Step 1: Gain Setting (R12, R13, R14, R15)

Gain 2 - 4 = 20 Log [R13 / R12]
-1 dB = 20 Log [R13 / R12]
$\therefore$ R12 = 112.2kΩ, R13 = 100kΩ.

Gain 4 - 2 = 20 Log [0.891 * [R14 / R15)]
-1 dB = 20 Log [0.891 * [R14 / R15)]
$\therefore$ R14 = 100kΩ, R15 = 100kΩ.

Step 2: Impedance Matching (R11, R18, R19, C8)

a) Z_o / (R1+R2) = kZ_o / R11
600/(220+220) = (k*600)/R11
let k = 125
∴ R11 = 55kΩ.

b) In general,

$kZ_o = Z_{LZ}$
where:
Z_{LZ} = R18, for a resistive load.
Z_{LZ} = [R18 + (R19 // C8)], for a complex load.

Since we are dealing with a resistive load in this example Z_{LZ} = R18, and therefore:

kZ_o = R18
(125 * 600)= R18
∴ R18 = 75kΩ.

Step 3: Network Balance Impedance (R16, R17)

$$\frac{R17}{R17 + R16} = \frac{[1.782 * Z_o / (Z_o+Z_{NB}) * (R13 / R12)]}{[1 + R13 / R12)]}$$

$$\frac{R17}{R17 + R16} = 0.4199$$

set R17 = 100kΩ, R16 becomes 138kΩ.
∴ R16 = 138kΩ, R17 = 100kΩ.

Complex Line Impedance, Z_o

In situations where the characteristic impedance of the line Z_o is a complex value, determining the component values for impedance matching (R11, R18, R19, C8) is as follows:

Given Z_o = 220Ω + (820Ω // 120nF)

Z_o / (R1+R2) = kZ_o / R11 (Equation 1)

where, kZ_o = [R18 + (R19 // C8)]

Choose a standard value for C8 to find a suitable value for k.

Since 1nF exists, let C8 = 1nF then,
k = 120nF / C8
k = 120nF / 1nF
∴ k =120
R18 = k * 220Ω
R18 = 120 * 220Ω
R18 = 26400
R19 = k * 820Ω
R19 = 120 * 820
R19 = 98400
∴ R18 = 26k4Ω, R19 = 98k4Ω

From (Equation 1)
R11 = k * (R1 + R2)
R11 = 120 * (220Ω + 220Ω)
∴ R11 = 52k8Ω

Power Sharing Resistor (R23)

To determine the value of R23, use the following equations:

$$R23(max) = \frac{|Vbat(min)|}{30mA} - 100 - (2*R2 + Lr + DCRP)$$

$$R23(min) = \frac{|Vbat(max)|}{40mA} - \frac{Pd(max)}{1.6mA} - R2$$

where,
Vbat(min/max) = the expected variation of Vbat.
R2 = the feed resistor.
Lr = maximum DC loop resistance.
DCRP = DC resistance of the phone set.
Pd(max) = the maximum power dissipation of the ring drive transistor Q3.

If R23(max) > R23(min), then set R23 to be the geometric center:
R23 = Square Root (R23(max) * R23(min))

If R23(max) < R23(min), then a violation has occurred. Pd(max) will have to be increased.
If R23 = negative value, power sharing is not required, i.e., R23=0

A numerical example:

Given:
R2 = 220Ω
Lr = 325Ω (2.5km of 28 gauge wire, averaged at 65Ω/km)
DCRP = 200Ω
Pd(max) = 1.5W
Vbat = -48V +/- 10% (i.e. -43V to -53V)

Therefore:

R23(max) = (43/30mA) - 100 - (2 * 220 + 325 + 200)
= 1433.3 - 100 - 965
R23(max) = 368.3Ω

R23(min) = (53/40mA) - (1.5/1.6mA) - 220
= 1325 - 937.5 - 220
R23(min) = 167.5 Ω

R23 = Square Root (368.3 * 167.5)
R23 = 248.4Ω

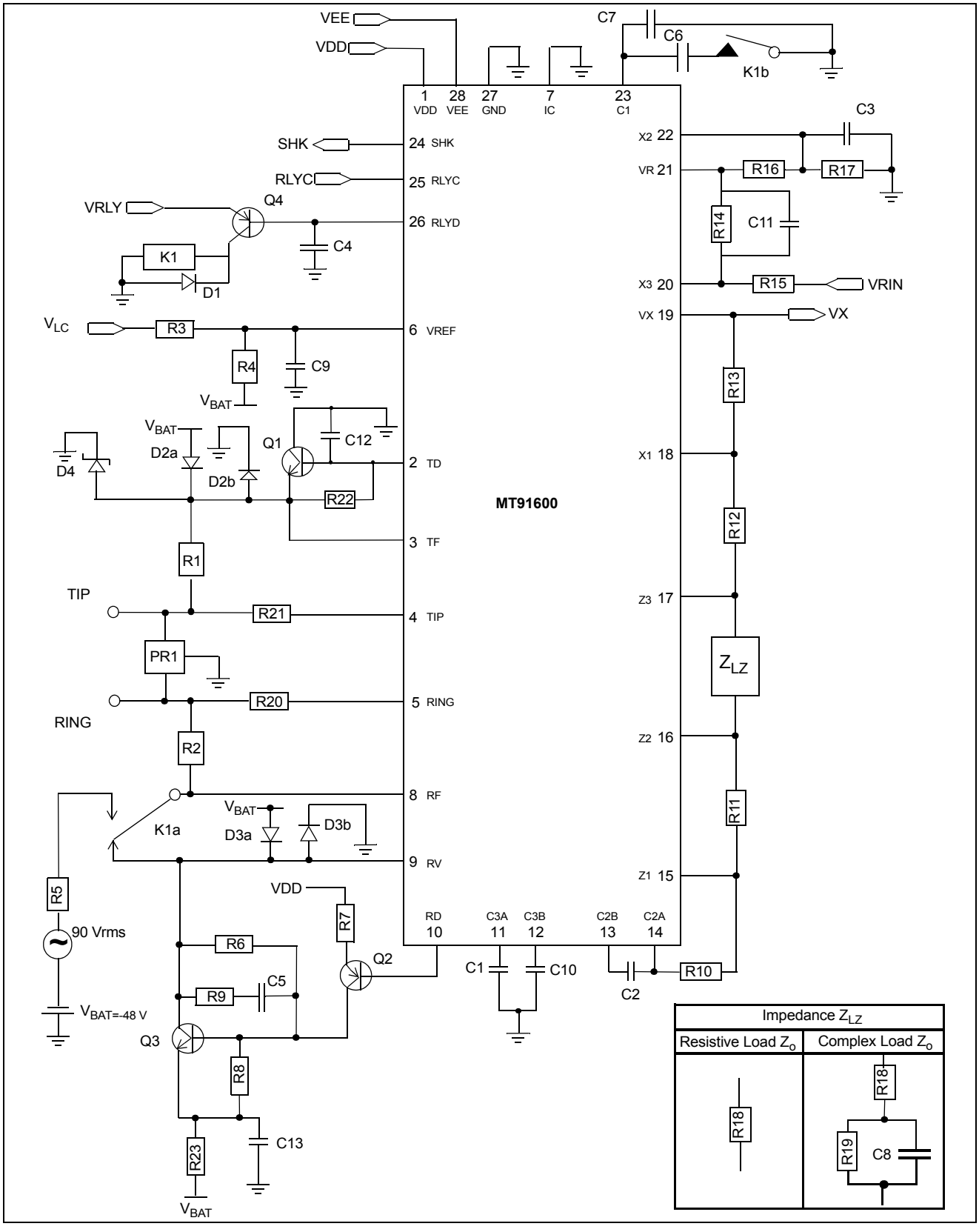


Figure 5 - Typical Application

Component List* for a Typical Application with a Resistive 600 Ω Line Impendance - Refer to Figure 5 for component designation and recommended configuration

Resistor Values			
R1	220 Ω 1% (0.15% matched), 1 W	R2	220 Ω 1% (0.15% matched), 1 W
R3	43 kΩ	R4	130 kΩ
R5	220 Ω	R6	75 kΩ
R7	3 kΩ	R8	1 kΩ
R9	1 kΩ	R10	560 kΩ
R11	55 kΩ	R12	112 kΩ
R13	100 kΩ	R14	100 kΩ
R15	100 kΩ	R16	138 kΩ
R17	100 kΩ	R18	75 kΩ
R19	0 Ω	R20	2 kΩ
R21	2 kΩ	R22	1 kΩ
R23	248 Ω		
Capacitor Values			
C1	100 nF, 5%	C2	300 nF, 5%
C3	100 pF, 5%	C4	33 nF, 20%
C5	3.3 nF, 5%	C6	1 uF, 20%, 16 V
C7	100 nF, 20%	C8	0 F
C9	100 nF, 20%	C10	100 nF, 5%
C11	47 pF, 20%	C12	33 nF, 10%
C13	100 nF 20%		
Diodes and Transistors			
D1	BAS16 or equivalent	D2a/b	BAV99 dual diode or equivalent
D3a/b	BAV99 dual diode or equivalent	Q1	2N2222 or MPSA42 or MMBTA42
Q2	2N2907 or MPSA92 or MMBTA92	Q3	2N2222 or MPSA42 or MMBTA42
Q4	2N2907 or MPSA92 or MMBTA92	D4	1N5242 12 V Zener or equivalent

Note: All resistors are 1/4 W, 1% unless otherwise indicated.
*Assumes $Z_o = Z_{NB} = 600\ \Omega$, Gain 2 - 4 = -1 dB, Gain 4 - 2 = -1 dB.
Decoupling capacitors, (1 uF, 100 V, 20%), can be added to V_{DD}, V_{EE}, V_{BAT} and V_{RLY} to provide improved PSRR performance.

K1 = Electro-mechanical relay, 5V, DPDT/2 FORM C

PR1 = This device must always be fitted to ensure damage does not occur from inductive loads.For simple applications, PR1 can be replaced by a single TVS, such as 1.5KE220C, across tip and ring. For applications requiring lightning and mains cross protection further circuitry will be required and the following protection devices are suggested: P2353AA, P2353AB (Teccor), THBT20011, THBT20012, THBT200S (SGS-Thomson), TISP2290, TSSP8290L (T.I.)

Absolute Maximum Ratings*

	Parameter	Sym.	Min.	Max.	Units	Comments
1	DC Supply Voltages	V_{DD} V_{EE} V_{BAT}	-0.3 -6.5 -80	+6.5 +0.3 +0.3	V V V	Limited by the Drive transistor, Q3.
2	Ringing Voltages	Vring		100	Vrms	Superimposed on V_{BAT}
3	Voltage setting for Loop Current	V_{REF}	-20	+0.3	V	Note 1
4	Overvoltage Tip/GND Ring/GND, Tip/Ring			200	V	MAX 1 ms (with power on)
5	Ringing Current	Iring		30	mA. RMS	
6	Ring Ground over-current			45	mA	Note 2
7	Storage Temp	Tstg	-65	+150	°C	
8	Package Power Dissipation	Pdiss		0.10	W	+85°C max, V_{BAT} = -48 V
9	ESD Rating			500	V	Human Body Model Note 3

*Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.
Note 1: Voltage at Vref pin set by VLC and potential divider.
Note 2: Tip and Ring must not be shorted together and to ground at the same time.
Note 3: The device contains circuitry to protect the inputs from static voltage up to 500 V. However, precautions should be taken to avoid static charge build up when handling the device.

Recommended Operating Conditions

	Parameter	Sym.	Min.	Typ.‡	Max.	Units	Test Conditions
1	Operating Supply Voltages	V_{DD} V_{EE} V_{BAT}	4.75 -5.25 -72	5.00 -5.00 -48	5.25 -4.75 -22	V V V	
2	Ringing Voltage	Vring	0	50		V_{RMS}	Note 4
3	Voltage setting for Loop Current	VREF		-10.3		V	I_{LOOP} = 25 mA, R1=R2=220 Ω V_{BAT} = -48 V
4	Operating Temperature	To	-40	+25	+85	°C	

‡ Typical figures are at 25°C with nominal supply voltages and are for design aid only
†Electrical Characteristics are over Recommended Operating Conditions unless otherwise stated.
‡Typical figures are at 25°C with nominal + 5 V supplies and are for design aid only.
Note 4: 16 to 68 Hz superimposed on a V_{BAT}.

DC Electrical Characteristics†

	Characteristics	Sym.	Min.	Typ.‡	Max.	Units	Test Conditions
1	Supply Current	I_{DD} I_{EE} I_{BAT}		 25	11 8.5 45	mA mA mA	
2	Power Consumption	PC		60	90	mW	Standby/Active
3	Constant Current Line Feed	I_{LOOP}	22	25	28	mA	V_{REF} = -10.3 V Test circuit as Fig. 6 V_{BAT} = -48 V
4	Programmable Loop Current Range	I_{LOOP}	18		32	mA	
5	Operating Loop (inclusive of Telephone Set)	R_{LOOP}	1200 450			Ω Ω	I_{LOOP} = 18 mA V_{BAT} = -48 V I_{LOOP} = 18 mA V_{BAT} = -22 V
6	Off Hook Detection Threshold	SHK		20		mA	V_{REF} = -10.3 V V_{BAT} = -48 V See Note 5. I_{LOOP} = 25 mA
7	RLYC Input Low Voltage Input High Voltage	 Vil Vih	 2.0	 0.4	 0.7	 V V	 Iil = 50 μA Iih = +50 μA
8	SHK Output Low Voltage Output High Voltage	 Vol Voh	 2.7	 	 0.4	 V V	 Iol = 8 mA Ioh = -0.4 mA
8	Dial Pulse Distortion ON OFF			+4 +4		ms ms	

†Electrical Characteristics are over Recommended Operating Conditions unless otherwise stated.
‡Typical figures are at 25°C with nominal +5 V and are for design aid only.
Note 5: Off hook detection is related to loop current.

AC Electrical Characteristics †

	Characteristics	Sym.	Min.	Typ.‡	Max.	Units	Test Conditions
1	Ring Trip Detect Time	Tt		100	300	mS	
2	Output Impedance at VX			10		Ω	
3	Gain 4-2 @ 1 kHz		-1.3	-1	-0.8	dB	Note 6 Test circuit as Fig. 8
4	Gain Relative to 1 kHz			±0.15		dB	300 Hz - 3400 Hz
5	Transhybrid Loss	THL	20	25		dB	Note 6 300 Hz - 3400 Hz Test circuit as Fig. 8
6	Gain 2-4 @ 1 kHz		-1.3	-1	-0.8	dB	Note 6 Test circuit as Fig. 7
7	Gain Relative to 1 kHz			±0.15		dB	300 Hz to 3400 Hz
8	Return Loss at 2-Wire	RL	20	30		dB	Note 6 300 Hz - 3400 Hz Test circuit as Fig. 10
9	Total Harmonic Distortion @2W @VX	THD		 0.3 0.3	 1.0 1.0	 % %	 3 dBm, 1 kHz @ 2 W 1 Vrms, 1 KHz @ 4 W
10	Common Mode Rejection 2 wire to Vx	CMR	35	42		dB	Input 0.5 Vrms, 1 KHz Test circuit as Fig. 9
11	Longitudinal to Metallic Balance	LCL		55		dB	200 Hz to 3400 Hz Test circuit as Fig. 9
12	Metallic to Longitudinal Balance			58 48		dB dB	200 Hz to 1000 Hz 1000 Hz to 3400 Hz
13	Idle Channel Noise @2W @VX	Nc			 12 12	 dBrnC dBrnC	 Cmessage Filter Cmessage Filter
14	Power Supply Rejection Ratio at 2 W and VX Vdd Vee	PSRR		 23 23		 dB dB	 0.1Vp-p @ 1kHz

†Electrical Characteristics are over Recommended Operating Conditions unless otherwise stated.
‡Typical figures are at 25°C with nominal +5 V and are for design aid only.
Note 6: Assumes $Z_o = Z_{NB} = 600\ \Omega$ and both transmit and receive gains are programmed externally to -1 dB, i.e. Gain 2-4 = -1 dB, Gain 4-2 = -1 dB.

Test Circuits

Figures 6, 7, 8, 9 and 10 are for illustrating the principles involved in making measurements and do not necessarily reflect the actual method used in production testing.

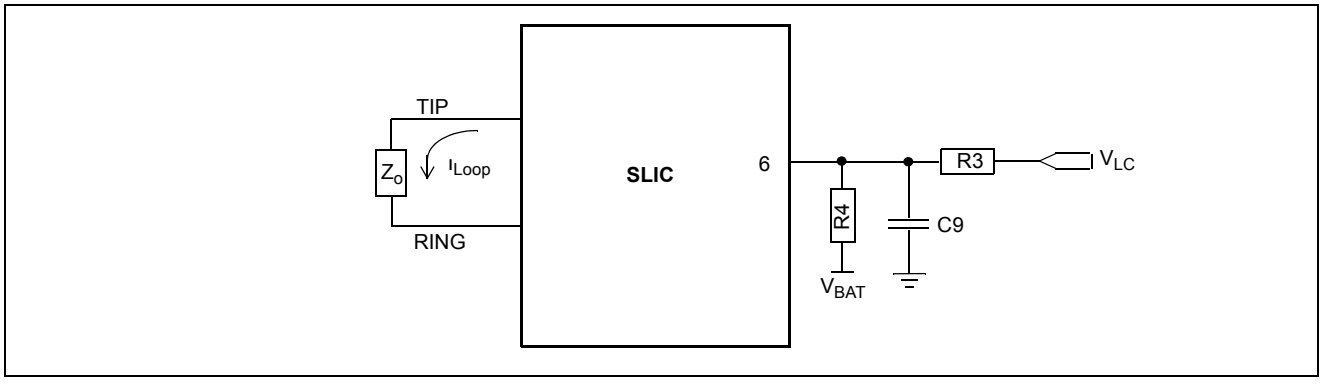


Figure 6 - Loop current programming

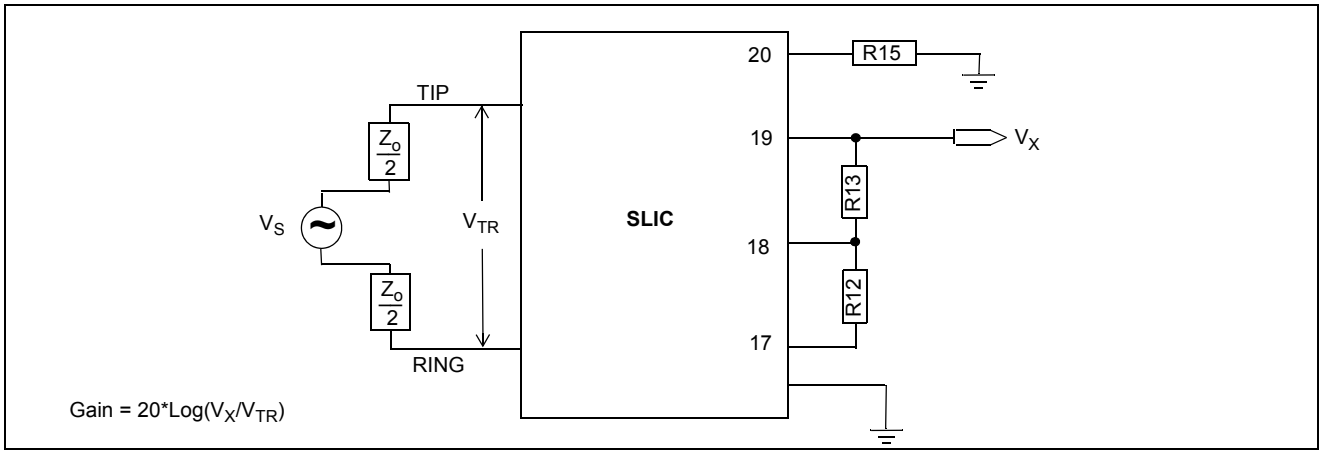


Figure 7 - 2-4 Wire Gain

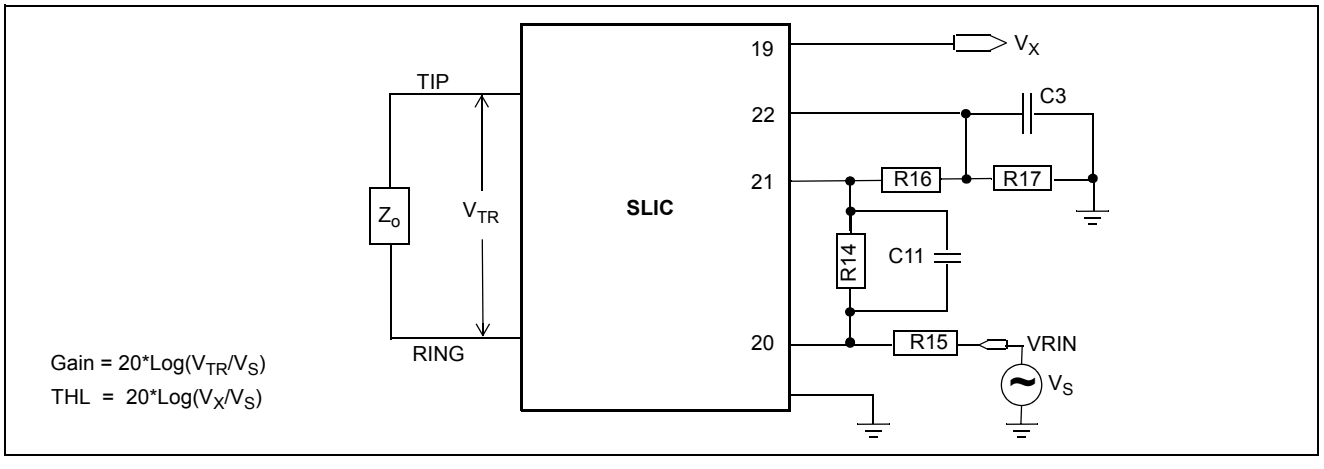


Figure 8 - 4-2 Wire Gain & Transhybrid Loss

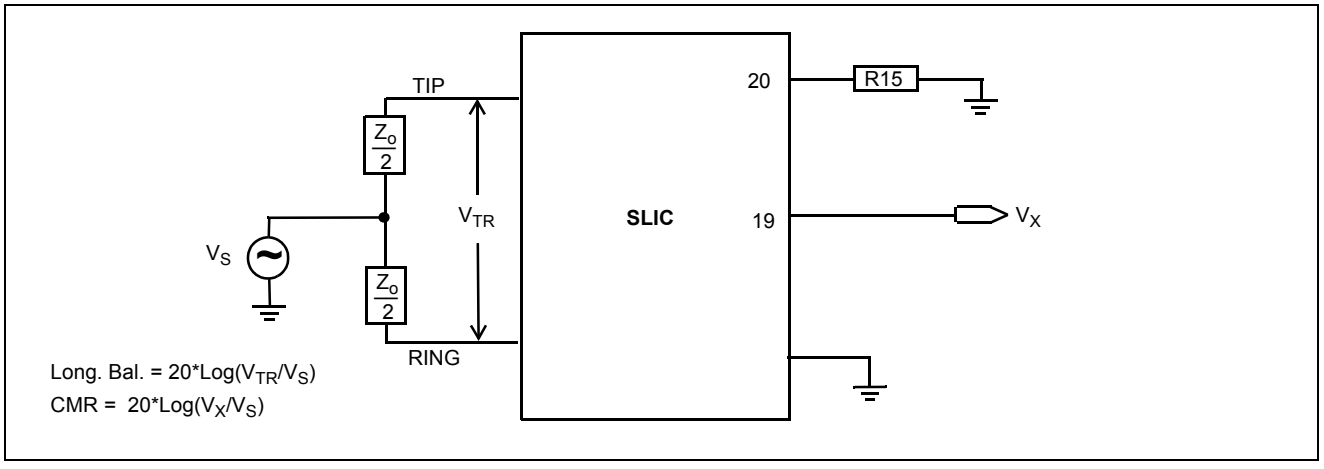


Figure 9 - Longitudinal Balance & CMR

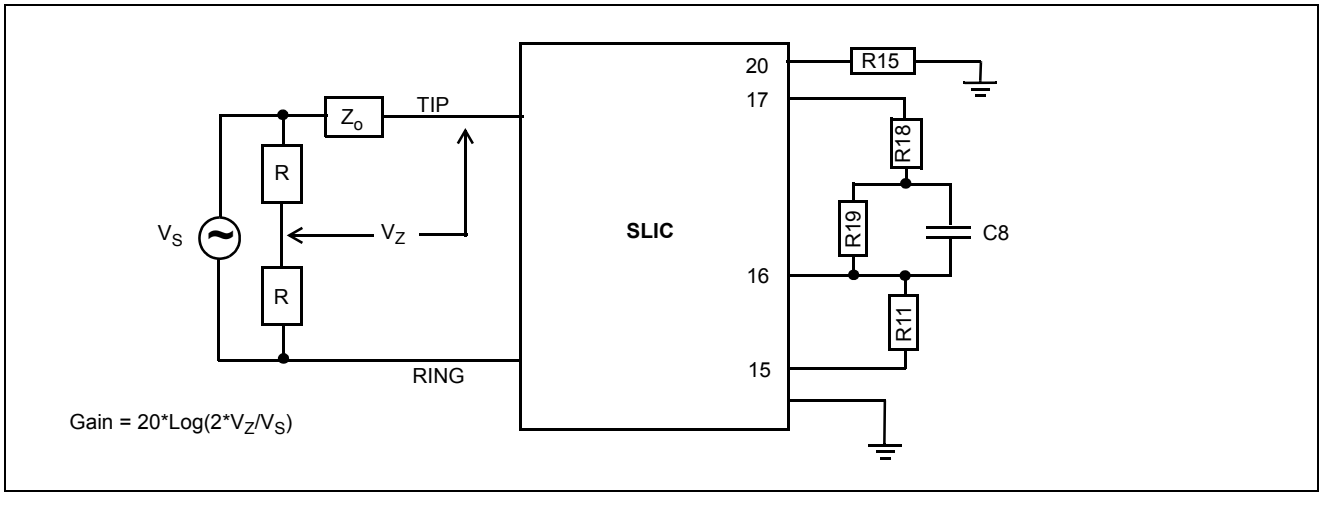
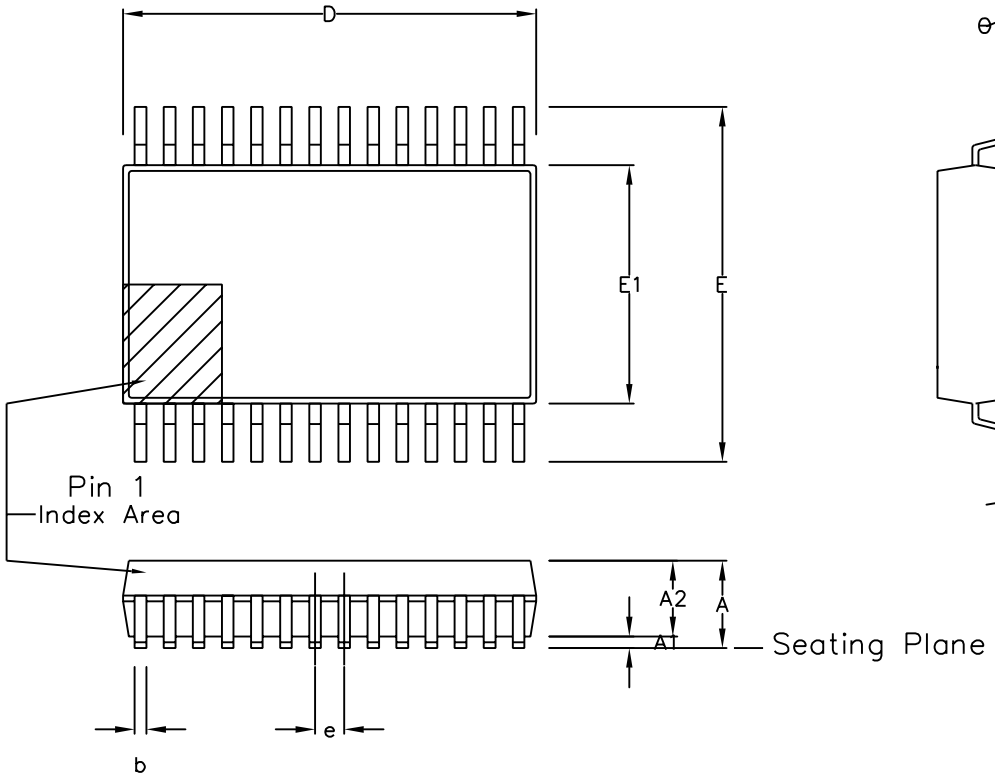


Figure 10 - Return Loss



Symbol	Control Dimensions in millimetres				Altern. Dimensions in inches		
	MIN	Nominal	MAX		MIN	Nominal	MAX
A	1.70		2.00		0.067		0.079
A1	0.05		0.20		0.002		0.008
A2	1.65		1.85		0.065		0.073
D	9.90		10.50		0.390		0.413
E	7.40		8.20		0.291		0.323
E1	5.00		5.60		0.197		0.220
L	0.55		0.95		0.022		0.037
e	0.65 BSC.				0.026 BSC.		
b	0.22		0.38		0.009		0.015
c	0.09		0.25		0.004		0.010
θ	0°		8°		0°		8°
	Pin features						
N	28						
Conforms to JEDEC MO-150 AH Iss. B							

This drawing supersedes:-
418/ED/51481/004 (Swindon/Plymouth)

Notes:
1. A visual index feature, e.g. a dot, must be located within the cross-hatched area.
2. Controlling dimension are in millimeters.
3. Dimensions D and E1 do not include mould flash or protusion. Mould flash or protusion shall not exceed 0.20 mm per side. D and E1 are maximum plastic body size dimensions including mould mismatch.
4. Dimension b does not include dambar protusion/intrusion. Allowable dambar protusion shall be 0.13 mm total in excess of b dimension. Dambar intrusion shall not reduce dimension b by more than 0.07 mm.

ISSUE	1	2	3	
ACN	201935	205232	212478	
DATE	27Feb97	25Sep98	3Apr02	
APPRD.				

ZARLINK SEMICONDUCTOR

Previous package codes
NP / N

Package Code DD

Package Outline for 28 lead SSOP (5.3mm Body Width)

GPD00296

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