

# NB4N840M

## 3.3V 3.2Gb/s Dual Differential Clock/Data 2 x 2 Crosspoint Switch with CML Output and Internal Termination

### Description

The NB4N840M is a high-bandwidth fully differential dual 2 x 2 crosspoint switch with CML inputs/outputs that is suitable for applications such as SDH/SONET, DWDM, Gigabit Ethernet and high speed switching. Fully differential design techniques are used to minimize jitter accumulation, crosstalk, and signal skew, which make this device ideal for loop-through and protection channel switching applications.

Internally terminated differential CML inputs accept AC-coupled LVPECL (Positive ECL) or direct coupled CML signals. By providing internal 50  $\Omega$  input and output termination resistor, the need for external components is eliminated and interface reflections are minimized. Differential 16 mA CML outputs provide matching internal 50  $\Omega$  terminations, and 400 mV output swings when externally terminated, 50  $\Omega$  to  $V_{CC}$ .

Single-ended LVCMOS/LVTTL SEL inputs control the routing of the signals through the crosspoint switch which makes this device configurable as 1:2 fan-out, repeater or 2 x 2 crosspoint switch. The device is housed in a low profile 5 x 5 mm 32-pin QFN package.

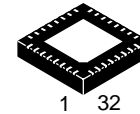
### Features

- Plug-in compatible to the MAX3840 and SY55859L
- Maximum Input Clock Frequency 2.7 GHz
- Maximum Input Data Frequency 3.2 Gb/s
- 225 ps Typical Propagation Delay
- 80 ps Typical Rise and Fall Times
- 7 ps Channel to Channel Skew
- 430 mW Power Consumption
- < 0.5 ps RMS Jitter
- 7 ps Peak-to-Peak Data Dependent Jitter
- Power Saving Feature with Disabled Outputs
- Operating Range:  $V_{CC} = 3.0\text{ V}$  to  $3.6\text{ V}$  with  $V_{EE} = 0\text{ V}$
- CML Output Level (400 mV Peak-to-Peak Output), Differential Output
- These are Pb-Free Devices



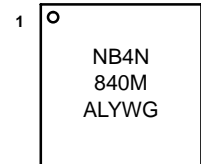
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QFN32  
MN SUFFIX  
CASE 488AM

### MARKING DIAGRAM



A = Assembly Location  
WL = Wafer Lot  
YY = Year  
WW = Work Week  
G = Pb-Free Package

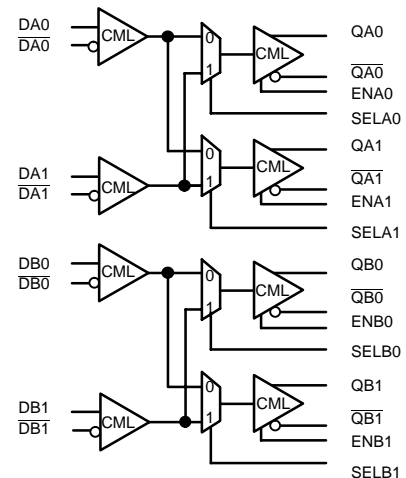


Figure 1. Functional Block Diagram

### ORDERING INFORMATION

See detailed ordering and shipping information on page 8 of this data sheet.

# NB4N840M

Table 1. TRUTH TABLE

SELA0/SELB0	SELA1/SELB1	ENA0/ENA1	ENB0/ENB1	QA0/QB0	QA1/QB1	Function
L	L	H	H	DA0/DB0	DA0/DB0	1:2 Fanout
L	H	H	H	DA0/DB0	DA1/DB1	Quad Repeater
H	L	H	H	DA1/DB1	DA0/DB0	Crosspoint Switch
H	H	H	H	DA1/DB1	DA1/DB1	1:2 Fanout
X	X	L	L	Disable/Power Down	Disable/Power Down	No output (@ V <sub>CC</sub> )

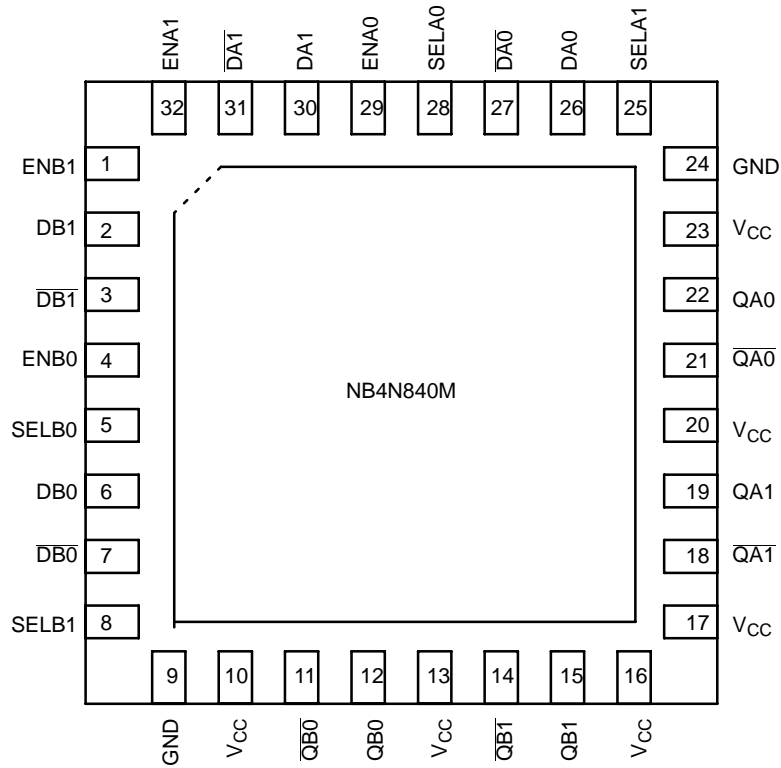


Figure 2. Pin Configuration (Top View)

# NB4N840M

**Table 2. PIN DESCRIPTION**

Pin	Name	I/O	Description
1	ENB1	LVTTTL	Channel B1 Output Enable. LVTTTL low input powers down B1 output stage.
2	DB1	CML Input	Channel B1 Positive Signal Input
3	$\overline{DB1}$	CML Input	Channel B1 Negative Signal Input
4	ENB0	LVTTTL	Channel B0 Output Enable. LVTTTL low input powers down B0 output stage.
5	SELB0	LVTTTL	Channel B0 Output Select. See Table 1.
6	DB0	CML Input	Channel B0 Positive Signal Input
7	$\overline{DB0}$	CML Input	Channel B0 Negative Signal Input
8	SELB1	LVTTTL	Channel B1 Output Select. See Table 1.
9,24	GND	–	Supply Ground. All GND pins must be externally connected to power supply to guarantee proper operation.
10, 13, 16, 17, 20, 23	V <sub>CC</sub>	–	Positive Supply. All V <sub>CC</sub> pins must be externally connected to power supply to guarantee proper operation.
11	$\overline{QB0}$	CML Output	Channel B0 Negative Output.
12	QB0	CML Output	Channel B0 Positive Output.
14	$\overline{QB1}$	CML Output	Channel B1 Negative Output.
15	QB1	CML Output	Channel B1 Positive Output.
18	$\overline{QA1}$	CML Output	Channel A1 Negative Output.
19	QA1	CML Output	Channel A1 Positive Output.
21	$\overline{QA0}$	CML Output	Channel A0 Negative Output.
22	QA0	CML Output	Channel A0 Positive Output.
25	SELA1	LVTTTL	Channel A1 Output Select, LVTTTL Input. See Table 1.
26	DA0	CML Input	Channel A0 Positive Signal Input.
27	$\overline{DA0}$	CML Input	Channel A0 Negative Signal Input.
28	SELA0	LVTTTL	Channel A0 Output Select, LVTTTL Input. See Table 1.
29	ENA0	LVTTTL	Channel A0 Output Enable. LVTTTL low input powers down A0 output stage.
30	DA1	CML Input	Channel A1 Positive Signal Input.
31	$\overline{DA1}$	CML Input	Channel A1 Negative Signal Input.
32	ENA1	LVTTTL	Channel A1 Output Enable. LVTTTL low input powers down A1 output stage.
–	EP	GND	Exposed Pad. The thermally exposed pad (EP) on package bottom (see case drawing) must be attached to a heat-sinking conduit. The exposed pad must be soldered to the circuit board GND for proper electrical and thermal operation.

# NB4N840M

**Table 3. ATTRIBUTES**

Characteristics		Value
ESD Protection	Human Body Model Machine Model	> 2000 V > 110 V
Moisture Sensitivity (Note 1)	QFN-32	Level 1
Flammability Rating	Oxygen Index: 28 to 34	UL 94 V-0 @ 0.125 in
Transistor Count		380
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test		

1. For additional information, refer to Application Note AND8003/D.

**Table 4. MAXIMUM RATINGS**

Symbol	Parameter	Condition 1	Condition 2	Rating	Unit
V <sub>CC</sub>	Positive Power Supply	GND = 0 V		3.8	V
V <sub>I</sub>	Positive Input	GND = 0 V	GND = V <sub>I</sub> = V <sub>CC</sub>	3.8	V
V <sub>INPP</sub>	Differential Input Voltage	D - $\bar{D}$		3.8	V
I <sub>IN</sub>	Input Current Through Internal 50 $\Omega$ Resistor	Static Surge		45 80	mA mA
I <sub>OUT</sub>	Output Current	Continuous Surge		25 80	mA mA
T <sub>A</sub>	Operating Temperature Range	QFN-32		-40 to +85	°C
T <sub>stg</sub>	Storage Temperature Range			-65 to +150	°C
$\theta_{JA}$	Thermal Resistance (Junction-to-Ambient) (Note 2)	0 lfpm 500 lfpm	QFN-32 QFN-32	31 27	°C/W °C/W
$\theta_{JC}$	Thermal Resistance (Junction-to-Case)	2S2P (Note 3)	QFN-32	12	°C/W
T <sub>sol</sub>	Wave Solder Pb-Free	<3 sec @ 260 C		260	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

2. JEDEC standard 51-6, multilayer board - 2S2P (2 signal, 2 power).

3. JEDEC standard multilayer board - 2S2P (2 signal, 2 power) with 8 filled thermal vias under exposed pad.

# NB4N840M

**Table 5. DC CHARACTERISTICS, CLOCK INPUTS, CML OUTPUTS**  $V_{CC} = 3.0\text{ V to }3.6\text{ V}$ ,  $T_A = -40^\circ\text{C to }+85^\circ\text{C}$

Symbol	Characteristic	Min	Typ	Max	Unit
$I_{CC}$	Power Supply Current (All outputs enabled)		130	170	mA
$V_{out,diff}$	CML Differential Output Swing (Note 4, Figures 5 and 12)	640	800	1000	mV
$V_{CMR}$ (Note 6)	CML Output Common Mode Voltage (Loaded $50\ \Omega$ to $V_{CC}$ )		$V_{CC} - 200$		mV
	CML Single-Ended Input Voltage Range	$V_{CC} - 0.8$		$V_{CC} + 0.4$	mV
$V_{ID}$	Differential Input Voltage ( $V_{IHD} - V_{ILD}$ )	300		1600	mV

## LVTTTL CONTROL INPUT PINS

$V_{IH}$	Input HIGH Voltage (LVTTTL Inputs)	2000			mV
$V_{IL}$	Input LOW Voltage (LVTTTL Inputs)			800	mV
$I_{IH}$	Input HIGH Current (LVTTTL Inputs)	-10		10	$\mu\text{A}$
$I_{IL}$	Input LOW Current (LVTTTL Inputs)	-10		10	$\mu\text{A}$
$R_{TIN}$	CML Single-Ended Input Resistance	42.5	50	57.5	$\Omega$
$R_{TOUT}$	Differential Output Resistance	85	100	115	$\Omega$

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

4. CML outputs require  $50\ \Omega$  receiver termination resistors to  $V_{CC}$  for proper operation (Figure 10).

5. Input and output parameters vary 1:1 with  $V_{CC}$ .

6.  $V_{CMR}$  min varies 1:1 with  $V_{EE}$ ,  $V_{CMR}$  max varies 1:1 with  $V_{CC}$ .

**Table 6. AC CHARACTERISTICS**  $V_{CC} = 3.0\text{ V to }3.6\text{ V}$ ,  $V_{EE} = 0\text{ V}$  (Note 7, Figure 9)

Symbol	Characteristic	$-40^\circ\text{C}$			$25^\circ\text{C}$			$85^\circ\text{C}$			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$V_{OUTPP}$	Output Voltage Amplitude (@ $V_{INPPmin}$ ) (See Figure 3) $f_{in} \leq 2\text{ GHz}$ $f_{in} \leq 3\text{ GHz}$ $f_{in} \leq 3.5\text{ GHz}$	280	365		280	365		280	365		mV
$f_{DATA}$	Maximum Operating Data Rate	3.2			3.2			3.2			Gb/s
$t_{PLH}$ , $t_{PHL}$	Propagation Delay to Output Differential $D/\bar{D}$ to $Q/\bar{Q}$	140	225	340	140	225	340	140	225	340	ps
$t_{SKEW}$	Duty Cycle Skew (Note 8) Within-Device Skew (Figure 4) Device-to-Device Skew (Note 12)		5	25		5	25		5	25	ps
$t_{JITTER}$	RMS Random Clock Jitter (Note 10) $f_{in} \leq 3.2\text{ GHz}$ Peak-to-Peak Data Dependent Jitter $f_{in} = 2.5\text{ Gb/s}$ (Note 11) $f_{in} = 3.2\text{ Gb/s}$		0.15	0.5		0.15	0.5		0.15	0.5	ps
			7	20		7	20		7	20	
			7	20		7	20		7	20	
	Crosstalk-Induced RMS Jitter (Note 13)			0.5			0.5			0.5	ps
$V_{INPP}$	Input Voltage Swing/Sensitivity (Differential Configuration) (Note 9)	150		800	150		800	150		800	mV
$t_r$ , $t_f$	Output Rise/Fall Times @ 0.5 GHz (20% – 80%)		80	135		80	135		80	135	ps

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

7. Measured by forcing  $V_{INPP}$  (MIN) from a 50% duty cycle clock source. All loading with an external  $R_L = 50\ \Omega$  to  $V_{CC}$ . Input edge rates 40 ps (20% – 80%).

8. Duty cycle skew is measured between differential outputs using the deviations of the sum of  $T_{pw-}$  and  $T_{pw+}$  @ 0.5 GHz.

9.  $V_{INPP}$  (MAX) cannot exceed 800 mV. Input voltage swing is a single-ended measurement operating in differential mode.

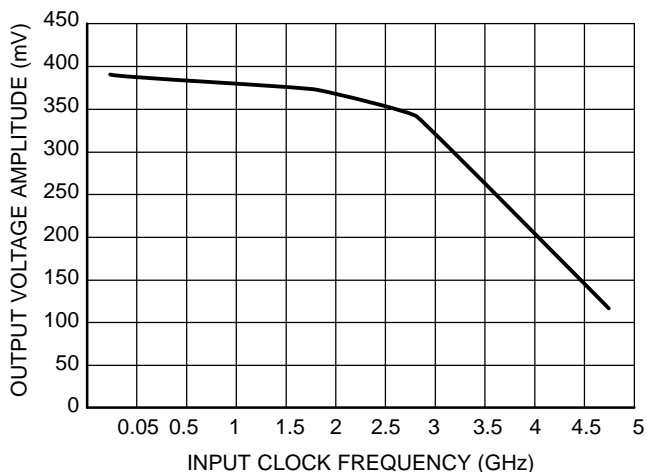
10. Additive RMS jitter using 50% duty cycle clock input signal.

11. Additive peak-to-peak data dependent jitter using input data pattern with PRBS 2<sup>23</sup>-1 and K28.5,  $V_{INPP} = 400\text{ mV}$ .

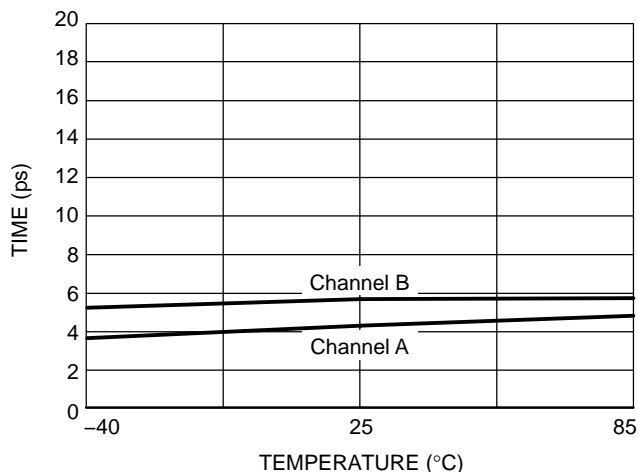
12. Device to device skew is measured between outputs under identical transition @ 0.5 GHz.

13. Data taken on the same device under identical condition.

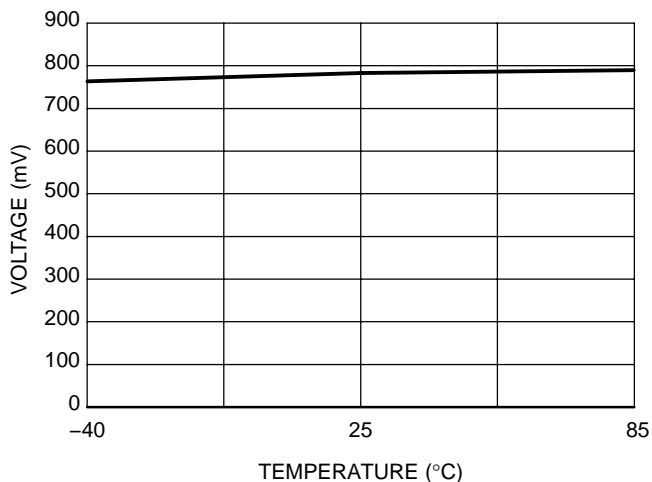
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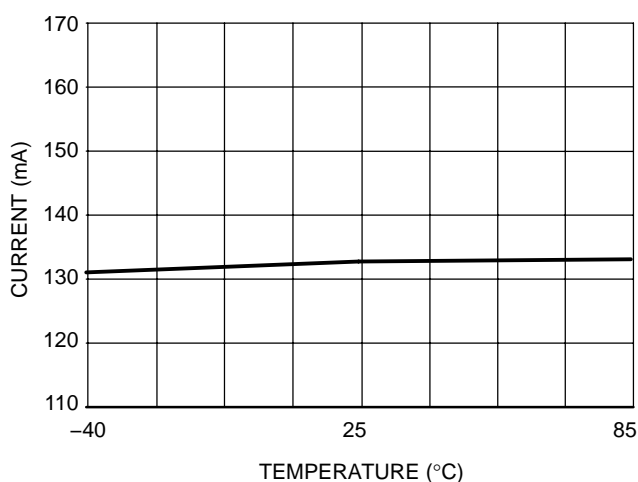
**Figure 3. Output Voltage Amplitude ( $V_{OUTPP}$ ) vs. Input Clock Frequency ( $f_{IN}$ ) at Ambient Temperature (Typ)**



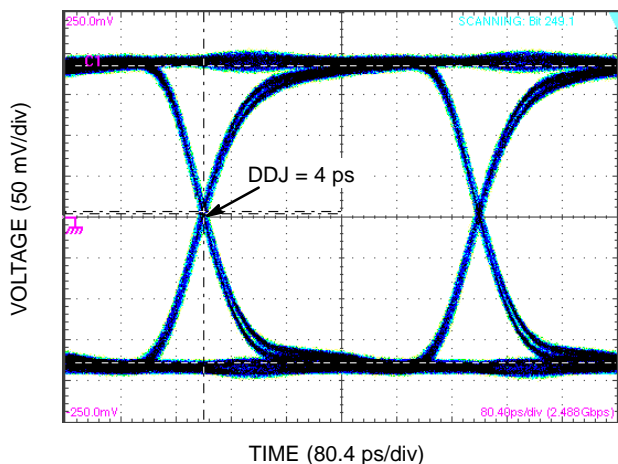
**Figure 4. Within-Device Skew vs. Temperature at  $V_{CC} = 3.3 V$**



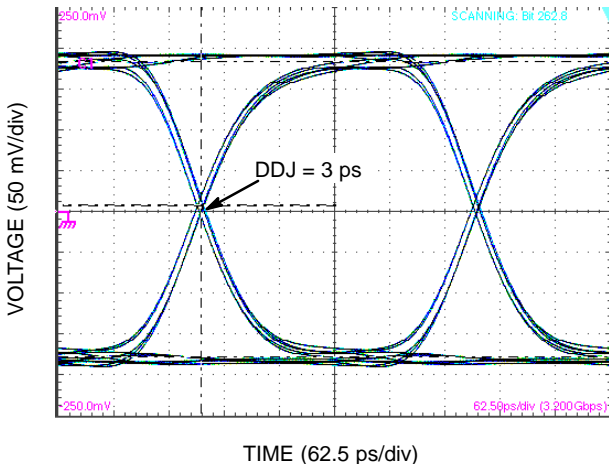
**Figure 5. CML Differential Voltage vs. Temperature**



**Figure 6. Supply Current vs. Temperature (All 4 Outputs Enabled)**



**Figure 7. Typical Output Waveform at 2.488 Gb/s with PRBS 2<sup>23</sup>-1 (Input Signal DDJ = 12 ps)**



**Figure 8. Typical Output Waveform at 3.2 Gb/s with K28.5 (Input Signal DDJ = 14 ps)**

# NB4N840M

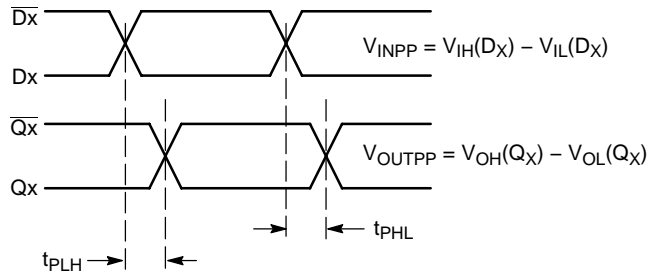


Figure 9. AC Reference Measurement

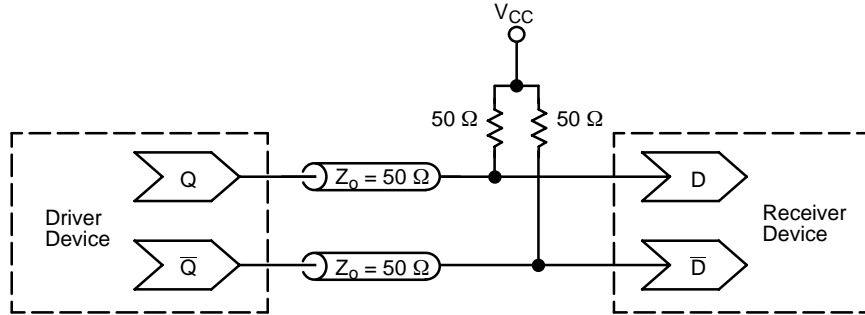


Figure 10. Typical Termination for Output Driver and Device Evaluation  
(See Application Note AND8173/D)

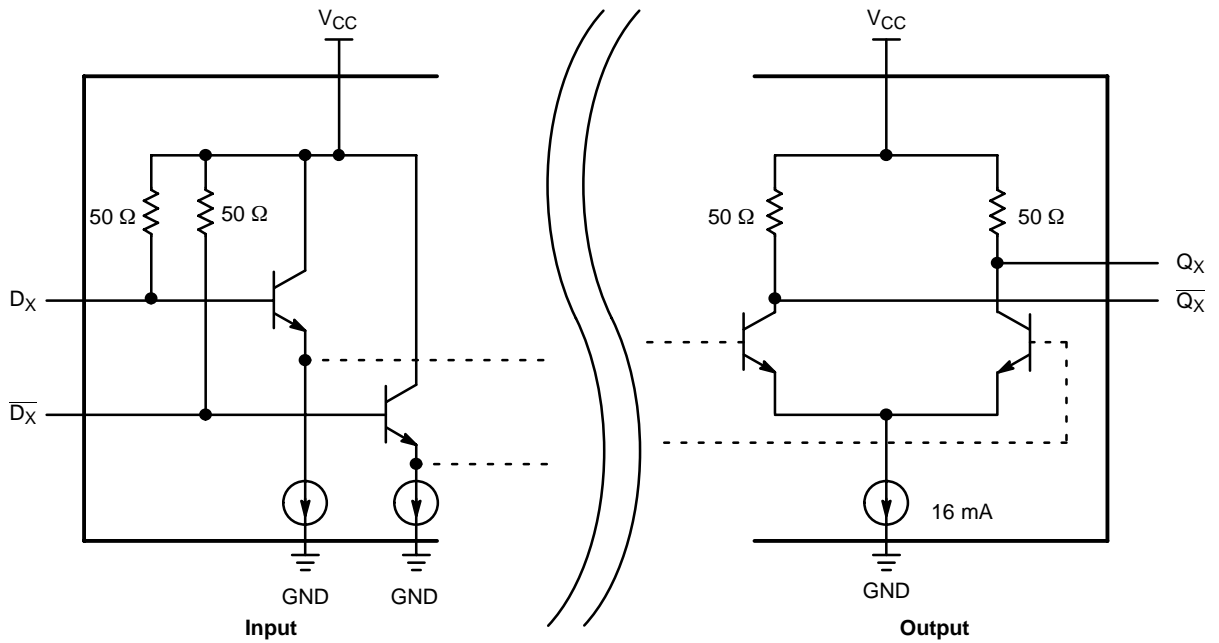


Figure 11. CML Input and Output Structure

# NB4N840M

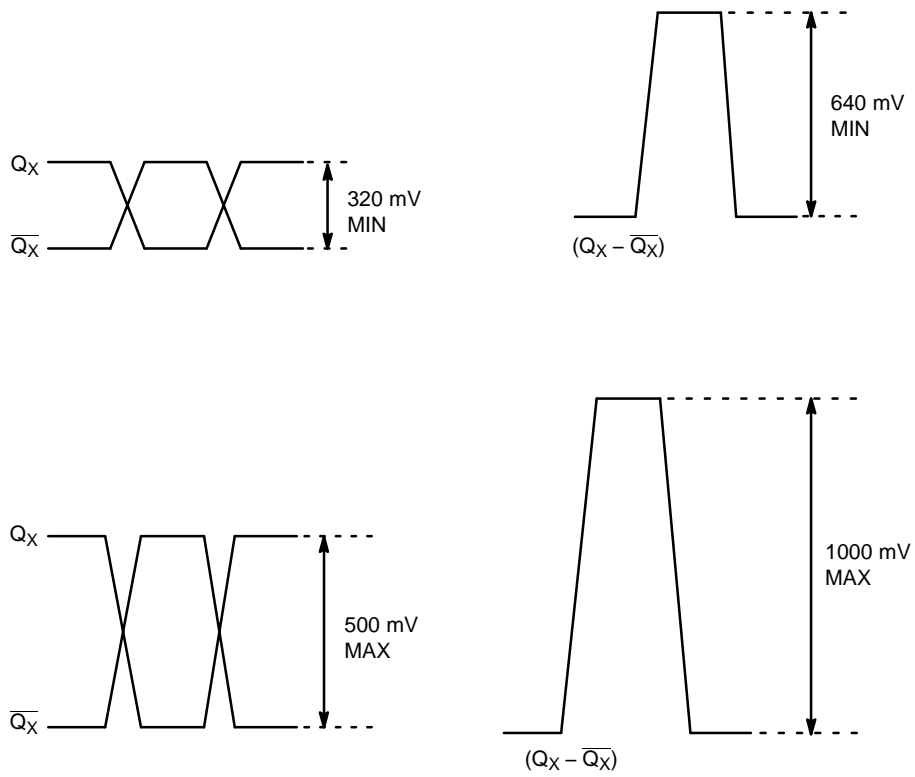


Figure 12. CML Output Levels

## ORDERING INFORMATION

Device	Package	Shipping
NB4N840MMNG	QFN32 (Pb-Free)	74 Units / Rail
NB4N840MMNR4G	QFN32 (Pb-Free)	1000 / Tape & Reel

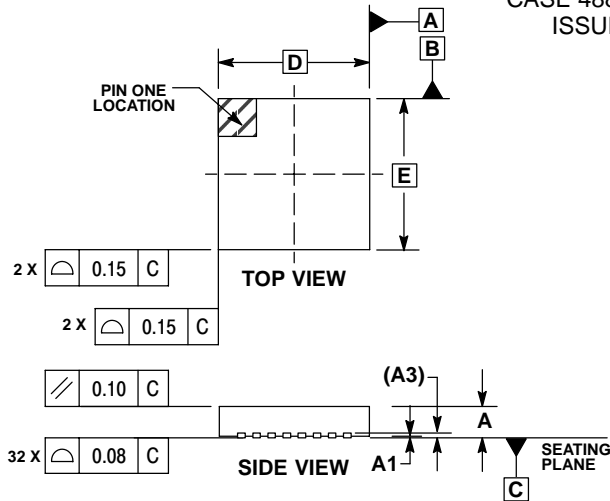
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.



# NB4N840M

## PACKAGE DIMENSIONS

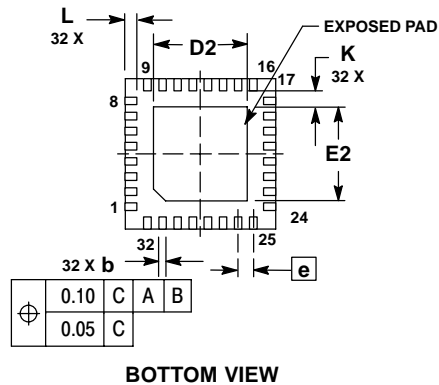
QFN32 5\*5\*1 0.5 P  
CASE 488AM-01  
ISSUE O



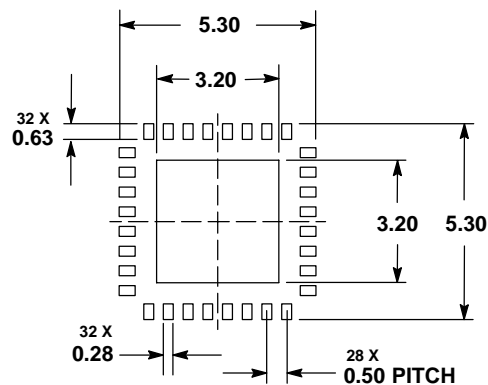
### NOTES:

1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM TERMINAL
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.800	0.900	1.000
A1	0.000	0.025	0.050
A3	0.200 REF		
b	0.180	0.250	0.300
D	5.00 BSC		
D2	2.950	3.100	3.250
E	5.00 BSC		
E2	2.950	3.100	3.250
e	0.500 BSC		
K	0.200	---	---
L	0.300	0.400	0.500



### SOLDERING FOOTPRINT\*



\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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