NBSG11

2.5V/3.3V SiGe 1:2 Differential Clock Driver with RSECL* Outputs

*Reduced Swing ECL

The NBSG11 is a 1-to-2 differential fanout buffer, optimized for low skew and ultra-low JITTER.

Inputs incorporate internal 50 Ω termination resistors and accept NECL (Negative ECL), PECL (Positive ECL), CML, LVCMOS, LVTTL, or LVDS. Outputs are RSECL (Reduced Swing ECL), 400 mV.

- Maximum Input Clock Frequency up to 12 GHz Typical
- Maximum Input Data Rate up to 12 Gb/s Typical
- 30 ps Typical Rise and Fall Times
- 125 ps Typical Propagation Delay
- RSPECL Output with Operating Range: V_{CC} = 2.375 V to 3.465 V with V_{EE} = 0 V
- RSNECL Output with RSNECL or NECL Inputs with Operating Range: V_{CC} = 0 V with V_{EE} = -2.375 V to -3.465 V
- RSECL Output Level (400 mV Peak-to-Peak Output), Differential Output Only
- 50 Ω Internal Input Termination Resistors
- Compatible with Existing 2.5 V/3.3 V LVEP, EP, and LVEL Devices

ON Semiconductor®

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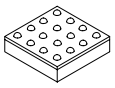
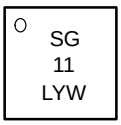
MARKING DIAGRAM*



FCBGA-16
BA SUFFIX
CASE 489



QFN-16
MN SUFFIX
CASE 485G

A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week

*For further details, refer to Application Note AND8002/D

ORDERING INFORMATION

Device	Package	Shipping
NBSG11BA	4x4 mm FCBGA-16	100 Units / Tray
NBSG11BAR2	4x4 mm FCBGA-16	500 / Tape & Reel
NBSG11MN	3x3 mm QFN-16	123 Units / Rail
NBSG11MNR2	3x3 mm QFN-16	3000 / Tape & Reel

Board	Description
NBSG11BAEVB	NBSG11BA Evaluation Board

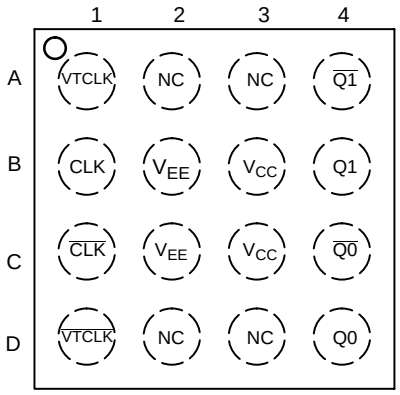


Figure 1. BGA-16 Pinout (Top View)

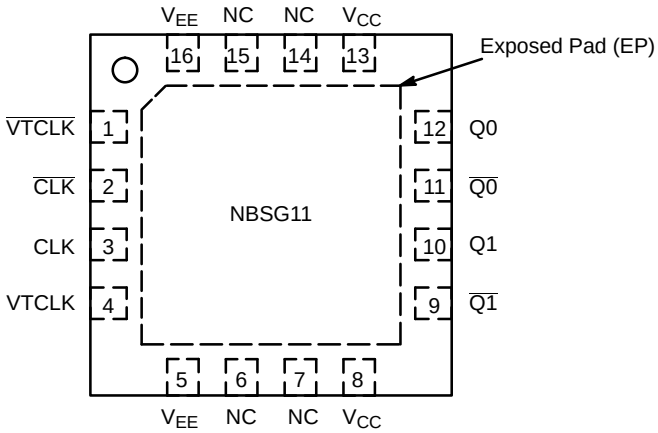


Figure 2. QFN-16 Pinout (Top View)

Table 1. Pin Description

Pin		Name	I/O	Description
BGA	QFN			
D1	1	$\overline{VTCLK}$	-	Internal 50 Ω Termination Pin. See Table 2.
C1	2	$\overline{CLK}$	ECL, CML, LVCMOS, LVDS, LVTTL Input	Inverted Differential Input. Internal 75 kΩ to V_{EE} and 36.5 kΩ to V_{CC}.
B1	3	CLK	ECL, CML, LVCMOS, LVDS, LVTTL Input	Noninverted Differential Input. Internal 75 kΩ to V_{EE}.
A1	4	VTCLK	-	Internal 50 Ω Termination Pin. See Table 2.
B2,C2	5,16	V_{EE}	-	Negative Supply Voltage
A2,A3,D2, D3	6,7,14,15	NC	-	No Connect
B3,C3	8,13	V_{CC}	-	Positive Supply Voltage
A4	9	$\overline{Q1}$	RSECL Output	Inverted Differential Output 1. Typically Terminated with 50 Ω to $V_{TT} = V_{CC}$ - 2 V
B4	10	Q1	RSECL Output	Noninverted Differential Output 1. Typically Terminated with 50 Ω to $V_{TT} = V_{CC}$ - 2 V
C4	11	$\overline{Q0}$	RSECL Output	Inverted Differential output 0. Typically Terminated with 50 Ω to $V_{TT} = V_{CC}$ - 2 V
D4	12	Q0	RSECL Output	Noninverted Differential Output 0. Typically Terminated with 50 Ω to $V_{TT} = V_{CC}$ - 2 V
N/A	-	EP	-	Exposed Pad (Note 2)

1. The NC pins are electrically connected to the die and must be left open.
2. All V_{CC} and V_{EE} pins must be externally connected to Power Supply to guarantee proper operation. The thermally exposed pad on package bottom (see case drawing) must be attached to a heat-sinking conduit.
3. In the differential configuration when the input termination pins (VTCLK, $\overline{VTCLK}$) are connected to a common termination voltage, and if no signal is applied then the device will be susceptible to self-oscillation.

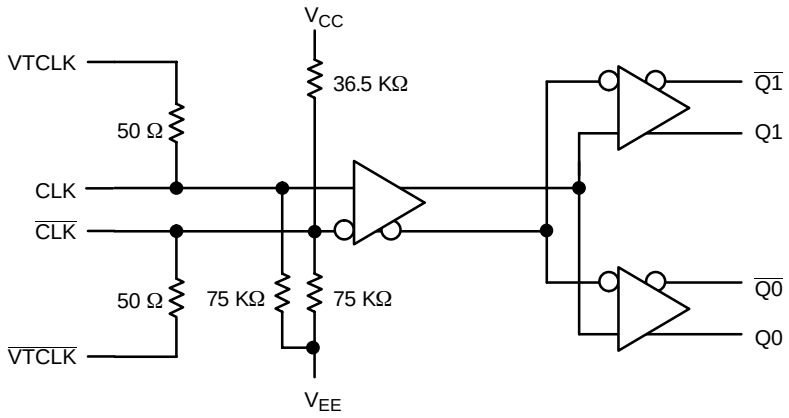


Figure 3. Logic Diagram

Table 2. Interfacing Options

INTERFACING OPTIONS	CONNECTIONS
CML	Connect VTCLK and $\overline{\text{VTCLK}}$ to V_{CC}
LVDS	Connect VTCLK and $\overline{\text{VTCLK}}$ together
AC-COUPLED	Bias VTCLK and $\overline{\text{VTCLK}}$ Inputs within (VIHCMR) Common Mode Range
RSECL, PECL, NECL	Standard ECL Termination Techniques
LVTTL, LVCMOS	An external voltage should be be applied to the unused complementary differential input. Nominal voltage is 1.5 V for LVTTL and $V_{CC}/2$ for LVCMOS inputs.

Table 3. ATTRIBUTES

Characteristics		Value
Internal Input Pulldown Resistor (CLK, $\overline{\text{CLK}}$)		75 kΩ
Internal Input Pullup Resistor ($\overline{\text{CLK}}$)		36.5 kΩ
ESD Protection	Human Body Model Machine Model	> 2 kV > 100 V
Moisture Sensitivity (Note 4)	FCBGA-16 QFN-16	Level 3 Level 1
Flammability Rating	Oxygen Index: 28 to 34	UL 94 V-0 @ 0.125 in
Transistor Count		125
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test		

4. For additional information, see Application Note AND8003/D.

Table 4. MAXIMUM RATINGS (Note 5)

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V_{CC}	Positive Power Supply	V_{EE} = 0 V		3.6	V
V_{EE}	Negative Power Supply	V_{CC} = 0 V		-3.6	V
V_I	Positive Input Negative Input	V_{EE} = 0 V V_{CC} = 0 V	$V_I \le V_{CC}$ $V_I \ge V_{EE}$	3.6 -3.6	V V
V_{INPP}	Differential Input Voltage $\lvert D - \overline{D} \rvert$	$V_{CC} - V_{EE} \ge$ 2.8 V $V_{CC} - V_{EE} <$ 2.8 V		2.8 $\lvert V_{CC} - V_{EE} \rvert$	V V
I_{out}	Output Current	Continuous Surge		25 50	mA mA
T_A	Operating Temperature Range	16 FCBGA 16 QFN		-40 to +70 -40 to +85	°C
T_{stg}	Storage Temperature Range			-65 to +150	°C
θ_{JA}	Thermal Resistance (Junction-to-Ambient) (Note 6)	0 LFPM 500 LFPM 0 LFPM 500 LFPM	16 FCBGA 16 FCBGA 16 QFN 16 QFN	108 86 41.6 35.2	°C/W °C/W °C/W °C/W
θ_{JC}	Thermal Resistance (Junction-to-Case)	1S2P (Note 6) 2S2P (Note 7)	16 FCBGA 16 QFN	5.0 4.0	°C/W °C/W
T_{sol}	Wave Solder	< 15 Seconds		225	°C

5. Maximum Ratings are those values beyond which device damage may occur.
6. JEDEC standard multilayer board - 1S2P (1 signal, 2 power).
7. JEDEC standard multilayer board - 2S2P (2 signal, 2 power) with 8 filled thermal vias under exposed pad.

Table 5. DC CHARACTERISTICS, INPUT WITH RSPECL OUTPUT V_{CC} = 2.5 V; V_{EE} = 0 V (Note 8)

		-40 °C			25°C			70°C(BGA)/85°C(QFN)**			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Negative Power Supply Current	45	60	75	45	60	75	45	60	75	mA
V_{OH}	Output HIGH Voltage (Note 9)	1450	1530	1575	1525	1565	1600	1550	1590	1625	mV
V_{OUTPP}	Output Amplitude Voltage	350	410	525	350	410	525	350	410	525	mV
V_{IH}	Input HIGH Voltage (Single-Ended) (Note 11)	V_{CC}-1435 mV	V_{CC}-1000 mV*	V_{CC}	V_{CC}-1435 mV	V_{CC}-1000 mV*	V_{CC}	V_{CC}-1435 mV	V_{CC}-1000 mV*	V_{CC}	V
V_{IL}	Input LOW Voltage (Single-Ended) (Note 12)	V_{IH}-2.5 V	V_{CC}-1400 mV*	V_{IH}-150 mV	V_{IH}-2.5 V	V_{CC}-1400 mV*	V_{IH}-150 mV	V_{IH}-2.5 V	V_{CC}-1400 mV*	V_{IH}-150 mV	V
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 10)	1.2		2.5	1.2		2.5	1.2		2.5	V
R_{TIN}	Internal Input Termination Resistor	45	50	55	45	50	55	45	50	55	Ω
I_{IH}	Input HIGH Current (@ V_{IH}, V_{IHMAX})		80	150		80	150		80	150	μA
I_{IL}	Input LOW Current (@ V_{IL}, V_{ILMIN})		25	100		25	100		25	100	μA

NOTE: SiGe circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500 lfpm is maintained.

8. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.125 V to -0.965 V.
9. All loading with 50 Ω to V_{CC} - 2.0 V. V_{OH}/V_{OL} measured at V_{IH}/V_{IL}.
10. V_{IHCMR} min varies 1:1 with V_{EE}, V_{IHCMR} max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal.
11. V_{IH} cannot exceed V_{CC}.
12. V_{IL} always ≥ V_{EE}.

*Typicals used for testing purposes.

**The device packaged in FCBGA-16 have maximum temperature specification of 70°C and devices packaged in QFN-16 have maximum temperature specification of 85°C.

Table 6. DC CHARACTERISTICS, INPUT WITH RSPECL OUTPUT V_{CC} = 3.3 V; V_{EE} = 0 V (Note 13)

Symbol	Characteristic	-40 °C			25°C			70°C(BGA)/85°C(QFN)**			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Negative Power Supply Current	45	60	75	45	60	75	45	60	75	mA
V_{OH}	Output HIGH Voltage (Note 14)	2250	2330	2375	2325	2365	2400	2350	2390	2425	mV
V_{OUTPP}	Output Amplitude Voltage	350	410	525	350	410	525	350	410	525	mV
V_{IH}	Input HIGH Voltage (Single-Ended) (Note 16)	V_{CC}- 1435 mV	V_{CC}- 1000 mV*	V_{CC}	V_{CC}- 1435 mV	V_{CC}- 1000 mV*	V_{CC}	V_{CC}- 1435 mV	V_{CC}- 1000 mV*	V_{CC}	V
V_{IL}	Input LOW Voltage (Single-Ended) (Note 17)	V_{IH}- 2.5 V	V_{CC}- 1400 mV*	V_{IH}- 150 mV	V_{IH}- 2.5 V	V_{CC}- 1400 mV*	V_{IH}- 150 mV	V_{IH}- 2.5 V	V_{CC}- 1400 mV*	V_{IH}- 150 mV	V
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Note 15) (Differential Configuration)	1.2		3.3	1.2		3.3	1.2		3.3	V
R_{TIN}	Internal Input Termination Resistor	45	50	55	45	50	55	45	50	55	Ω
I_{IH}	Input HIGH Current (@ V_{IH}, V_{IHMAX})		80	150		80	150		80	150	μA
I_{IL}	Input LOW Current (@ V_{IL}, V_{ILMIN})		25	100		25	100		25	100	μA

NOTE: SiGe Circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500 lfpm is maintained.

13. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.925 V to -0.165 V.
14. All loading with 50 Ω to V_{CC} - 2.0 V. V_{OH}/V_{OL} measured at V_{IH}/V_{IL}.
15. V_{IHCMR} min varies 1:1 with V_{EE}, V_{IHCMR} max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal.
16. V_{IH} cannot exceed V_{CC}.
17. V_{IL} always ≥ V_{EE}.

*Typicals used for testing purposes.

**The device packaged in FCBGA-16 have maximum temperature specification of 70°C and devices packaged in QFN-16 have maximum temperature specification of 85°C.

Table 7. DC CHARACTERISTICS, NECL OR RSNECL INPUT WITH NECL OUTPUT

V_{CC} = 0 V; V_{EE} = -3.465 V to -2.375 V (Note 18)

		-40 °C			25°C			70°C(BGA)/85°C(QFN)**			
Symbol	**Characteristic**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
I_{EE}	Negative Power Supply Current	45	60	75	45	60	75	45	60	75	mA
VOH	Output HIGH Voltage (Note 19)	-1050	-970	-925	-975	-935	-900	-950	-910	-875	mV
V_{OUTPP}	Output Amplitude Voltage	350	410	525	350	410	525	350	410	525	mV
V_{IH}	Input HIGH Voltage (Single-Ended) (Note 21)	V_{CC}- 1435 mV	V_{CC}- 1000 mV*	V_{CC}	V_{CC}- 1435 mV	V_{CC}- 1000 mV*	V_{CC}	V_{CC}- 1435 mV	V_{CC}- 1000 mV*	V_{CC}	V
V_{IL}	Input LOW Voltage (Single-Ended) (Note 22)	V_{IH}- 2.5 V	V_{CC}- 1400 mV*	V_{IH}- 150 mV	V_{IH}- 2.5 V	V_{CC}- 1400 mV*	V_{IH}- 150 mV	V_{IH}- 2.5 V	V_{CC}- 1400 mV*	V_{IH}- 150 mV	V
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 20)	V_{EE}+1.2		0.0	V_{EE}+1.2		0.0	V_{EE}+1.2		0.0	V
R_{TIN}	Internal Input Termination Resistor	45	50	55	45	50	55	45	50	55	Ω
I_{IH}	Input HIGH Current (@ V_{IH}, V_{IHMAX})		80	150		80	150		80	150	μA
I_{IL}	Input LOW Current (@ V_{IL}, V_{ILMIN})		25	100		25	100		25	100	μA

NOTE: SiGe circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500lfpm is maintained.

18. Input and output parameters vary 1:1 with V_{CC}.
19. All loading with 50 Ω to V_{CC} - 2.0 V. V_{OH}/V_{OL} measured at V_{IH}/V_{IL}.
20. V_{IHCMR} min varies 1:1 with V_{EE}, V_{IHCMR} max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal.
21. V_{IH} cannot exceed V_{CC}.
22. V_{IL} always ≥ V_{EE}.

*Typicals used for testing purposes.

**The device packaged in FCBGA-16 have maximum temperature specification of 70°C and devices packaged in QFN-16 have maximum temperature specification of 85°C.

Table 8. AC CHARACTERISTICS for FCBGA-16

V_{CC} = 0 V; V_{EE} = -3.465 V to -2.375 V or V_{CC} = 2.375 V to 3.465 V; V_{EE} = 0 V

		-40 °C			25°C			70°C			
Symbol	**Characteristic**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
f_{max}	Maximum Frequency (See Figure 4. F_{max}/JITTER) (Note 23)	10.709	12		10.709	12		10.709	12		GHz
t_{PLH}, t_{PHL}	Propagation Delay to Output Differential	90	125	160	90	125	160	90	125	160	ps
t_{SKEW}	Duty Cycle Skew (Note 24) Within-Device Skew (Note 25) Device-to-Device Skew (Note 26)		3 6 25	15 15 50		3 6 25	15 15 50		3 6 25	15 15 50	ps
t_{JITTER}	RMS Random Clock Jitter f_{in} < 10 GHz Peak-to-Peak Data Dependent Jitter f_{in} < 10 Gb/s		0.2 TBD	1		0.2 TBD	1		0.2 TBD	1	ps
V_{INPP}	Input Voltage Swing/Sensitivity (Differential Configuration) (Note 27)	75		2600	75		2600	75		2600	mV
t_r t_f	Output Rise/Fall Times Q, $\overline{Q}$ (20% - 80%) @ 1 GHz	20	30	55	20	30	55	20	30	55	ps

23. Measured using a 500 mV source, 50% duty cycle clock source. All loading with 50 Ω to V_{CC}-2.0 V. For minimum f_{max} value of 10.709 GHz, output amplitude is approximately 200 mV (as shown in Figure 4, where output P-P spec is shown as a minimum/guarantee of around 150 mV). Input edge rates 40 ps (20% - 80%).
24. See Figure 5. $t_{SKEW} = |t_{PLH} - t_{PHL}|$ for a nominal 50% Differential Clock Input Waveform.
25. Within-Device skew is defined as identical transitions on similar paths through a device.
26. Device-to-device skew for identical transitions at identical V_{CC} levels.
27. V_{INPP} (MAX) cannot exceed V_{CC} - V_{EE}.

Table 9. AC CHARACTERISTICS for QFN-16 V_{CC} = 0 V; V_{EE} = -3.465 V to -2.375 V or V_{CC} = 2.375 V to 3.465 V; V_{EE} = 0 V

		-40 °C			25°C			85°C			
Symbol	**Characteristic**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
f_{max}	Maximum Frequency (See Figure 4. F_{max}/JITTER) (Note 28)	10.5	12		10.5	12		10.5	12		GHz
t_{PLH}, t_{PHL}	Propagation Delay to Output Differential	90	125	160	90	125	160	90	125	160	ps
t_{SKEW}	Duty Cycle Skew (Note 29) Within-Device Skew (Note 30) Device-to-Device Skew (Note 31)		3 6 25	15 15 50		3 6 25	15 15 50		3 6 25	15 15 50	ps
t_{JITTER}	RMS Random Clock Jitter f_{in} < 10 GHz Peak-to-Peak Data Dependent Jitter f_{in} < 10 Gb/s		0.2 TBD	1		0.2 TBD	1		0.2 TBD	1	ps
V_{INPP}	Input Voltage Swing/Sensitivity (Differential Configuration) (Note 32)	75		2600	75		2600	75		2600	mV
t_r t_f	Output Rise/Fall Times Q, $\overline{Q}$ (20% - 80%) @ 1 GHz	15	30	55	20	30	55	20	30	55	ps

28. Measured using a 500 mV source, 50% duty cycle clock source. All loading with 50 Ω to V_{CC}-2.0 V. For minimum f_{max} value of 10.5 GHz, output amplitude is approximately 200 mV (as shown in Figure 4, where output P-P spec is shown as a minimum/guarantee of around 150 mV). Input edge rates 40 ps (20% - 80%).
29. See Figure 5. $t_{SKEW} = |t_{PLH} - t_{PHL}|$ for a nominal 50% Differential Clock Input Waveform.
30. Within-Device skew is defined as identical transitions on similar paths through a device.
31. Device-to-device skew for identical transitions at identical V_{CC} levels.
32. V_{INPP} (MAX) cannot exceed V_{CC} - V_{EE}.

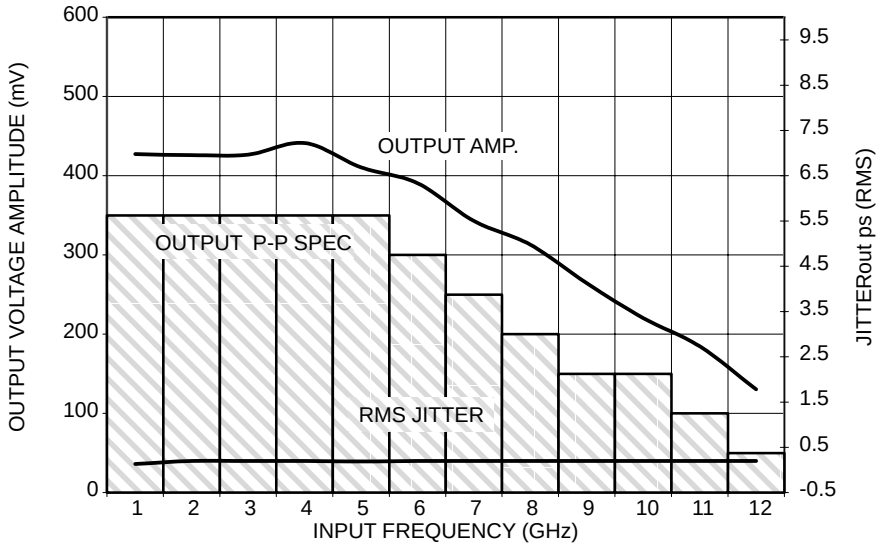


Figure 4. Output Voltage Amplitude (V_{OUTPP}) / RMS Jitter vs. Input Frequency (f_{in}) at Ambient Temperature (Typical)

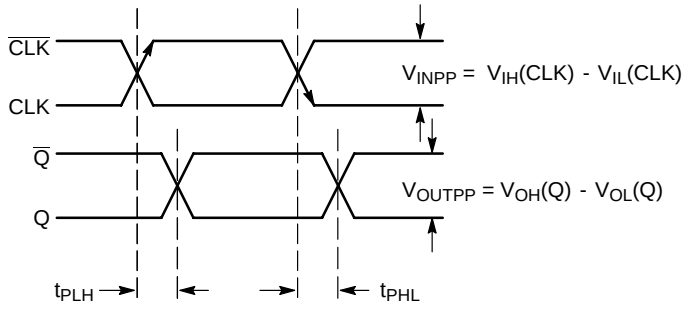


Figure 5. AC Reference Measurement

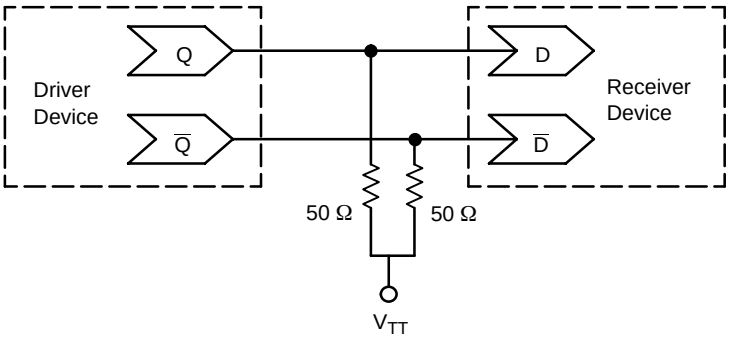
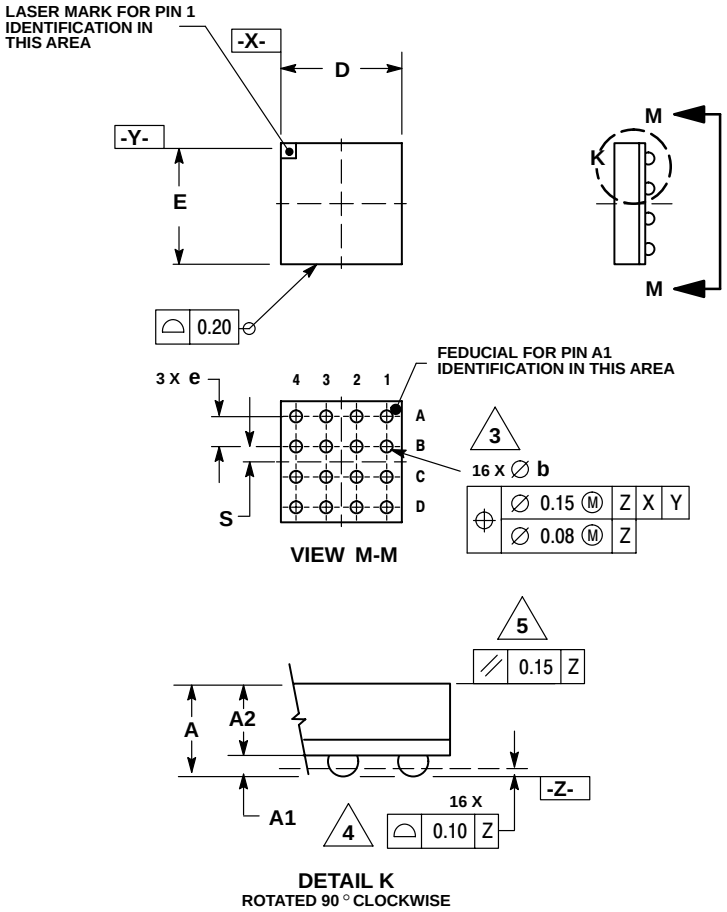


Figure 6. Typical Termination for Output Driver and Device Evaluation (Refer to Application Note AND8020 - Termination of ECL Logic Devices)

PACKAGE DIMENSIONS

FCBGA-16
BA SUFFIX
PLASTIC 4X4 (mm) BGA FLIP CHIP PACKAGE
CASE 489-01
ISSUE O



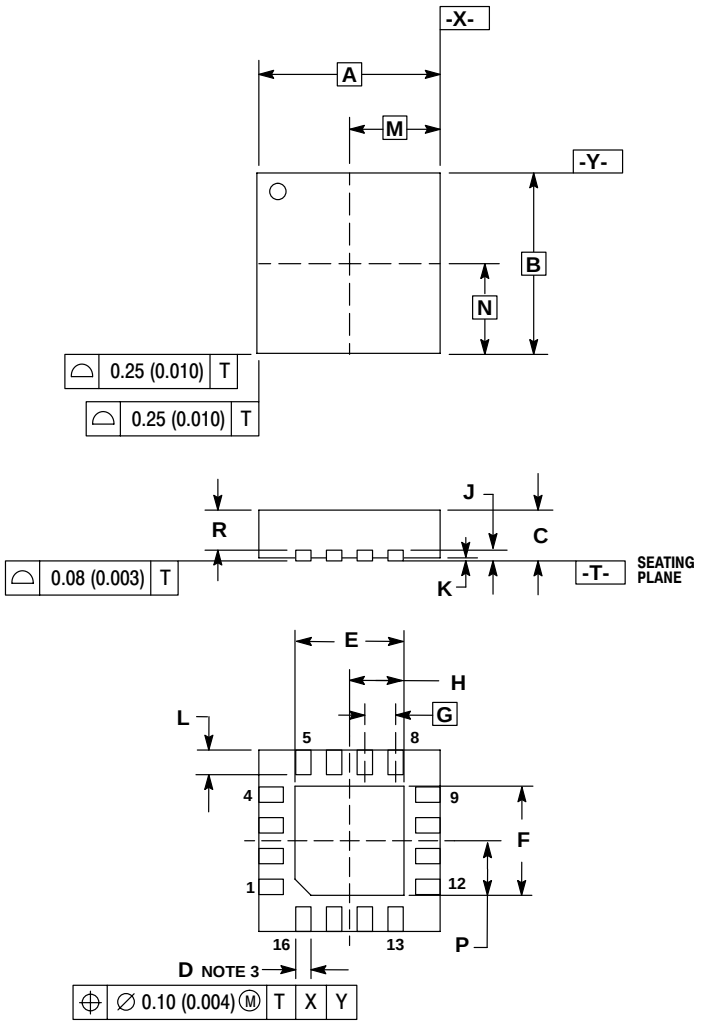
NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO DATUM PLANE Z.
4. DATUM Z (SEATING PLANE) IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
5. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.

	MILLIMETERS	
DIM	MIN	MAX
A	1.40 MAX	
A1	0.25	0.35
A2	1.20 REF	
b	0.30	0.50
D	4.00 BSC	
E	4.00 BSC	
e	1.00 BSC	
S	0.50 BSC	

NBSG11

PACKAGE DIMENSIONS

16 PIN QFN
MN SUFFIX
CASE 485G-01
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION D APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	3.00 BSC		0.118 BSC	
B	3.00 BSC		0.118 BSC	
C	0.80	1.00	0.031	0.039
D	0.23	0.28	0.009	0.011
E	1.75	1.85	0.069	0.073
F	1.75	1.85	0.069	0.073
G	0.50 BSC		0.020 BSC	
H	0.875	0.925	0.034	0.036
J	0.20 REF		0.008 REF	
K	0.00	0.05	0.000	0.002
L	0.35	0.45	0.014	0.018
M	1.50 BSC		0.059 BSC	
N	1.50 BSC		0.059 BSC	
P	0.875	0.925	0.034	0.036
R	0.60	0.80	0.024	0.031

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