



TDA7053A

LINEAR INTEGRATED CIRCUIT

STEREO BTL AUDIO OUTPUT AMPLIFIER WITH DC VOLUME CONTROL

■ DESCRIPTION

The UTC **TDA7053A** is stereo BTL output amplifiers with DC volume control and specially is designed for use in TV and monitors, but are also suitable for battery-fed portable recorders and radios.

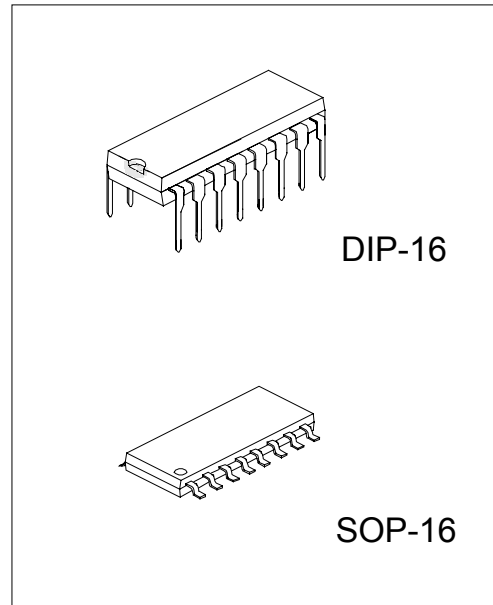
Different packages are supplied for different output power, DIP-16 for 2×1W and SOP-16 for 2×0.5W.

■ FEATURES

- * DC volume control
- * Few external components
- * Mute mode
- * Thermal protection
- * Short-circuit proof
- * No switch-on and switch-off clicks
- * Good overall stability
- * Low power consumption
- * Low HF radiation
- * ESD protected on all pins.

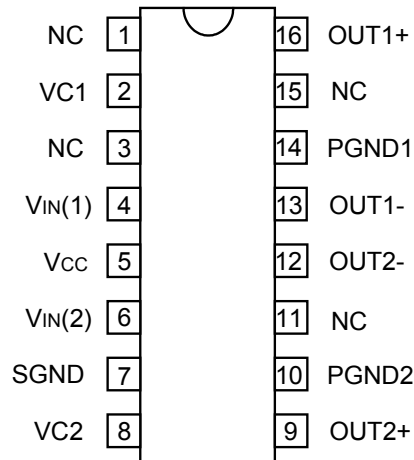
■ ORDERING INFORMATION

Order Number		Package	Packing
Normal	Lead Free Plating		
TDA7053A-D16-T	TDA7053AL-D16-T	DIP-16	Tube
TDA7053A-S16-R	TDA7053AL-S16-R	SOP-16	Tape Reel
TDA7053A-S16-T	TDA7053AL-S16-T	SOP-16	Tube



*Pb-free plating product number: TDA7053AL

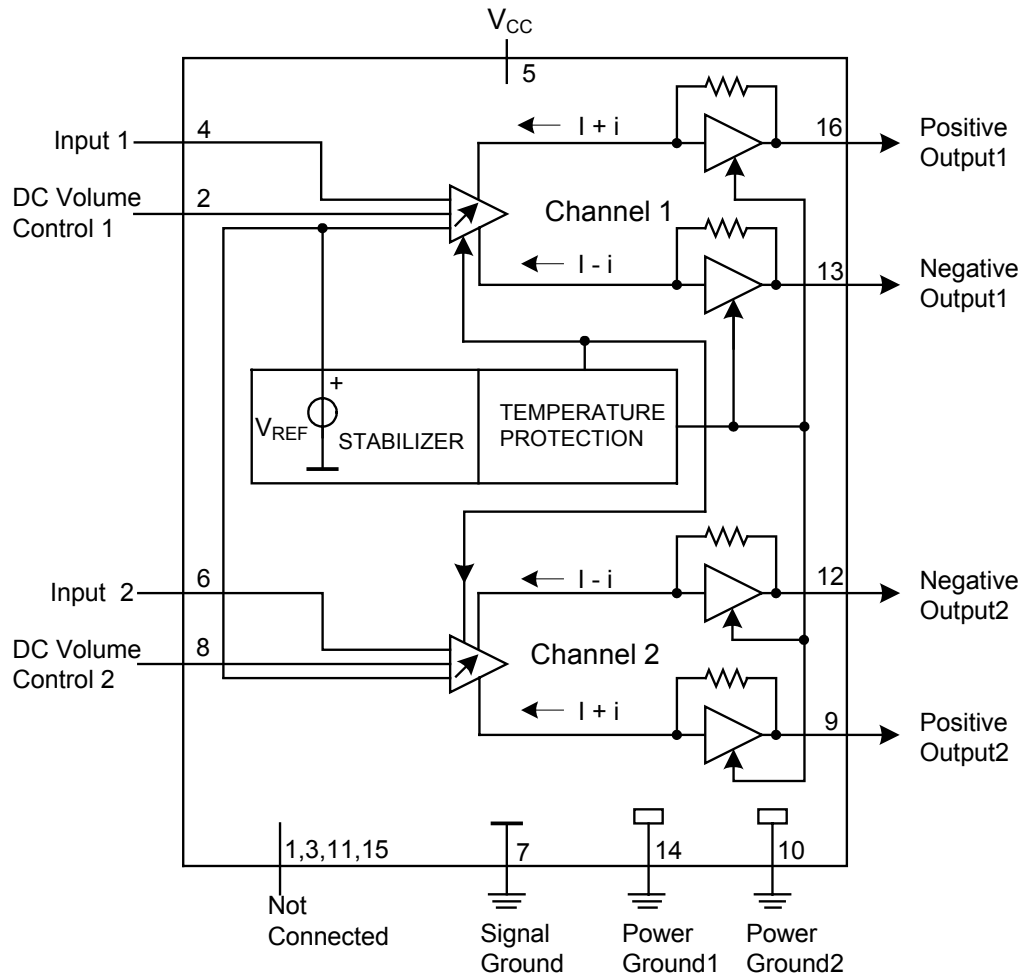
■ PIN CONFIGURATION



■ PIN DESCRIPTION

PIN NO.	SYMBOL	DESCRIPTION
1	NC	No connection
2	VC1	DC volume control 1
3	NC	No connection
4	V _{IN} (1)	Voltage input 1
5	V _{CC}	Positive supply voltage
6	V _{IN} (2)	Voltage input 2
7	SGND	Signal ground
8	VC2	DC volume control 2
9	OUT2+	Positive output 2
10	PGND2	Power ground 2
11	NC	No connection
12	OUT2-	Negative output 2
13	OUT1-	Negative output 1
14	PGND1	Power ground 1
15	NC	No connection
16	OUT1+	Positive output 1

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V_{CC}	18	V
Repetitive Peak Output Current	I_{ORM}	1.25	A
Non- Repetitive Peak Output Current	I_{OSM}	1.5	A
Total Power Dissipation ($T_a = 25^\circ C$)	DIP-16	2.5	W
	SOP-16	1.32	W
Short-Circuit Time	T_{SC}	1	hr
Input Voltage Pins 2, 4, 6 and 8	V_{IN}	5	V
Junction Temperature	T_J	+125	
Operating Ambient Temperature	T_{OPR}	-20~+85	
Storage Temperature	T_{STG}	-40~+150	

Note 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. The device is guaranteed to meet performance specification within $0^\circ C \sim +70^\circ C$ operating temperature range and assured by design from $-20^\circ C \sim +85^\circ C$.

■ THERMAL DATA

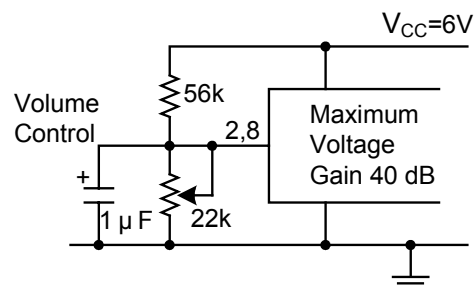
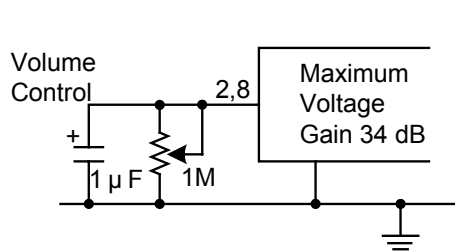
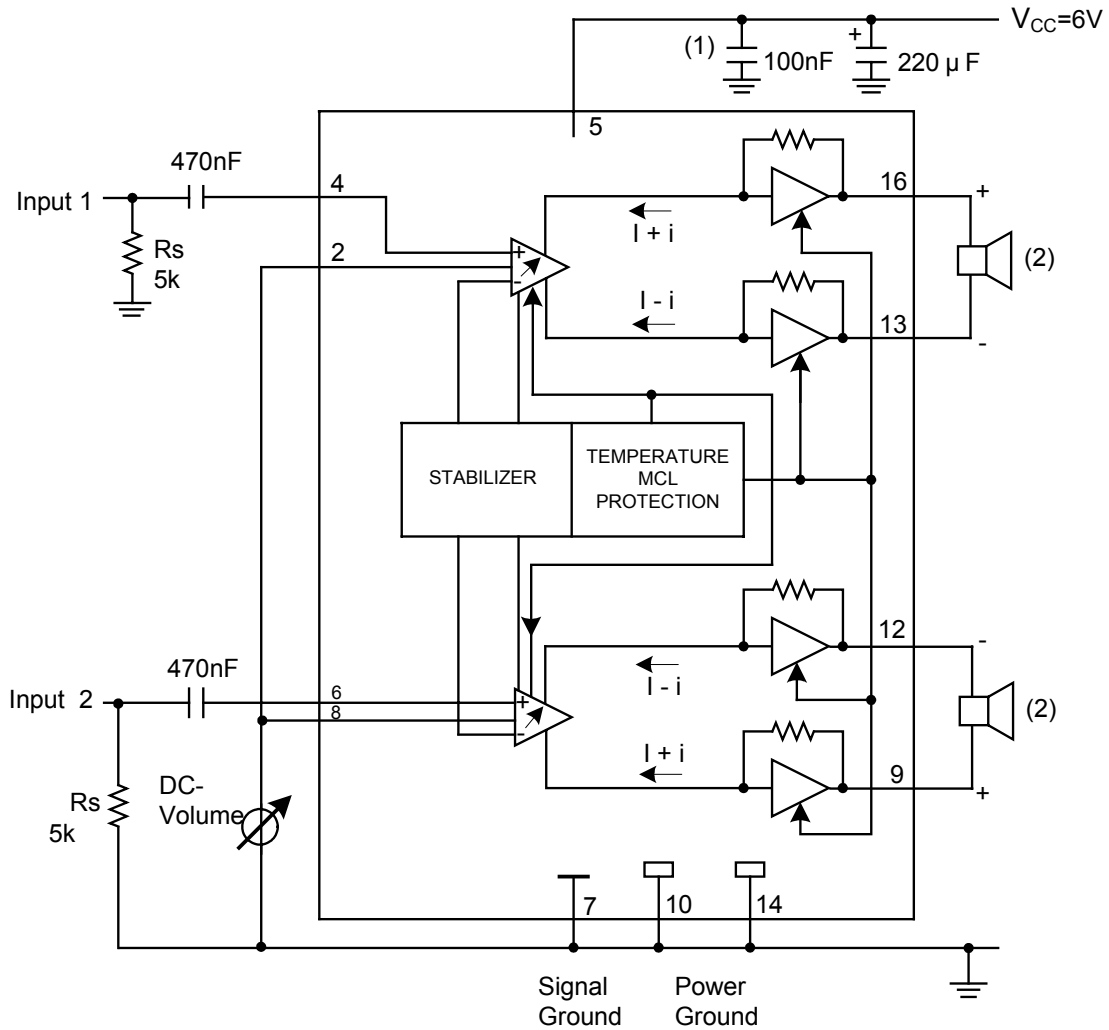
PARAMETER	SYMBOL	RATINGS	UNIT
Thermal Resistance From Junction To Ambient In Free Air	DIP-16	50	K/W
	SOP-16	95	K/W

■ ELECTRICAL CHARACTERISTICS ($V_{CC}=6V$, $T_a=25^\circ C$, $f_{IN}=1kHz$, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT	
Supply Voltage	V_{CC}		4.5		18	V	
Total Quiescent Current (Note)	I_Q	$V_{CC}=6V, R_L=\infty$		22	25	mA	
Maximum Gain: $V_{2,8} \geq 1.4 V$							
Output Power	DIP-16	P_{OUT}	THD=10%, $R_L=8\Omega$	1.0	1.1		W
	SOP-16			0.5	0.55		W
Total Harmonic Distortion	DIP-16	THD	$P_{OUT}=0.5W$		0.3	1	%
	SOP-16			$P_{OUT}=0.25W$		0.3	1
Voltage Gain	G_V		39.5	40.5	41.5	dB	
Input Signal Handling (RMS value)	$V_{IN(RMS)}$	$G_V=0dB, THD<1\%$	1			V	
Noise Output Voltage	eN	$f_{IN}=500kHz, R_S=0\Omega, BW=5kHz$		210		μV	
Bandwidth	BW	At-1dB	20Hz ~ 300kHz(TYP.)			Hz	
Supply Voltage Ripple Rejection	RR	$V_{IN(RMS)}=200mV, R_S=0\Omega, f_{IN}=100Hz\sim 10kHz$	34	38		dB	
DC Output Offset Voltage	$V_{O(OFF)}$	$ V_{16}\sim V_{13} $ and $ V_{12}\sim V_9 $		0	200	mV	
Input Impedance (pins 4 and 6)	Z_{IN}		15	20	25	k Ω	
Channel Separation	α_{CS}	$R_S=5k\Omega$	40			dB	
Channel Unbalance	$ G_V $	$V_{DC1} = V_{DC2}$			1	dB	
		$G_1=0dB, V_{DC1} = V_{DC2}$			1	dB	
Mute Position: $V_{2,8} = 0.4 V \pm 30 mV$							
Output Voltage In Mute Position	$V_{O(MUTE)}$	$V_{IN}=1.0V, R_S=5k\Omega$		30	40	μV	
DC Volume Control							
Gain Control	G_C		68.5	73.5		dB	
Volume Control Current	I_{DC}	$V_2=V_8=0V$	-20	-25	-30	μA	

Notes: With a load connected to the outputs the quiescent current will increase, the maximum value of this increase being equal to the DC output offset voltage divided by R_L .

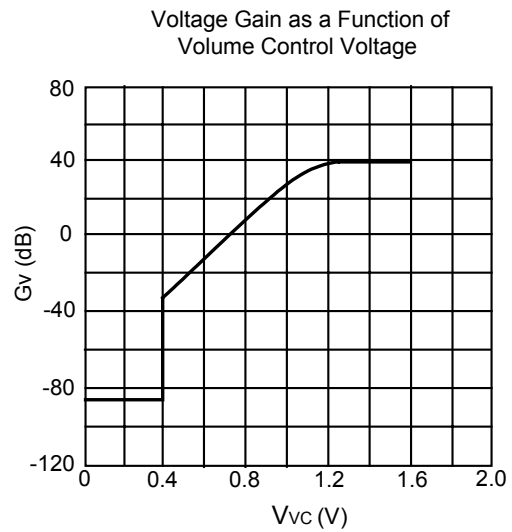
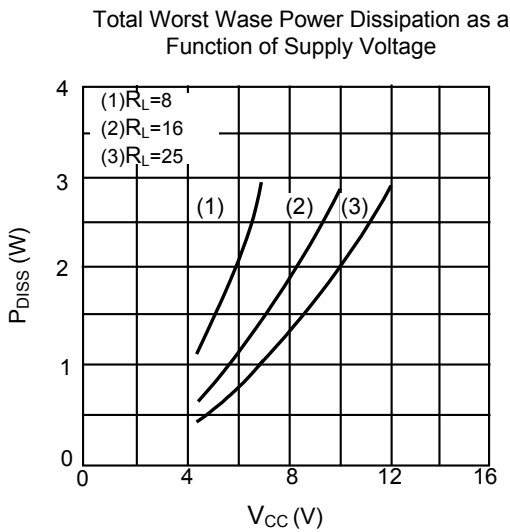
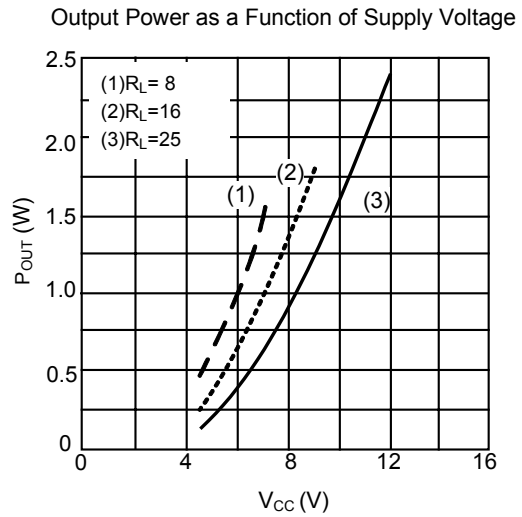
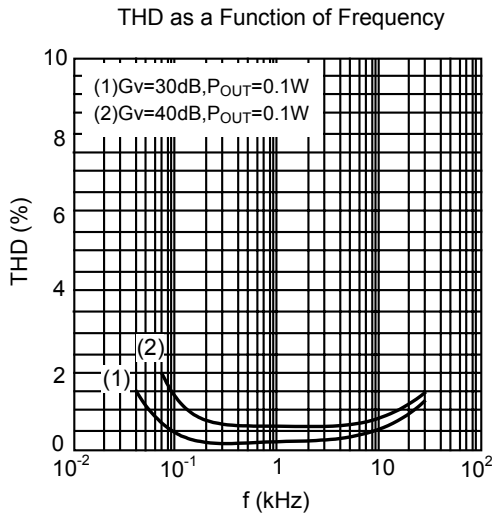
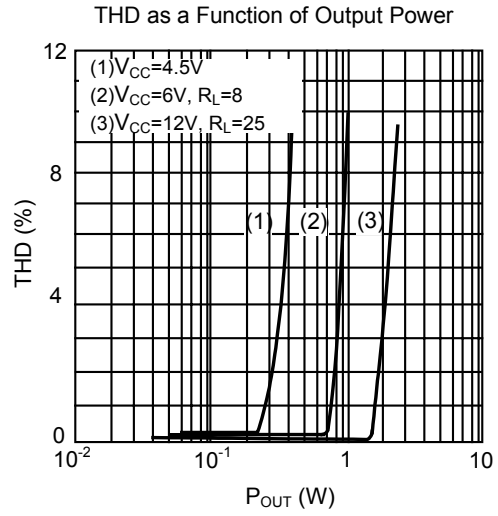
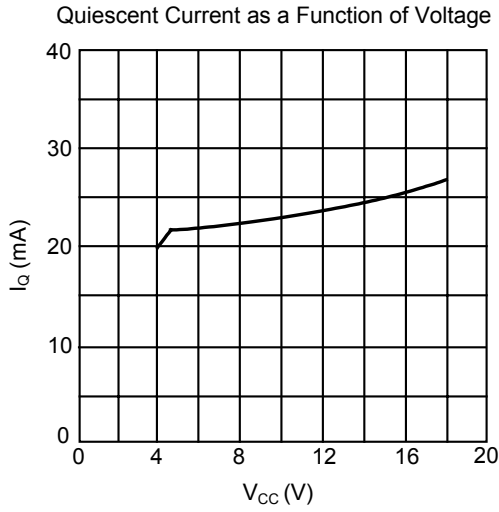
TEST AND APPLICATION DIAGRAM CIRCUITS



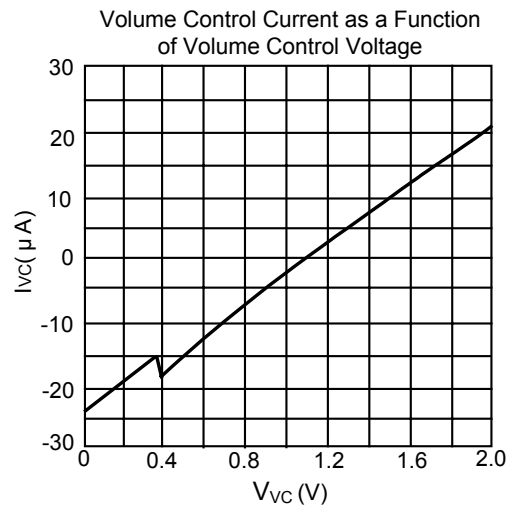
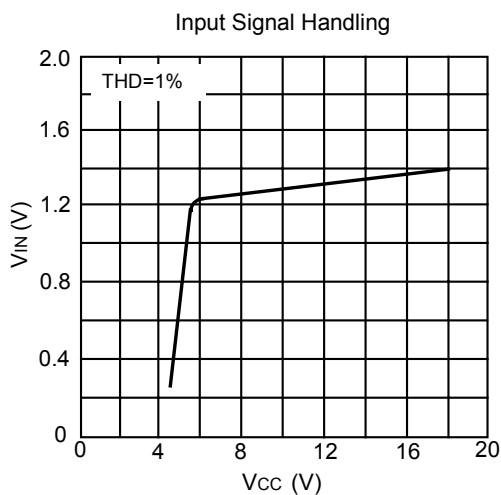
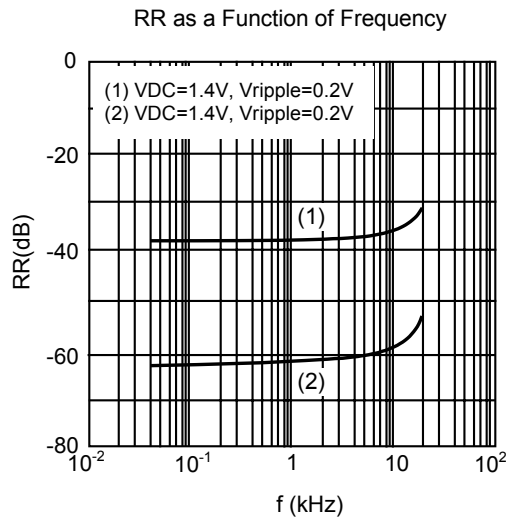
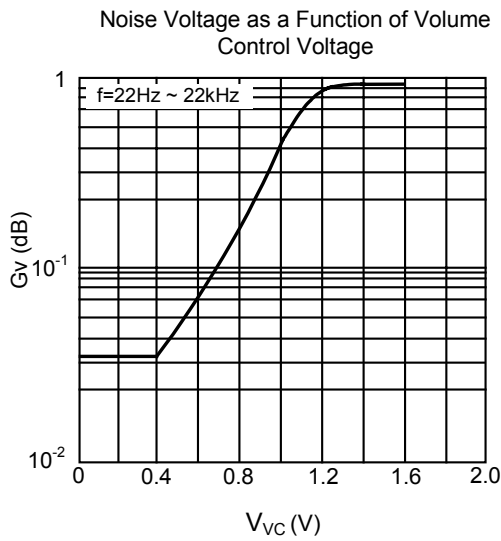
(1) This capacitor can be omitted if the 220 µ F electrolytic capacitor is connected close to pin 5.

(2) $R_L = 8$

TYPICAL CHARACTERISTICS



■ TYPICAL CHARACTERISTICS(Cont.)



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