

4-BIT SINGLE CHIP MICROCONTROLLER

The μPD17P108 is a tiny microcontroller consisting of a 1K-byte ROM, 16-word RAM, and 16 input/output ports. It is a one-time PROM version of the μPD17108, whose internal mask ROM is replaced with a one-time PROM.

Two μPD17P108 models are available: μPD17P108CS and μPD17P108GS, which allow a program to be written only once. They are suitable for evaluation of μPD17108 and for small-scale production.

The 17K architecture of the CPU uses general registers so that data memory can be manipulated directly for effective programming. Every instruction is 1 word long, consisting of 16 bits.

FEATURES

- Compatible with the μPD17108
- Program memory (one-time PROM) : 1K bytes (512 words x 16 bits)
- Data memory (RAM) : 16 words x 4 bits
- Input/output ports : 16 ports (including four N-ch open-drain outputs)
- Instruction execution time : 128 μs (62.5 kHz) to 8 μs (1 MHz)
- Number of instructions : 24 (Each instruction is 1 word long.)
- Stack level : 1
- A standby function is supported (with the STOP and HALT instructions).
- Data memory can retain data on low voltage (2.0 V at minimum).
- An oscillator is included for the system clock. (Only resistors are mounted externally.)
- Operating supply voltage : 2.5 to 6.0 V (at 250 kHz)
4.5 to 6.0 V (at 1 MHz)

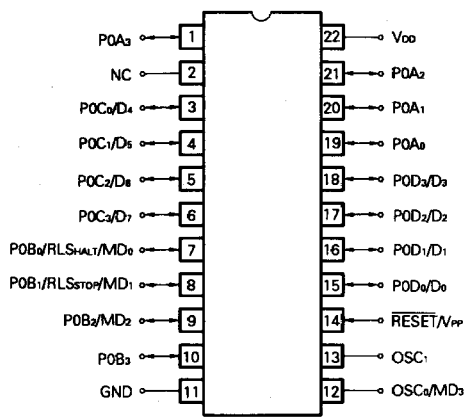
APPLICATIONS

- Controlling electric appliances or toys

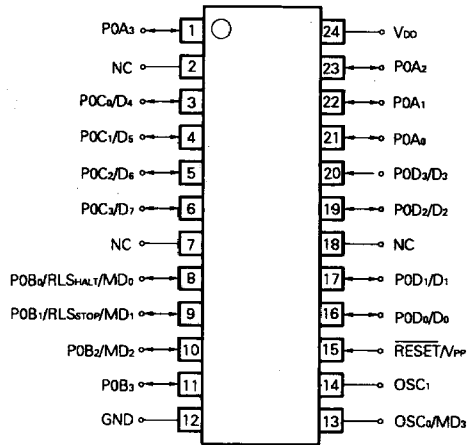
ORDERING INFORMATION

Order Code	Package
μPD17P108CS	22-pin plastic shrink DIP (300 mil)
μPD17P108GS	24-pin plastic SOP (300 mil)

PIN CONFIGURATION (Top View)

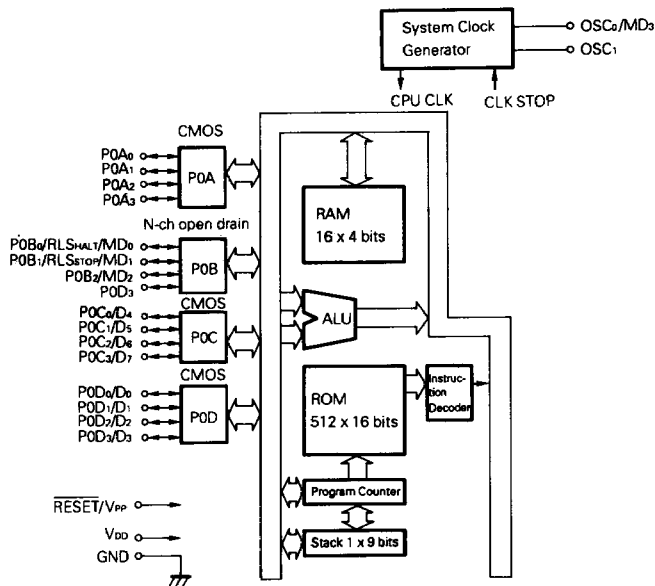


22-pin plastic shrink DIP



24-pin plastic SOP

BLOCK DIAGRAM



PIN FUNCTIONS

Pin Functions

- Port pins

Pin name	Input/output	Dual function pin		Function		When writing to program memory or verifying its contents	When reset
POA ₀	Input/output			CMOS (push-pull) 4-bit input/output port (port 0A)		Pull down	High impedance (input mode)
POA ₁							
POA ₂							
POA ₃							
POB ₀	Input/output	RLS _{HALT}	MD ₀	N-ch open-drain 4-bit input/output port (port 0B)	For the HALT mode releasing	Mode selection pin	High impedance (input mode)
POB ₁		RLS _{STOP}	MD ₁				
POB ₂		MD ₂					
POB ₃						Pull down	
POC ₀	Input/output	D ₄		CMOS (push-pull) 4-bit input/output port (port 0C)		8-bit data input/output pin (high-order 4 bits)	High impedance (input mode)
POC ₁		D ₅					
POC ₂		D ₆					
POC ₃		D ₇					
POD ₀	Input/output	D ₀		CMOS (push-pull) 4-bit input/output port (port 0D)		8-bit data input/output pin (low-order 4 bits)	High impedance (input mode)
POD ₁		D ₁					
POD ₂		D ₂					
POD ₃		D ₃					

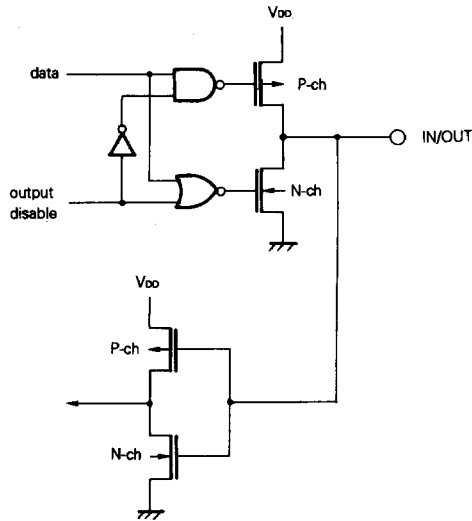
- Non-port pins

Pin name	Input/output	Dual Function pin	Function	When writing to program memory or verifying its contents
RESET	Input	V _{PP}	System reset input pin	Voltage is applied to this pin (+12.5 V)
V _{DD}			Positive power supply pin	Positive power supply pin (+6.0 V)
GND			GND pin	GND pin
OSC ₁			Pins to be connected to the system clock resonator	Program memory address update
OSC ₀		MD ₃	Pins to be connected to the system clock resonator	
NC			NC pin is not connected internally.	Mode selection pin

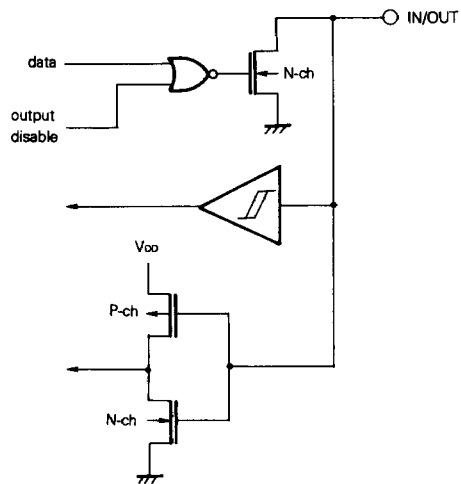
PIN INPUT/OUTPUT CIRCUITS

Following are schematics of the input/output circuits of the pins of the μPD17P108.

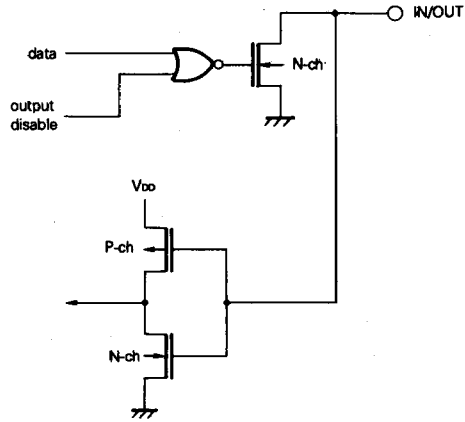
(1) P0A, P0C, and P0D



(2) P0B₀ and P0B₁

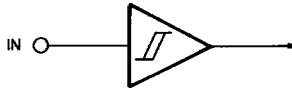


(3) P0B₂ and P0B₃



2

(4) RESET



μPD17P108

10. WRITING TO AND VERIFYING ONE-TIME PROM (PROGRAM MEMORY)

The μPD17P108's internal program memory consists of a 512 x 16 bit one-time PROM.

Writing to the one-time PROM or verifying the contents of the PROM is accomplished using the pins shown in the table below. Note that address inputs are not used; instead, the address is updated using the clock input from the OSC₁ pin.

Pin name	Function
V _{PP}	Voltage is applied to this pin when writing to program memory or verifying its contents.
OSC ₁	Input pin for address update clock used when writing to program memory or verifying its contents
MD ₀ to MD ₃	Pins that turn to input pins and are used as operation mode selection pins when writing to program memory or verifying its contents
D ₀ to D ₇	Input/output pins for 8-bit data used when writing to program memory or verifying its contents

10.1 PROGRAM MEMORY WRITE/VERIFY MODES

If +6 V is applied to the V_{DD} pin and +12.5 V is applied to the V_{PP} pin after a certain duration of reset status (V_{DD} = 5 V, $\overline{\text{RESET}} = 0$ V), the μPD17P108 enters program memory write/verify mode. A specific operating mode is then selected by setting the MD₀ through MD₃ pins as follows. Set the other unused pins to GND level by means of pull-down resistors.

Operating mode specification						Operating mode
V _{PP}	V _{DD}	MD ₀	MD ₁	MD ₂	MD ₃	
+12.5 V	+6 V	H	L	H	L	Program memory address clear mode
		L	H	H	H	Write mode
		L	L	H	H	Verify mode
		H	x	H	H	Program inhibit mode

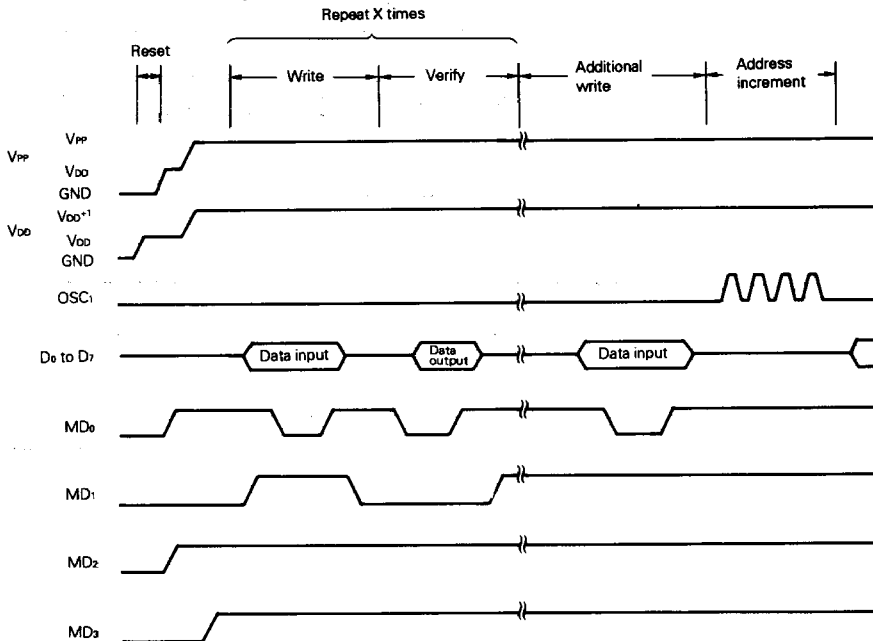
x : L (low) or H (high)

10.2 WRITING TO PROGRAM MEMORY

The procedure for writing to program memory is described below; high-speed write is possible.

- (1) Pull low the levels on all unused pins to GND by means of resistors. Bring OSC₁ to low level.
- (2) Apply 5 V to V_{DD} and bring V_{PP} to low level.
- (3) Wait 10 μs. Then apply 5 V to V_{PP}
- (4) Set the mode selection pins to program memory address clear mode.
- (5) Apply 6 V to V_{DD} and 12.5 V to V_{PP}.
- (6) Select program inhibit mode.
- (7) Write data in 1 ms write mode.
- (8) Select program inhibit mode.
- (9) Select verify mode. If the write operation is found successful, proceed to step (10). If the operation is found unsuccessful, repeat steps (7) to (9).
- (10) Perform additional write for (number of repetitions of steps (7) to (9) x 1 ms).
- (11) Select program inhibit mode.
- (12) Increment the program memory address by one on reception of four pulses on the OSC₁ pin.
- (13) Repeat steps (7) to (12) until the last address is reached.
- (14) Select program memory address clear mode.
- (15) Apply 5 V to the V_{DD} and V_{PP} pins.
- (16) Turn power off.

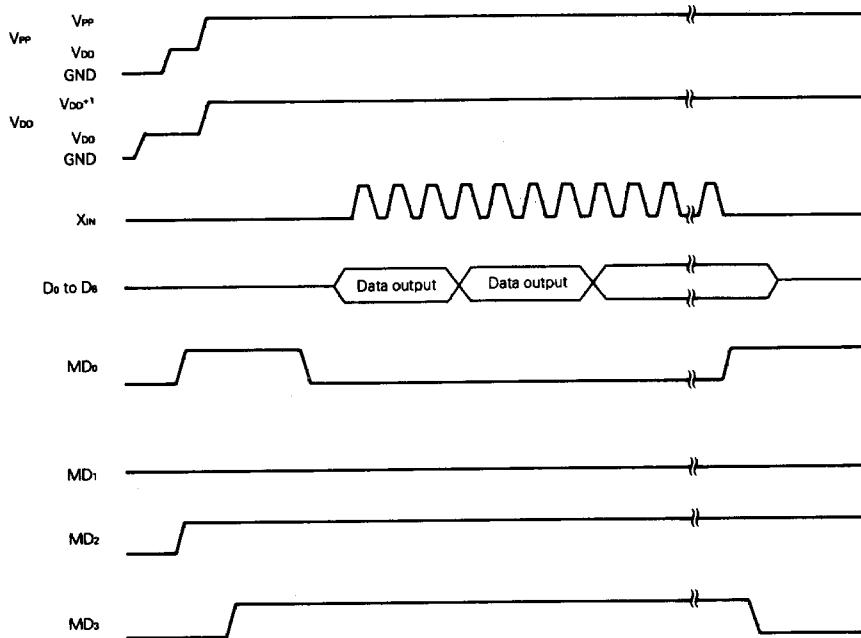
The timing for steps (2) to (12) is shown below.



10.3 READING PROGRAM MEMORY

- (1) Pull low the levels of all unused pins to GND by means of resistors. Bring OSC₁ to low level.
- (2) Apply 5 V to V_{DD} and bring V_{PP} to low level.
- (3) Wait 10 μs. Then apply 5 V to V_{PP}
- (4) Set the mode selection pins to program memory address clear mode.
- (5) Apply 6 V to V_{DD} and 12.5 V to V_{PP}
- (6) Select program inhibit mode.
- (7) Select verify mode. Data is output sequentially one address at a time for each cycle of four clock pulses on the OSC₁ pin.
- (8) Select program inhibit mode.
- (9) Select program memory address clear mode.
- (10) Apply 5 V to the V_{DD} and V_{PP} pins.
- (11) Turn power off.

The timing for steps (2) to (9) is shown below.



11. ASSEMBLER RESERVED WORDS

Table 11-1 lists the reserved words defined in the μPD17P108 device file (AS17108).

Table 11-1 Reserved Words

Name	Attribute	Value	Read/write	Description
POA0	FLG	0.70H.0	Read/write	Bit 0 of port 0A
POA1	FLG	0.70H.1	Read/write	Bit 1 of port 0A
POA2	FLG	0.70H.2	Read/write	Bit 2 of port 0A
POA3	FLG	0.70H.3	Read/write	Bit 3 of port 0A
POB0	FLG	0.71H.0	Read/write	Bit 0 of port 0B
POB1	FLG	0.71H.1	Read/write	Bit 1 of port 0B
POB2	FLG	0.71H.2	Read/write	Bit 2 of port 0B
POB3	FLG	0.71H.3	Read/write	Bit 3 of port 0B
POC0	FLG	0.72H.0	Read/write	Bit 0 of port 0C
POC1	FLG	0.72H.1	Read/write	Bit 1 of port 0C
POC2	FLG	0.72H.2	Read/write	Bit 2 of port 0C
POC3	FLG	0.72H.3	Read/write	Bit 3 of port 0C
POD0	FLG	0.73H.0	Read/write	Bit 0 of port 0D
POD1	FLG	0.73H.1	Read/write	Bit 1 of port 0D
POD2	FLG	0.73H.2	Read/write	Bit 2 of port 0D
POD3	FLG	0.73H.3	Read/write	Bit 3 of port 0D
BCD	FLG	0.7EH.0	Read/write	BCD arithmetic flag
PSW	MEM	0.7FH	Read/write	Program status word
Z	FLG	0.7FH.1	Read/write	Zero flag
CY	FLG	0.7FH.2	Read/write	Carry flag
CMP	FLG	0.7FH.3	Read/write	Compare flag

12. INSTRUCTION SET

12.1 INSTRUCTION SET LIST

b ₁₄ -b ₁₁		b ₁₅		0		1	
		BIN	HEX				
0 0 0 0	0	ADD	r, m	ADD	m, #i		
0 0 0 1	1	SUB	r, m	SUB	m, #i		
0 0 1 0	2	ADDC	r, m	ADDC	m, #i		
0 0 1 1	3	SUBC	r, m	SUBC	m, #i		
0 1 0 0	4	AND	r, m	AND	m, #i		
0 1 0 1	5	XOR	r, m	XOR	m, #i		
0 1 1 0	6	OR	r, m	OR	m, #i		
0 1 1 1	7	RET					
		RETSK					
		RORC	r				
		STOP	s				
		HALT	h				
		NOP					
1 0 0 0	8	LD	r, m	ST	m, r		
1 0 0 1	9	SKE	m, #i	SKGE	m, #i		
1 0 1 0	A						
1 0 1 1	B	SKNE	m, #i	SKLT	m, #i		
1 1 0 0	C	BR	addr	CALL	addr		
1 1 0 1	D			MOV	m, #i		
1 1 1 0	E			SKT	m, #n		
1 1 1 1	F			SKF	m, #n		

12.2 INSTRUCTIONS

Legend:

M	: One of data memory	n	: Bit position : 4 bits
m	: Data memory address specified by $[m_H, m_L]$ of each bank	addr	: One of program memory address : 11 bits
m_H	: Data memory address high (row address) : 3 bits	a_H	: Program memory address high : 3 bits
m_L	: Data memory address low (column address) : 4 bits	a_M	: Program memory address middle : 4 bits
R	: One of general register specified by $[(RP), r]$	a_L	: Program memory address low : 4 bits
r	: General register address low (column address) : 4 bits	CY	: Carry flag
RP	: General register pointer	CMP	: Compare flag
PC	: Program counter	s	: Stop release condition
SP	: Stack pointer	h	: Halt release condition
STACK	: Stack specified by (SP)	[]	: Address of M,R
i	: Immediate data : 4 bits	()	: Contents of M,R

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Type	Mnemonic	Operand	Function	Operation	Machine code			
					Op code	3 bits	4 bits	4 bits
Add	ADD	r,m	Add memory to register	$R ← (R) + (M)$	0000	m_H	m_L	r
		m,#i	Add immediate data to memory	$M ← (M) + i$	1000	m_H	m_L	i
	ADDC	r,m	Add memory to register with carry	$R ← (R) + (M) + (CY)$	00010	m_H	m_L	r
		m,#i	Add immediate data to memory with carry	$R ← (M) + i + (CY)$	10010	m_H	m_L	i
Subtract	SUB	r,m	Subtract memory from register	$R ← (R) - (M)$	00001	m_H	m_L	r
		m,#i	Subtract immediate data from memory	$M ← (M) - i$	10001	m_H	m_L	i
	SUBC	r,m	Subtract memory from register with borrow	$R ← (R) - (M) - (CY)$	00011	m_H	m_L	r
		m,#i	Subtract immediate data from memory with borrow	$M ← (M) - i - (CY)$	10011	m_H	m_L	i
Compare	SKE	m,#i	Skip if memory equal to immediate data	$M - i$, skip if zero	01001	m_H	m_L	i
	SKGE	m,#i	Skip if memory greater than or equal to immediate data	$M - i$, skip if not borrow	11001	m_H	m_L	i
	SKLT	m,#i	Skip if memory less than immediate data	$M - i$, skip if borrow	11011	m_H	m_L	i
	SKNE	m,#i	Skip if memory not equal to immediate data	$M - i$, skip if not zero	01011	m_H	m_L	i
Logical operation	AND	m,#i	Logical AND of memory and immediate data	$M ← (M) AND i$	10100	m_H	m_L	i
		r,m	Logical AND of register and memory	$R ← (R) AND (M)$	00100	m_H	m_L	r
	OR	m,#i	Logical OR of memory and immediate data	$M ← (M) OR i$	10110	m_H	m_L	i
		r,m	Logical OR of register and memory	$R ← (R) OR (M)$	00110	m_H	m_L	r
XOR	m,#i	Logical XOR of memory and immediate data	$M ← (M) XOR i$	10101	m_H	m_L	i	
	r,m	Logical XOR of register and memory	$R ← (R) XOR (M)$	00101	m_H	m_L	r	
Transfer	LD	r,m	Load memory of register	$R ← (M)$	01000	m_H	m_L	r
	ST	m,r	Store register to memory	$(M) ← R$	11000	m_H	m_L	r
	MOV	m,#i	Move immediate data to memory	$M ← i$	11101	m_H	m_L	i
Test	SKT	m,#n	Test memory bits, then skip if all bits specified are true	$CMP ← 0$ skip if $M_n = \text{all "1"}$	11110	m_H	m_L	n
	SKF	m,#n	Test memory bits, then skip if all bits specified are false	$CMP ← 0$ skip if $M_n = \text{all "0"}$	11111	m_H	m_L	n

Type	Mnemonic	Operands	Function	Operation	Machine code			
					Op code	3 bits	4 bits	4 bits
Branch	BR	addr	Jump to the address	PC←ADDR	01100	a _H	a _M	a _L
Shift	RORC	r	Rotate register right with carry	(CY)→(R)→CY	00111	000	0111	r
Subroutine	CALL	addr	Call subroutine	SP←(SP) - 1 STACK←((PC) + 1), PC←ADDR	11100	a _H	a _M	a _L
	RET		Return to main routine from subroutine	PC←(STACK), SP←(SP) + 1	00111	000	1110	0000
	RETSK		Return to main routine from subroutine, then skip unconditionary	PC←(STACK), SP←(SP) + 1 and skip	00111	001	1110	0000
Miscellaneous	STOP	s	Stop clock	STOP	00111	010	1111	s
	HALT	h	Halt the CPU, restart by condition h	HALT	00111	011	1111	h
	NOP		No operation	No Operation	00111	100	1111	0000

13. ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS (T_a = 25 °C)

Supply Voltage	V _{DD}			-0.3 to +7.0	V
Supply Voltage	V _{FP}			-0.3 to +13.5	V
Input Voltage	V _I	P0A, P0C, P0D		-0.3 to V _{DD} +0.3	V
		P0B		-0.3 to +11	V
Output Voltage	V _O	P0A, P0C, P0D		-0.3 to V _{DD} +0.3	V
		P0B		-0.3 to +11	V
High-Level output Current	I _{OH}	Each of P0A, P0B, P0C, P0D		-5	mA
		Total of all pins		-15	mA
Low-Level output Current	I _{OL}	Each of P0A, P0B, P0C, P0D		30	mA
		Total of all pins		100	mA
Operating Temperature	T _{opt}			-40 to +85	°C
Storage Temperature	T _{stg}			-65 to +150	°C
Power Consumption	P _d	T _a = 85 °C	22-pin shrink DIP	400	mW
			24-pin SOP	250	

CAPACITY (T_a = 25 °C, V_{DD} = 0 V)

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
Input Capacitance	C _{IN}			15	pF	f = 1 MHz
Input/Output Capacitance	C _{IO}			15	pF	0 V for pins other than pins to be measured

DC CHARACTERISTICS (T_a = -40 to +85 °C, V_{DD} = 2.5 to 6.0 V)

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION	
High-Level Input Voltage	V _{IH1}	0.7 V _{DD}		V _{DD}	V	Other than the following pins and port	
	V _{IH2}	0.8 V _{DD}		V _{DD}	V	P0B and RESET	
	V _{IH3}	0.8 V _{DD}		9	V	P0B (*)	
	V _{IH4}	V _{DD} - 0.5		V _{DD}	V	OSC1	
Low-Level Input Voltage	V _{IL1}	0		0.3 V _{DD}	V	Other than the following pins and port	
	V _{IL2}	0		0.2 V _{DD}	V	P0B and RESET	
	V _{IL3}	0		0.5	V	OSC1	
High-Level Output Voltage on P0A, P0C, and P0D	V _{OH}	V _{DD} - 2.0			V	V _{DD} = 4.5 to 6.0 V, I _{OH} = -2 mA	
		V _{DD} - 1.0			V	I _{OH} = -200 μA	
Low-Level Output Voltage on P0A, P0B, P0C, and P0D	V _{OL}			2.0	V	V _{DD} = 4.5 to 6.0 V, I _{OL} = 15 mA	
				0.5	V	I _{OL} = 600 μA	
High-Level Input Leakage Current on P0A to P0D	I _{LH1}			5	μA	V _{IN} = V _{DD}	
	I _{LH2}			10	μA	V _{IN} = 9 V (*)	
Low-Level Input Leakage Current on P0A to P0D	I _{LIL}			-5	μA	V _{IN} = 0 V	
High-Level Output Leakage Current on P0A to P0D	I _{LOH1}			5	μA	V _{OUT} = V _{DD}	
	I _{LOH2}			10	μA	V _{OUT} = 9 V (*)	
Low-Level Output Leakage Current on P0A to P0D	I _{LOL}			-5	μA	V _{OUT} = 0 V	
Power Supply Current	I _{DD1}		0.4	1.2	mA	Operation mode	V _{DD} = 5 V ±10%, f _{CL} = 1.0 MHz ±20%
			50	150	μA		V _{DD} = 3 V ±10%, f _{CL} = 250 kHz ±20%
	I _{DD2}		0.3	0.9	mA	HALT mode	V _{DD} = 5 V ±10%, f _{CL} = 1.0 MHz ±20%
			40	120	μA		V _{DD} = 3 V ±10%, f _{CL} = 250 kHz ±20%
	I _{DD3}		0.1	10	μA	STOP mode	V _{DD} = 5 V ±10%
			0.1	5	μA		V _{DD} = 3 V ±10%

* When N-ch open-drain input/output is selected

CHARACTERISTICS OF DATA MEMORY FOR HOLDING DATA ON LOW SUPPLY VOLTAGE IN THE STOP MODE ($T_s = -40$ to $+85$ °C)

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
Data Hold Supply Voltage	V_{DDDR}	2.0		6.0	V	
Data Hold Supply Current	I_{DDDR}		0.1	5.0	μA	$V_{DDDR} = 2.0$ V
Release Signal Set Time	t_{SREL}	0			μS	

2

AC CHARACTERISTICS ($T_s = -40$ to $+85$ °C, $V_{DD} = 2.5$ to 6.0 V)

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
Internal Clock Cycle Time	T_{CY}	6.6		160	μS	$V_{DD} = 4.5$ to 6.0 V
		26.6		160	μS	
High/Low Level Width on P0B ₀ and P0B ₁	T_{PBH} T_{PBL}	10			μS	
High/Low Level Width on RESET	T_{RSH} T_{RSL}	10			μS	

DC PROGRAMMING CHARACTERISTICS ($T_s = 25$ °C, $V_{DD} = 6.0 \pm 0.25$ V, $V_{PP} = 12.5 \pm 0.5$ V)

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
Input Voltage High	V_{IH1}	$0.7 V_{DD}$		V_{DD}	V	Except OSC ₁
	V_{IH2}	$V_{DD} - 0.5$		V_{DD}	V	OSC ₁
Input Voltage Low	V_{IL1}	0		$0.3 V_{DD}$	V	Except OSC ₁
	V_{IL2}	0		0.4	V	OSC ₁
Input Leakage Current	I_U			10	μA	$V_{IN} = V_{IL}$ or V_{IH}
Output Voltage High	V_{OH}	$V_{DD} - 1.0$			V	$I_{OH} = -1$ mA
Output Voltage Low	V_{OL}			0.4	V	$I_{OL} = 1.6$ mA
V_{DD} Power Supply Current	I_{DD}			30	mA	
V_{PP} Power Supply Current	I_{PP}			30	mA	MD0 = V_{IL} , MD1 = V_{IH}

- Notes 1. V_{PP} must be under +13.5 V including overshoot.
 2. V_{DD} must be applied before V_{PP} on and must be off after V_{PP} off.

AC PROGRAMMING CHARACTERISTICS (T_a = 25 °C, V_{DD} = 6.0 ±0.25 V, V_{PP} = 12.5 ±0.5 V)

CHARACTERISTICS	SYMBOL	(*1)	MIN.	TYP.	MAX.	UNIT	CONDITION
Address Set Up Time to MD0↓ (*2)	t _{AS}	t _{AS}	2			μS	
MD1 Setup Time to MD0↓	t _{M1S}	t _{OES}	2			μS	
Data Setup Time to MD0↓	t _{DS}	t _{DS}	2			μS	
Address Hold Time to MD0↑ (*2)	t _{AH}	t _{AH}	2			μS	
Data Hold Time to MD0↑	t _{DH}	t _{DH}	2			μS	
Data Output Float Delay Time from MD0↓→	t _{DF}	t _{DF}	0		130	ns	
V _{PP} Setup Time to MD3↑	t _{VPS}	t _{VPS}	2			μS	
V _{DD} Setup Time to MD3↑	t _{VDS}	t _{VDS}	2			μS	
Initial Program Pulse Width	t _{PW}	t _{PW}	0.95	1.0	1.05	ms	
Additional Program Pulse Width	t _{OPW}	t _{OPW}	0.95		21.0	ms	
MD0 Setup Time to MD1↑	t _{M0S}	t _{CS}	2			μS	
Data Output Delay Time from MD0↓→	t _{DOV}	t _{DOV}			1	μS	
MD1 Hold Time to MD0↑	t _{M1H}	t _{OEH}	2			μS	MD0 = MD1 = V _{IL}
MD1 Recovery Time to MD0↓	t _{M1R}	t _{OR}	2			μS	
Program Counter Reset Time	t _{PCR}	-	10			μS	t _{M1H} = t _{M1R} ≥ 50 μS
OSC ₁ Input High, Low Level Range	t _{OH} t _{OL}	-	0.42			μS	
OSC ₁ Input Frequency	f _{OSC}				1.2	MHz	
Initial Mode Set Time	t _i	-	2			μS	
MD3 Setup Time to MD1↑	t _{M3S}	-	2			μS	
MD3 Hold Time to MD1↓	t _{M3H}	-	2			μS	
MD3 Setup Time to MD0↓	t _{M3SR}	-	2			μS	Read program memory
Data Output Delay Time From Address (*2)	t _{OAD}	-	2			μS	Read program memory
Data Output Hold Time From Address (*2)	t _{OAH}	t _{ACC}	0		130	ns	Read program memory
MD3 Hold Time to MD0↑	t _{M3HR}	t _{OH}	2			μS	Read program memory
Data Output float Delay Time From MD3↓→	t _{OFR}	-	2			μS	Read program memory
Reset Setup Time	t _{RES}	-	10			μS	

*1 Symbols for corresponding μPD27C256.

*2 Internal address signal is incremented by one at the falling edge of the third OSC₁ input, and it is not connected to the pin.

Write program memory timing

