Zero Drift, Digital Programmable Instrumentation Amplifier

Preliminary Data Sheet

AD8231

FEATURES

Digitally programmable gain
- **G= 1, 2, 4, 8, 16, 32, 64, 128**
- **Software or pin programmable**

Excellent temperature performance
- **Specified from −40°C to +125°C**
- **50 nV/°C max input offset drift**
- **10 ppm/°C max gain drift**

Excellent dc performance
- **122 dB min CMR, G = 128**
- **25 µV max input offset voltage**
- **100 pA max bias current**
- **0.7 uV p-p (0.1 Hz to 10 Hz)**

Good ac performance
- **Gain Bandwidth Product 1 MHz**
- **Slew Rate 0.7 V/µs**

Rail-to-rail input and output
Shutdown/Multiplex
Additional uncommitted op amp
Supply range: 3.0V to 5.5V

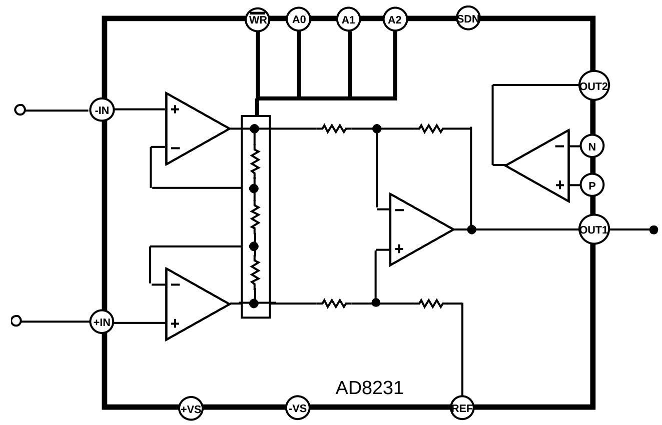


Figure 1. AD8231 Functional Diagram

APPLICATIONS

Pressure and Strain Transducers
Thermocouples and RTDs
Programmable Instrumentation
Industrial Controls
Weigh Scales

GENERAL DESCRIPTION

The AD8231 is a low drift, rail to rail, instrumentation amplifier with software programmable gains of 1, 2, 4, 8, 16, 32, 64 or 128. The gains are programmed via digital logic or pin strapping.

The AD8231 is ideal for applications that require precision performance over a wide temperature range, such as industrial temperature sensing and data logging. Because the gain setting resistors are internal, maximum gain drift is only 10 ppm/°C. Because of the autozero input stage, maximum input offset is 25 uV and maximum input offset drift is just 50 nV/°C. CMRR is also guaranteed over temperature: 80 dB for G=1, increasing to 122 dB at a gain of 128. Voltage noise is just 0.7 uV p-p (0.01 Hz to 10 Hz).

The AD8231 also includes an uncommitted op amp which can be used for additional gain, differential signal driving or filtering. Like the in amp, the op amp has an autozero architecture, rail to rail input, and rail to rail output.

The AD8231 includes a shutdown feature that reduces current to 1 uA and makes the amplifier output high impedance. This allows easy multiplexing of multiple amplifiers without additional switches.

The AD8231 is specified over the extended industrial temperature range of -40°C to +125°C. It is available in a 4mm x 4mm 16-Lead LFCSP (Chip Scale) package.

Rev. PrC

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 **www.analog.com**
Fax: 781.326.8703

SPECIFICATIONS

Table 1. V_S = 5 V, V_{REF} = 2.5 V, G=1, R_L = 10 kΩ, -40°C ≤T_A ≤ +125°C unless otherwise noted).

Parameter	Conditions	Min	Typ	Max	Unit
INSTRUMENTATION AMPLIFIER					
OFFSET VOLTAGE	VOS RTI = V_{OSI} + V_{OSO}/G				
Input Offset, V_{OSI}			5	25	µV
Average Temperature Drift			0.01	0.05	µV/°C
Output Offset, V_{OSO}			15	50	µV
Average Temperature Drift			0.02	0.1	µV/°C
INPUT CURRENTS					
Input Bias Current	T_A = 25°C		200	400	pA
				1	nA
Input Offset Current	T_A = 25°C		50	100	pA
				0.5	nA
GAINS	1, 2, 4, 8, 16, 32, 64, 128				
Gain Error					
G = 1			0.1	0.3	%
G = 2 to 128			1	TBD	%
Gain Drift					
G = 1			2	10	ppm/°C
G = 2 to 128			2	10	ppm/°C
Gain Nonlinearity	V_{OUT} = 0.1 to 4.9V				
G= 1			5		ppm
G= 8			TBD		ppm
G= 128			TBD		ppm
CMRR					
G=1		80	100		dB
G=2		86	106		dB
G=4		92	112		dB
G=8		98	118		dB
G=16		104	124		dB
G=32		110	130		dB
G=64		116	136		dB
G=128		122	142		dB
NOISE	Noise RTI = sqrt(eni^2 + (eno/G)^2				
	V_{IN+}, V_{IN-} =2.5V ; T_A = 25°C				
Input Voltage Noise, eni	f = 1 kHz,		32		nV/√Hz
	f = 0.1 Hz to 10 Hz		0.7		µV p-p
	f = 0.01 Hz to 1 Hz		0.2		µV p-p
Output Voltage Noise, eno	f = 1 kHz		60		nV/√Hz
	f = 0.1 Hz to 10 Hz		1		µV p-p
	f = 0.01 Hz to 1 Hz		0.5		µV p-p
OTHER INPUT CHARACTERISTICS					
Differential Input Impedance	Common Mode		10‖5		GΩ‖pF
Common Mode Input Impedance	Differential		10‖5		GΩ‖pF
Power Supply Rejection Ratio		100	110		dB
Input Operating Voltage Range		0.05		4.95	V
REFERENCE INPUT					
Input Impedance			10‖10		GΩ‖pF
Voltage Range		0.05		4.95	V

DYNAMIC PERFORMANCE					
Gain Bandwidth Product			1		MHz
Slew Rate			0.6		V/µs
OUTPUT CHARACTERISTICS					
Output Voltage High	R_L = 100kΩ to ground	4.9	4.94		V
	R_L = 10kΩ to ground	4.8	4.88		V
Output Voltage Low	R_L = 100kΩ to 5V		60	100	mV
	R_L = 10kΩ to 5V		80	200	mV
Short-Circuit Current		10	20		mA
DIGITAL INTERFACE					
Input Voltage Low				1.0	V
Input Voltage High		4.0			V
Leakage Current				TBD	nA
Setup Time : t_{DS}		TBD			ns
Hold Time: t_{DH}		TBD			ns
Write Width: t_{CS}		TBD			ns
Gain switching time			TBD		ns
OPERATIONAL AMPLIFIER					
INPUT CHARACTERISTICS					
Offset Voltage, V_{OS}			10	30	µV
Temperature Drift			0.01	0.05	uV/°C
Input Bias Current	T_A = 25°C		200	400	pA
				1	nA
Input Offset Current	T_A = 25°C		50	100	pA
				0.5	nA
Input Voltage Range		0.05		4.95	V
Open Loop Gain		TBD			V/mV
Common-Mode Rejection Ratio		100	110		dB
Power Supply Rejection Ratio		100	110		dB
Voltage Noise Density			17	TBD	nV/√Hz
Voltage Noise	f = 0.1 Hz to 10 Hz		0.4	TBD	µV p-p
DYNAMIC PERFORMANCE					
Gain Bandwidth Product			1		MHz
Slew Rate			0.6		V/µs
OUTPUT CHARACTERISTICS					
Output Voltage High	R_L = 100kΩ to ground	4.9	4.96		V
	R_L = 10kΩ to ground	4.8	4.92		V
Output Voltage Low	R_L = 100kΩ to 5V		60	100	mV
	R_L = 10kΩ to 5V		80	200	mV
Short-Circuit Current		10	20		mA
BOTH AMPLIFIERS					
POWER SUPPLY					
Quiescent Current			3.5	4.5	mA
Quiescent Current (Shutdown)			1	10	uA
SHD high to high output impedance			TBD		ns
SHD low to low output impedance			TBD		ns
Shutdown output impedance			TBD		GΩ||pF

Table 2. V_S = 3.3 V, V_{REF} = 1.65 V, -40°C ≤T_A ≤ +125°C, G=1, R_L = 10 kΩ, unless otherwise noted).

Parameter	Conditions	Min	Typ	Max	Unit
INSTRUMENTATION AMPLIFIER					
OFFSET VOLTAGE	VOS RTI = V_{OSI} + V_{OSO}/G				
Input Offset, V_{OSI}			5	25	µV
Average Temperature Drift			0.01	0.05	nV/°C
Output Offset, V_{OSO}			15	50	µV
Average Temperature Drift			0.02	0.1	µV/°C
INPUT CURRENTS					
Input Bias Current	T_A = 25°C		200	400	pA
				1	nA
Input Offset Current	T_A = 25°C		5	100	pA
				0.5	nA
GAINS	1, 2, 4, 8, 16, 32, 64, 128				
Gain Error					
G= 1			0.1	0.3	%
G= 2 to 128			1	TBD	%
Gain Drift					
G= 1			2	10	ppm/°C
G= 2 to 128			2	10	
Gain Nonlinearity	0.1 to 3.2V				
G= 1			TBD		ppm
G= 8			TBD		ppm
G= 128			TBD		ppm
CMRR					
G=1		80	100		dB
G=2		86	106		dB
G=4		92	112		dB
G=8		98	118		dB
G=16		104	124		dB
G=32		110	130		dB
G=64		116	136		dB
G=128		122	142		dB
NOISE	Noise RTI = sqrt(eni^2 + $(eno/G)^2$				
	V_{IN+}, V_{IN-} =2.5V; T_A = 25°C				
Input Voltage Noise, eni	f = 1 kHz		45		nV/√Hz
	f = 0.1 Hz to 10 Hz		0.7		µV p-p
	f = 0.01 Hz to 1 Hz		0.2		µV p-p
Output Voltage Noise, eno	f = 1 kHz		60		nV/√Hz
	f = 0.1 Hz to 10 Hz		1		µV p-p
	f = 0.01 Hz to 1 Hz		0.5		µV p-p
OTHER INPUT CHARACTERISTICS					
Differential Input Impedance	Common Mode		10||5		GΩ||pF
Common Mode Input Impedance	Differential		10||5		GΩ||pF
Power Supply Rejection Ratio		100	110		dB
Input Operating Voltage Range		0.05		3.25	V
REFERENCE INPUT					
Input Impedance			10||10		GΩ||pF
Voltage Range		0.05		3.25	V

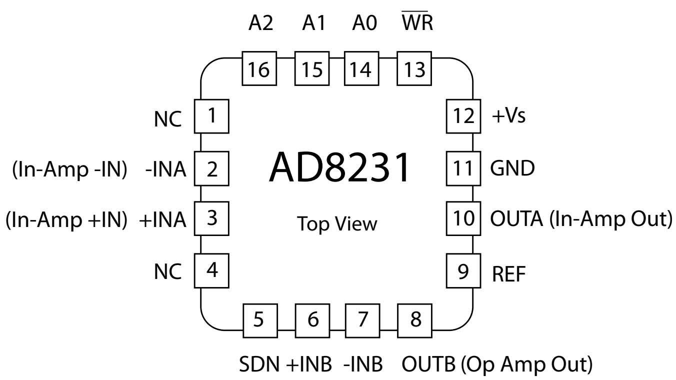
DYNAMIC PERFORMANCE					
Gain Bandwidth Product			1		MHz
Slew Rate			0.6		V/µs
OUTPUT CHARACTERISTICS					
Output Voltage High	R_L = 100kΩ to ground	3.2	3.24		V
	R_L = 10kΩ to ground	3.1	3.18		V
Output Voltage Low	R_L = 100kΩ to 3.3V		60	100	mV
	R_L = 10kΩ to 3.3V		80	200	mV
Short-Circuit Current		10	20		mA
DIGITAL INTERFACE					
Input Voltage Low				0.7	V
Input Voltage High		2.0			V
Leakage Current				TBD	nA
Setup Time : t_{DS}		TBD			ns
Hold Time: t_{DH}		TBD			ns
Write Width: t_{CS}		TBD			ns
Gain switching time			TBD		ns
OPERATIONAL AMPLIFIER					
INPUT CHARACTERISTICS					
Offset Voltage, V_{OS}			10	30	µV
Temperature Drift			0.01	0.05	uV/°C
Input Bias Current	T_A = 25°C		200	400	pA
				1	nA
Input Offset Current	T_A = 25°C		50	100	pA
				0.5	nA
Input Voltage Range		0.05		3.25	V
Open Loop Gain		TBD			V/mV
Common-Mode Rejection Ratio		100	110		dB
Power Supply Rejection Ratio		100	110		dB
Voltage Noise Density			25	TBD	nV/√Hz
Voltage Noise	f = 0.1 Hz to 10 Hz		0.4	TBD	µV p-p
DYNAMIC PERFORMANCE					
Gain Bandwidth Product			1		MHz
Slew Rate			0.6		V/µs
OUTPUT CHARACTERISTICS					
Output Voltage High	R_L = 100kΩ to ground	3.2	3.26		V
	R_L = 10kΩ to ground	3.1	3.12		V
Output Voltage Low	R_L = 100kΩ to 3.3V		60	100	mV
	R_L = 10kΩ to 3.3V		80	200	mV
Short-Circuit Current		10	20		mA
BOTH AMPLIFIERS					
POWER SUPPLY					
Quiescent Current			3	4	mA
Quiescent Current (Shutdown)			1	10	uA
SHD high to high output impedance			TBD		ns
SHD low to low output impedance			TBD		ns
Shutdown output impedance			TBD		GΩ||pF

ABSOLUTE MAXIMUM RATINGS

Table 2. AD8231 Absolute Maximum Ratings

Parameter	Rating
Supply Voltage	
Internal Power Dissipation	
Output Short Circuit Current	
Input Voltage (Common-Mode)	
Differential Input Voltage	
Storage Temperature	−65°C to +150°C
Operational Temperature Range	−40°C to +125°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions may affect device reliability.



16-Lead LFCSP (Chip Scale) Package

Pin Number	Mnemonic	Function	Pin Number	Mnemonic	Function
1	NC	No connect	9	REF	Reference Pin to set the Output Level
2	-INA	Negative Input for In-amp	10	OUTA	Output for In Amp
3	+INA	Positive Input for In-amp	11	GND	Power Supply Ground
4	NC	No connect	12	+Vs	Positive Power Supply
5	$\overline{\text{SDN}}$	Shut Down	13	$\overline{\text{WR}}$	Write Enable to latch gain setting
6	+INB	Positive Input for Undedicated Op Amp	14	A0	Gain Setting Bit
7	-INB	Negative Input for Undedicated Op Amp	15	A1	Gain Setting Bit
8	OUTB	Output for Undedicated Op Amp	16	A2	Gain Setting Bit

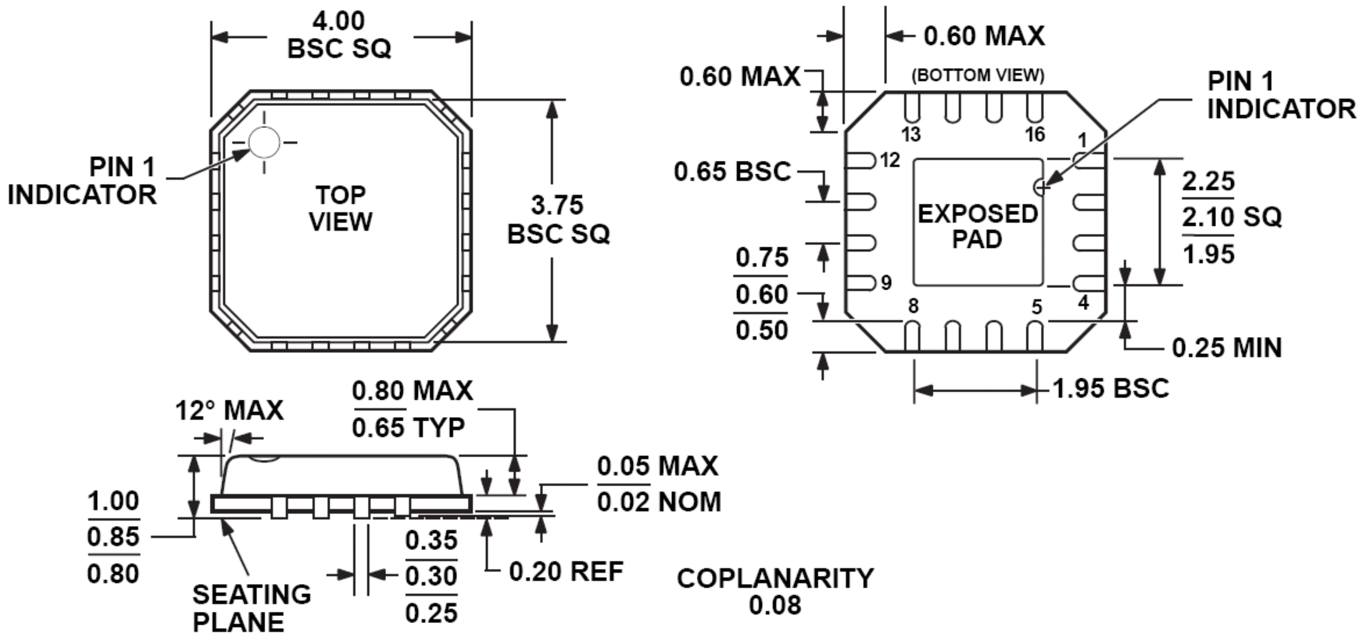
GAIN SELECTION

The AD8231's gain is set by voltages applied to the A0, A1, and A2 pins. High (HI) or low (LO) voltage limits are listed in the specifications section. To change the gain, the $\overline{WR}$ pin must be driven low. When the $\overline{WR}$ pin is driven high, the gain is latched, and voltages at the A0-A2 pins will have no effect. Table 3 is the truth table showing the different gain settings.

$\overline{WR}$	A2	A1	A0	Gain
LO	LO	LO	LO	1
LO	LO	LO	HI	2
LO	LO	HI	LO	4
LO	LO	HI	HI	8
LO	HI	LO	LO	16
LO	HI	LO	HI	32
LO	HI	HI	LO	64
LO	HI	HI	HI	128
HI	X	X	X	No change

Table 3 Truth table for AD8231's gain settings

16-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
4 x 4 mm Body, Very Thin Quad
(CP-16-4)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-220-VGGC

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

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