Ordering number: EN5177

Monolithic Linear IC

LA7583

IF Signal Processing Circuit (A^{2}C PLL VIF + SIF) for TVs and VCRs

Overview

The LA7583 is a VIF + SIF IC that requires no adjustments. In order to eliminate the need for adjustments in the VIF block, a multi-network PLL has been developed and adopted for video detection. In the SIF block, adjustments were eliminated by using gyrator technology in the FM quadrature detector. In addition to eliminating the need for adjustments, a buzz canceller that suppresses Nyquist buzz has been built into the LA7583 in order to provide excellent sound quality.

Features

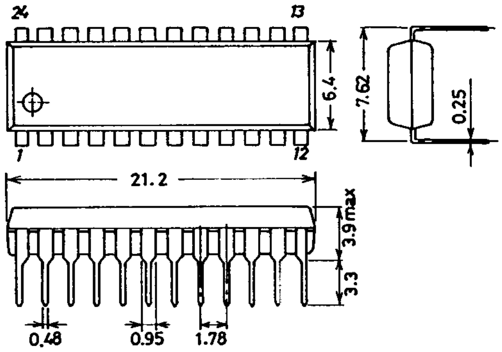
- Elimination of VCO, AFT, and SIF coils eliminates the need for adjustments.
- A variety of built-in filters.
- Built-in buzz canceller results in excellent audio characteristics.

Note: A^{2}C Automatic Adjustment Control
AQT Automatic Quadrature Tuning

Package Dimensions

unit : mm

3067-DIP24S



Functions

[VIF]
- VIF amplifier
- Equalizer amplifier
- AGC lag lead filter
- Multinetwork PLL
- AFT
- Video driver
- BNC
- IFAGC
- FAGC
- Buzz canceller

[1st SIF]
- Preamplifier
- 1st SIF detector
- AGC detector
- Built-in AGC filter

[SIF]
- Limiter amplifier
- AQT detector (gyrator)
- J/U switch

[mute]
- Audio mute
- AV mute

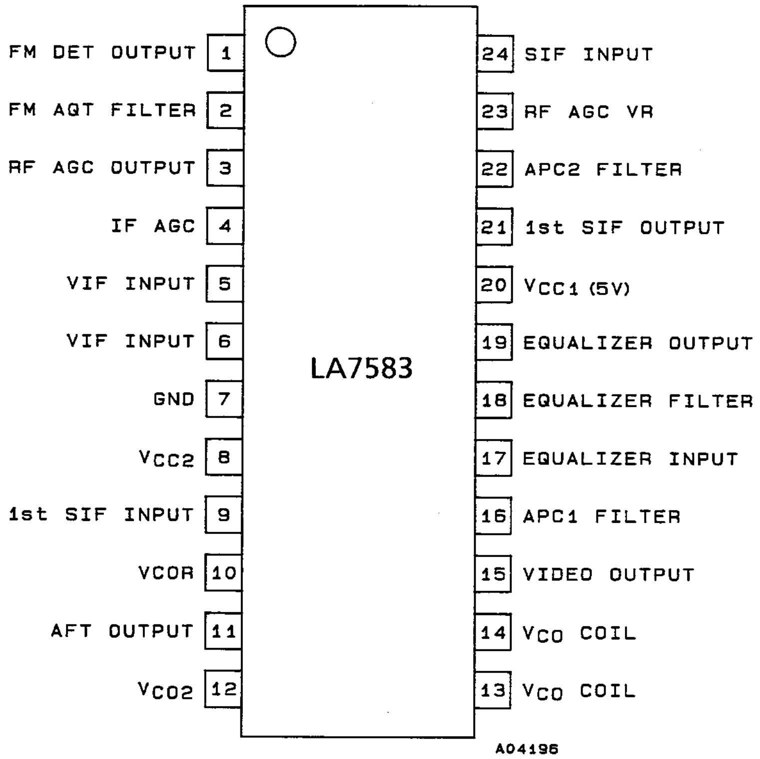
Specifications

Maximum Ratings at Ta = 25 °C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{CC} 1		7	V
	V_{CC} 2		13.2	V
Circuit voltage	V4		V_{CC} 1	V
	V3, V11		V_{CC} 2	V
Circuit current	I1, I10, I23		–1	mA
	I3, I21		–3	mA
	I15, I19		–5	mA
Allowable power dissipation	Pd max	$T_a \leqq 50$ °C	1000	mW
Operating temperature	Topr		–20 to +70	°C
Storage temperature	Tstg		–55 to +150	°C

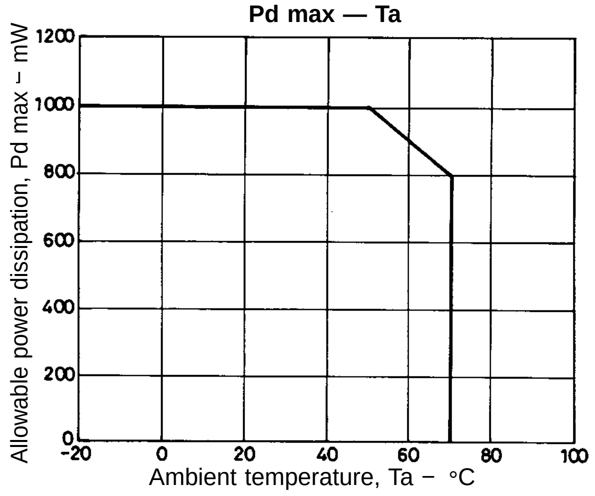
* A^2C (Automatic Adjustment Control)
Note: Current flowing into the IC is positive (no signal) and current flowing out is negative.

Pin Assignment



Top View

Pd max — Ta



Operating Conditions at Ta = 25 °C

Parameter	Symbol	Conditions	Ratings	Unit
Recommended supply voltage	$V_{CC}1$		5	V
	$V_{CC}2$		9	V
Operating supply voltage range	$V_{CC}1$		4.6 to 6	V
	$V_{CC}2$		7 to 12	V

Electrical Characteristics at Ta = 25 °C, $V_{CC}1$ = 5 V, $V_{CC}2$ = 9 V, fp = 45.75 MHz

Parameter	Symbol	Conditions	min	typ	max	Unit
[VIF Block]						
Circuit current 1	I20	V_{CC} = 5 V	57	66	78	mA
Circuit current 2	I8	V_{CC} = 9 V	7.8	11.0	14.0	mA
Maxinum RF AGC voltage	V3H	V4 = 3 V	7.5	8.1	9	V
Mininum RF AGC voltage	V3L	V4 = 1.5 V		0	+0.5	V
Input sensitivity	Vi	S1 = OFF	32	38	44	dBµ
AGC range	G_R		56	62		dB
Maxinum Allowable Input	Vi max		95	103		dBµ
Video output voltage with no signal	V19	V4 = 2 V	3.3	3.6	3.9	V
Sync signal tip voltage	V19(tip)	Vi = 10 mV	1.1	1.4	1.7	V
Video output amplitude	$V_O(V)$	87.5% mod	1.7	2.0	2.3	Vp-p
Black noise threshold level voltage	V_{BTH}		0.4	0.7	1.1	V
Black noise clamp voltage	V_{BCL}		1.65	1.95	2.25	V
Output S/N	S/N		48	52		dB
920 kHz beat level	I920	P = 0, C = –10 dB, S = –10 dB	41	45		dB
Frequency characteristics	f_C	P = 0, S = –14 dB	6	8		MHz
Differential gain	DG	Vi = 10 mV, 87.5%		3	8	%
Differential phase	DP	10STAR STEP		3	8	rad
AFT output voltage with no signal	V11		0.3	4.5	8.7	V
Maxinum AFT output voltage	V11H		7.5	8.5	9	V
Mininum AFT output voltage	V11L		0	+1	+1.5	V
AFT detection sensitivity	Sf		33	48	69	mV/kHz
VIF input resistance	Ri(VIF)	f = 45.75 MHz	0.8	1.1	1.5	kΩ
VIF input capacity	Ci(VIF)	f = 45.75 MHz	2	3	5	pF
APC pull-in range (U)	f_{PU}		1.0	3		MHz
APC pull-in range (L)	f_{PL}			–4.5	–1.0	MHz
AFT crossover frequency	Δf_A		–65		+65	kHz
VCO1 maximum variable range	Δf_U1	V22 = 4 V	2.0	5.0		MHz
	Δf_L1	V22 = 2 V		–5.0	–2.0	MHz
VCO2 maximum variable range	Δf_U2	V16 = 4 V	100	200		kHz
	Δf_L2	V16 = 2 V		–1000	–200	kHz
VCO1 control sensitivity	$\beta 1$	V22 = 2.8 V to 3.2 V	2.4	4.8	9.6	kHz/mV
VCO2 control sensitivity	$\beta 2$	V16 = 2.8 V to 3.2 V	0.3	0.6	1.2	kHz/mV
[1st SIF Block]						
4.5 MHz output gain	VG	Vi = 1 mV, 41.25 MHz	23	26	29	dB
4.5 MHz output level	SO	Vi = 10 mV, 41.25 MHz	50	85	120	mVrms
1st SIF maximum input level	Si (max)	So + 12 dB – 1 dB	60	70		mVrms
1st SIF input resistance	Ri (SIF1)	f = 41.25 MHz	1.2	2		kΩ
1st SIF input capacity	Ci (SIF1)	f = 41.25 MHz		3	6	pF

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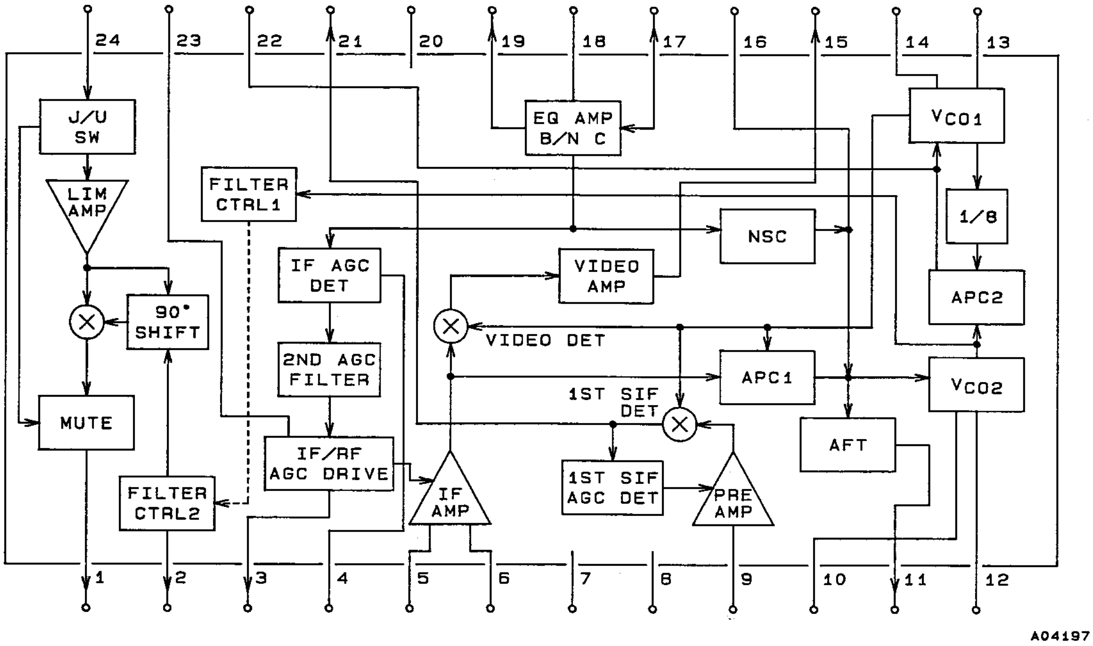
Parameter	Symbol	Conditions	min	typ	max	Unit
[SIF Block]						
SIF limiting sensitivity	Vi (lim)	Δf = 25 kHz, 400 Hz	47	53	59	dBμ
FM detection output voltage	V_O	Vi = 100 mV, Δf = 25 kHz, 400 Hz	300	400	520	mVrms
AMR	AMR	AM = 30%, 400 Hz	40	56		dB
Total harmonic distortion	THD	Δf = 25 kHz, 400 Hz		0.4	1.5	%
SIF S/N	S/N(SIF)	Δf = 25 kHz, 400 Hz	55	59		dB
[Mute defeat]						
FM mute	V24T		0.5	1.0		V
AFT defeat voltage	VD11		3.9	4.5	5.1	V
J/U SW start voltage	VJU24		1.5	2.0	2.5	V
AV mute voltage	VM23		1	1.5		V

Equivalent Circuit Block Diagram



Multinetwork PLL (Automatic Adjustment Control)

The LA7583's PIF detector uses a multinetwork PLL and a buzz canceller. The multinetwork PLL is a PLL detector that was developed in order to eliminate the need for adjustments in video detection.

This PLL detector offers the following features:

(1) Eliminates the need for adjustments in video detection.

(2) The PLL detection characteristics are unaltered.

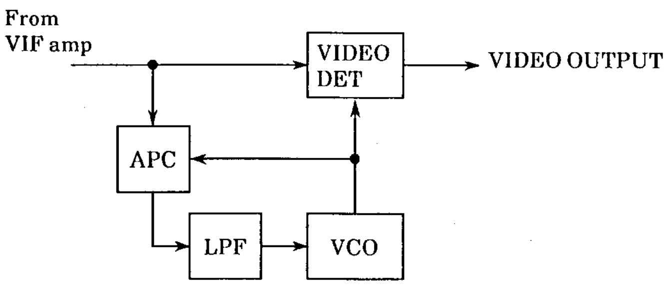
a. Offers better waveform response characteristics in comparison with the quasi-synchronous detection method.

b. The harmonic wave component of the video signal (demodulated output) is reduced.

c. The 1/2 IF signal suppression ratio is improved.

(3) Audio buzz is greatly reduced by the buzz canceller.

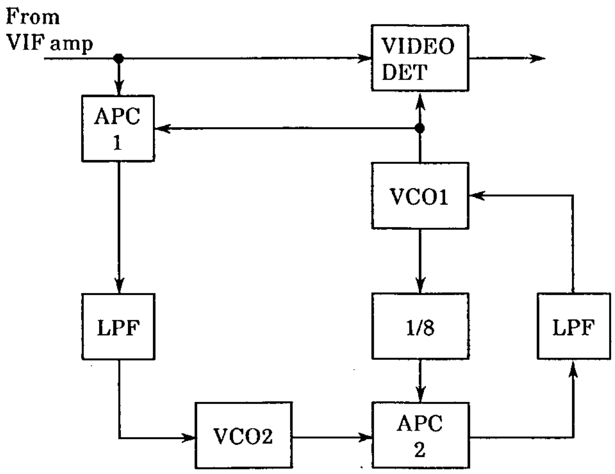
A typical PLL detector consists of the blocks shown below.



(PLL DETECTOR)

In these blocks, if the VCO coil is not adjusted to the IF frequency, a phase difference will appear in the control loop. As a result, the PLL detector detection axis will shift from the ideal 180 °. The group delay, DP characteristics, etc., deteriorate as a result.

[Multinetwork PLL]
The multinetwork PLL consists of the blocks shown below.



(MULTI NETWORK PLL)

The multinetwork PLL has two VCO circuits. Each of these form a separate PLL. The operational relationship between these circuits is as follows:

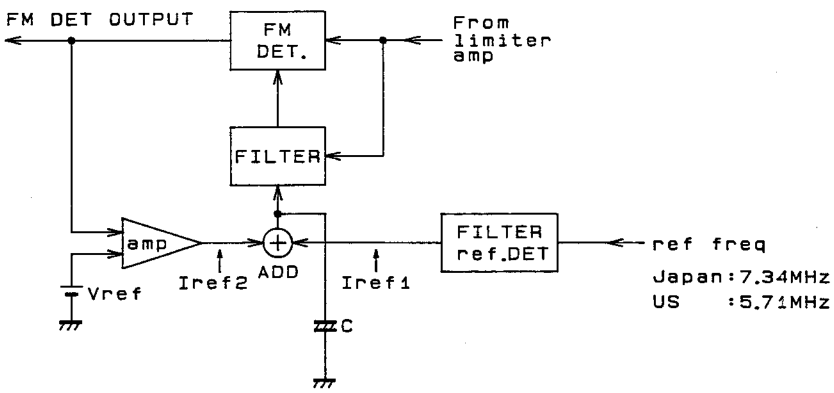
$f_{VCO1} = f_{VCO2} \times 8$

Initially, in APC1, the phases of the IF signal and the VCO carrier are compared. The control signal derived is then used to control VCO2. VCO1 is controlled by comparing the phases of VCO2 and VCO1 x 1/8. As a result, VCO1 always has the same frequency as the IF signal, and the following relationship results:

$f_{VCO1} = f_{VCO2} \times 8$

If the precision of the ceramic oscillator for f_{VCO2} is within the adjustment range for VCO in a typical PLL, the video detector phase error is very small. As a result, the multinetwork PLL operates as an ideal PLL detector.

Automatic Quadrature Tuning (AQT)
A quadrature detector that is controlled automatically is used in the FM detector. The AQT in the LA7583 consists of the blocks shown in the following diagram.



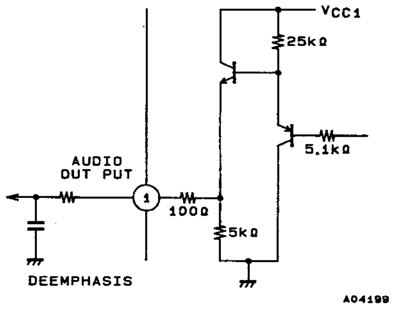
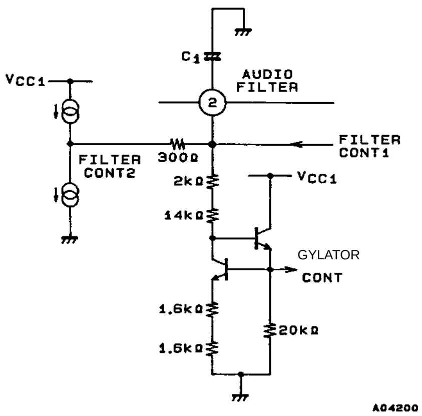
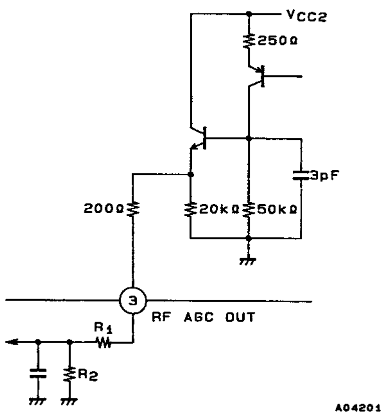
(Auto matic Quad Tuneing)

A04198

The FM detection filter (gyrator) is controlled at 4.5 MHz by the control current (Iref1) generated by reference circuit 1. At the same time, precision control is performed by using the control current (Iref2) derived by detecting the offset from the detected output so that the FM detector phase relationship is 90 °. As a result, automatic control makes an ideal quadrature detector possible.

(Note) Gyrator: Circuit-formed equivalent inductance
The SIF circuit contains a 4.5 MHz tank circuit having the gyrator and an internal capacitor.

Pin Functions

Pin No.	Symbol	Circuit Configuration	Description
1	FM DETECTOR OUTPUT		Pin 1 is an audio FM output pin. A 100 Ω resistor is connected in series with the emitter follower. (1) Monaural applications CR are used to form a de-emphasis cicuit externally. t = CR1 (2) Audio multiplexing applications Depending on the audio multiplexing decoder application, the input impedance is low, which may distort the L-R signals, etc., and degrade the stereo characteristics. In such an event, add a resistor between pin 1 and GND. R2 ≧ 5.1 kΩ
2	FM AQT FILTER		Pin 2 is the FM Automatic Quadrature Tuning filter pin. This pin controls the quadrature detector so that it remains at its center frequency (4.5 MHz), and is the point where the two control currents are added. If the value of external capacitor C1 is small, the low-range frequency characteristics deteriorate. If the capacitance is too large, the low-range characteristics improve, but the response characteristics at SW-ON, etc., worsen. The recommended value for C1 is 10 µF to 33 µF.
3	RF AGC OUTPUT		Pin 3 is the RF AGC output pin. It is an emitter output, and a protective resistor of 200 Ω is connected between pin 3 and emitter. This pin determines the resistance bleeder (R1, R2) values according to the maximum gain of the tuner.

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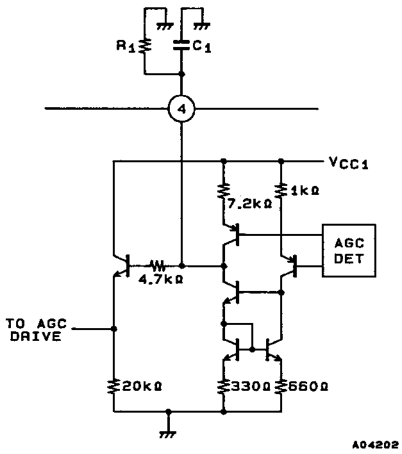
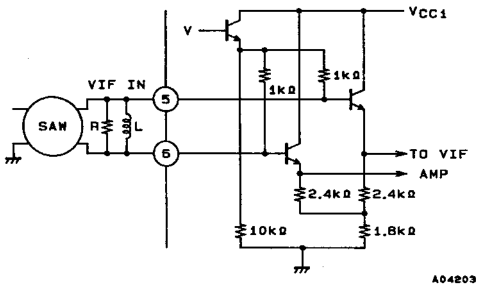
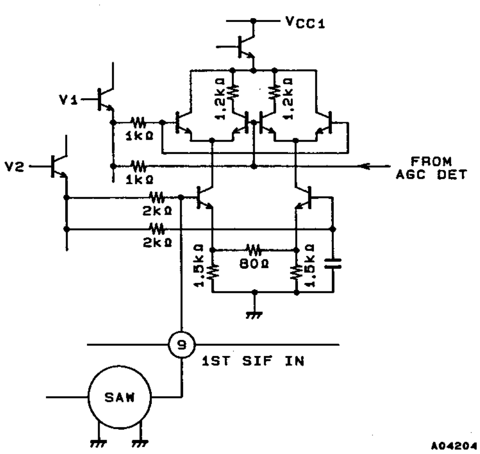
Pin No.	Symbol	Circuit Configuration	Description
4	IF AGC		Pin 4 is the 1st IFAGC filter pin. This filter smoothes out the peaks detected in the signal by the AGC detector, and generates the AGC voltage. The 2nd AGC filter (lag lead filter) is built in using filter technology. The cutoff frequency is approximately 500 Hz. • AGC filter constants and AGC speed Medium-speed AGC: R1 = 330 kΩ C1 = 0.1 µF High-speed AGC: R1 = 470 kΩ C1 = 0.056 µF
5 6	VIF INPUT		Pins 5 and 6 are the VIF amplifier input pins. The VIF amplifier has three stages, each of which uses a C cut, so when used in conjunction with a SAW filter, DC cut by a capacitor becomes unnecessary. Ri = 1.1 kΩ Ci = 3 pF
9	1st SIF INPUT		Pin 9 is the 1st SIF input pin. Input is such that DC cut must be performed using a capacitor. When a SAW filter, etc. is used in the input circuit, an L that is used to neutralize the SAW filter output capacitance and the IC input capacitance serves to improve the 1st SIF sensitivity.

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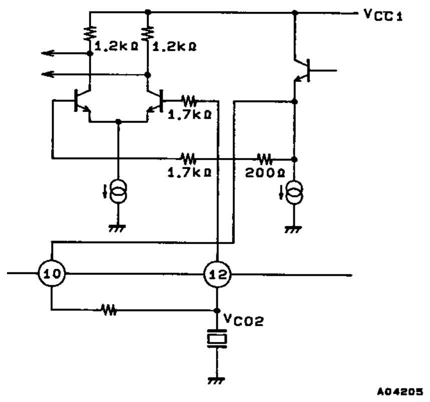
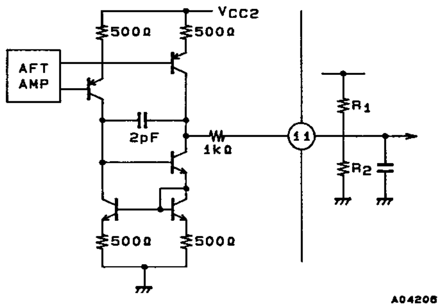
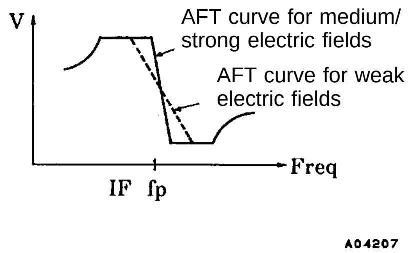
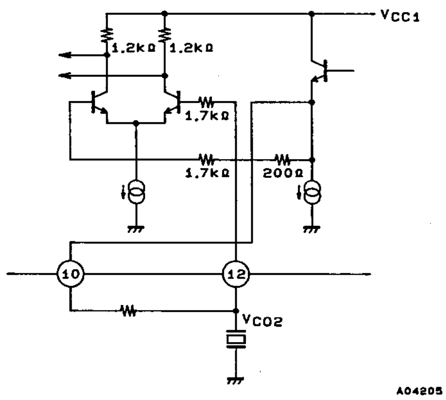
Pin No.	Symbol	Circuit Configuration	Description
10	VCOR		Pin 10 is the pin for connecting the resistor that determines the impedance of the oscillation point of the oscillating circuit by the ceramic oscillator. Oscillation frequency variations can be reduced by connecting a resistor with a tolerance of 1% between pin 10 and pin 12.
11	AFT OUTPUT		Pin 11 is the AFT output pin. This pin determines the gain (control sensitivity: β (kHz/mV)) according to the R1 and R2 bleeder resistance values. β is decreased in weak electric fields by AGC voltage in order to reduce malfunction of AFT. R1 and R2 must be 200 kΩ or less. 
12	VCO2		Pin 12 is the ceramic oscillator (VCO2) pin. A series resonance-type oscillator is used to oscillate 1/8 of the IF signal. Japan = 58.75 MHz × 1/8 U.S. = 45.75 MHz × 1/8

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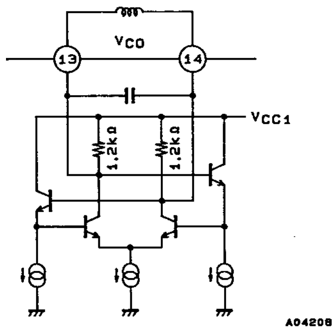
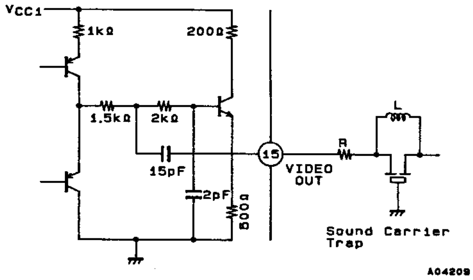
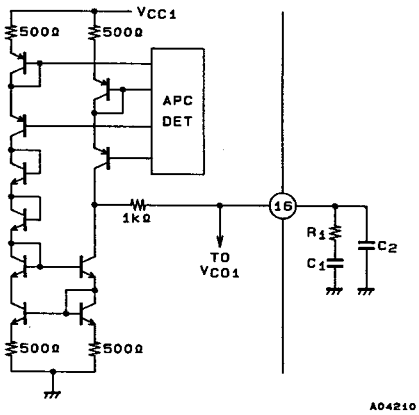
Pin No.	Symbol	Circuit Configuration	Description
13 14	VCO COIL		Pins 13 and 14 are the VCO tank circuit. VCO coil recommended • Japan 1.2 µH • U.S. 1.8 µH Make the circuit pattern between the IC and the coil as short as possible.
15	VIDEO OUTPUT		Pin 15 is the SIF carrier (4.5 MHz)-contained video output pin. The level of the video output is approximately 1.5 Vp-p.
16	APC1 FILTER		Pin 16 is the APC1 filter pin. The filter smoothes the output after comparing the phase of the IF signal with that of VCO1 in APC1. C_1 = 0.47 µF R_1 = 330 to 560Ω C_2 = 470 pF

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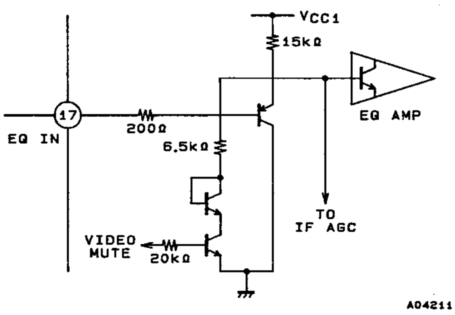
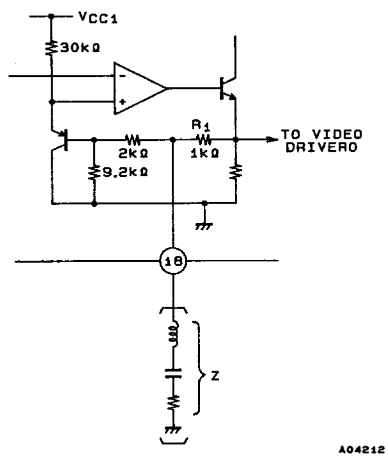
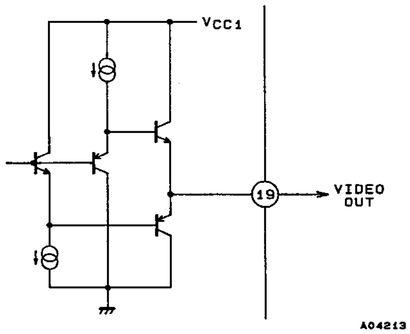
Pin No.	Symbol	Circuit Configuration	Description
17	EQUALIZER INPUT		Pin 17 is the equalizer amplifier input pin. A signal which has passed through a 4.5 MHz trap is input through pin 17 and is output through pin 19. • The input level of pin 17 is 1.5 Vp-p. This is amplified 3 dB to 2 Vp-p by the equalizer amplifier.
18	EQUALIZER FILTER		Pin 18 is the equalizer pin. The equalizer amplifier is of the voltage follower type with a voltage gain of 3 dB. To correct the frequency characteristics, connect LCR externally. The operating characteristics are as follows: $Av = \frac{Ve}{Vi} = 1 + \frac{R1}{Z}$ (times)
19	EQUALIZER OUTPUT		Pin 19 is the equalizer amplifier output pin. This output has a built-in low-impedance drive circuit.

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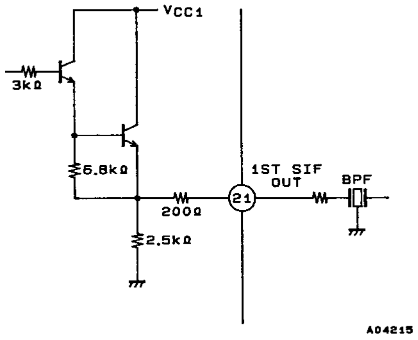
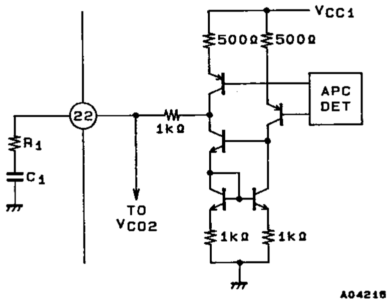
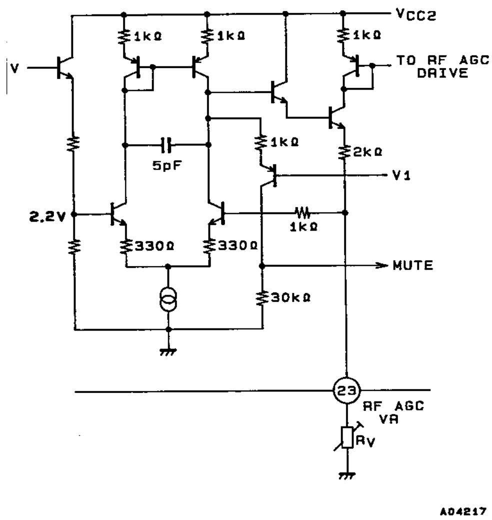
Pin No.	Symbol	Circuit Configuration	Description
21	1st SIFOUT		Pin 21 is the 1st SIF output pin. The SIF carrier output level is approximately 50 mVrms.
22	APC2 FILTER		Pin 22 is the APC2 filter pin. The filter smoothes the output after comparing the phase of VCO2 with that of VCO1 x 1/8 in APC2. C_1 = 0.47µF R_1 = 33 Ω
23	RF AGC VR		Pin 23 is the RF AGC adjusting pin. The adjustment point is where Rv approximates 15 kΩ. AV (audio/video) mute is effected by dropping this pin to GND.

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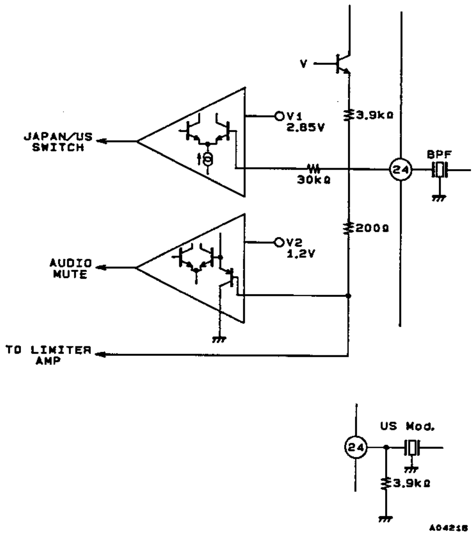
Pin No.	Symbol	Circuit Configuration	Description
24	SIF INPUT, J/U SW		Pin 24 is used both for SIF input and J/U SW audio mute. • The input impedance is approximately 1.5 kΩ. • J/U (Japan/U.S.) switch The oscillating frequency for VCO2 in Japan and the U.S. differs. However, the center frequency of the SIF detector is controlled using VCO2 as a reference. As a result, the filter control mode can be changed either by leaving this pin open or dropping it to GND through a 3.9 kΩ resistor. Open: Japan mode 3.9 kΩ: U.S. mode • Audio mute: Audio muting can be applied by dropping the voltage on this pin to 0.5 V or less.

LA7583 VCO COIL design considerations

1. Design criteria

   Allow for an adequate variable range for the IF frequency in the design. Specifically, select a coil value so that the carrier frequency is roughly in the center of the characteristics diagram shown below when 2 V and 4 V are applied to pin 22.

2. Design notes

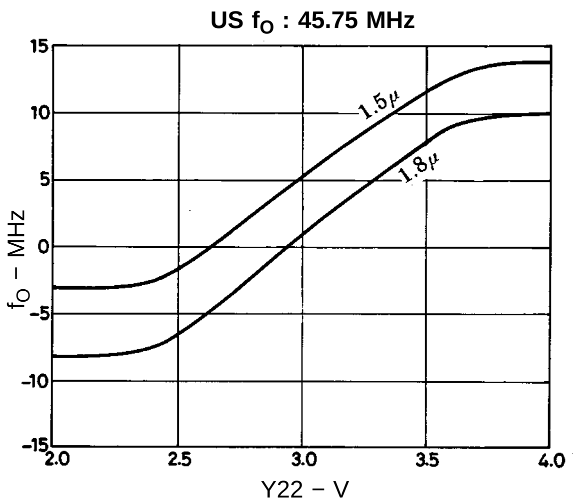
   a. When selecting the L value, the LA7583 must be soldered directly on the board. If an IC socket is used, an error in the VCO center frequency will arise from the capacitance of the socket.

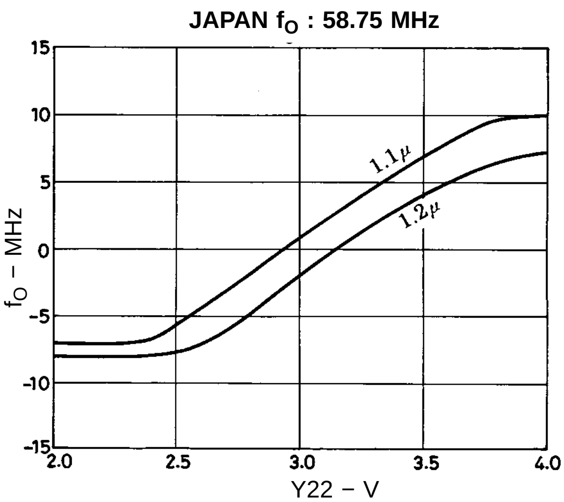
   b. The patterns for pins 13 and 14 must be made as short as possible (15 mm or less). Minimize the effect of the printed pattern.

   c. A VCO coil of which tolerance is ± 5% must be used.

3. Measuring the IF frequency range

   Drop the IF AGC (pin 4) to GND. Next, pick up the VCO carrier leak at a pin other than the VCO coil (pins 13 and 14) and read the carrier frequency. And then, apply a voltage ranging from 1.5 V to 4.5 V to pin 22, and record the characteristics of the maximum variable frequency range for VCO as shown in the diagram below.





4. Recommended VCO coil

   A. Tokyo Parts Industry Co., Ltd. 5LC JAPAN 1.2 μH ± 5%
   U.S. 1.8 μH ± 5%

Notes on Sanyo SAW Filters

There are two types of filters, depending on the piezoelectric substrate material.

(1) $LiTaO_3$ (lithium tantalate) SAW filters: TSF1xxx
TSF2xxx

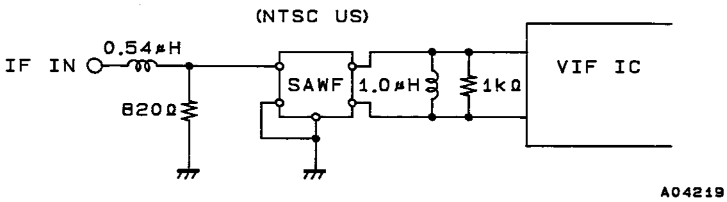
While the $LiTaO_3$ SAW filters offer excellent stability with a low temperature coefficient of –18 ppm/ °C, the insertion loss is high. However, by using a coil, etc., to obtain proper matching on the SAW filter output side (which does increase the number of external components), it is possible to suppress the insertion loss while at the same time making the level of the characteristics variable, which provides additional design freedom. (Refer to Fig. 13.) In addition, because the SAW (surface wave) reflection is small, ripple within the band can be kept low.

(2) $LiNbO_3$ (lithium niobate) SAW filter: TSF5xxx

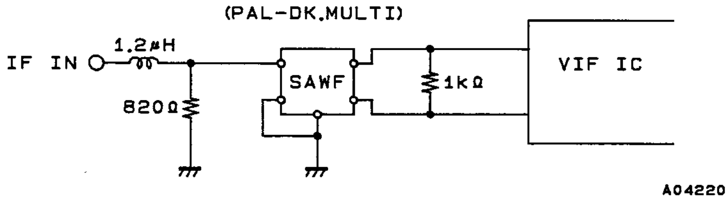
While the $LiNbO_3$ SAW filter has a high temperature coefficient of –72 ppm/ °C, it has a lower insertion loss by about 10 dB compared to the $LiTaO_3$ SAW filters. Therefore, matching on the output side of the SAW filter is not necessary. (Refer to the diagram below.) In addition, because the insertion loss is low (although the ripple within the band is somewhat higher than in the case of the $LiTaO_3$ SAW filter), the low impedance and small feedthrough diminish the effects of peripheral circuit components and the pattern layout, and make it possible to stabilize the trap characteristics outside of the band.

From the above, it is clear that the $LiTaO_3$ SAW filter is suitable for Japan and U.S. bands where the IF frequency is high, while the $LiNbO_3$ SAW filter is suitable for PAL and U.S. bands where the IF frequency is low.

$LiTaO_3$ SAW Filter



$LiNbO_3$ SAW Filter



(a) Picture wide BAND SAW Filter

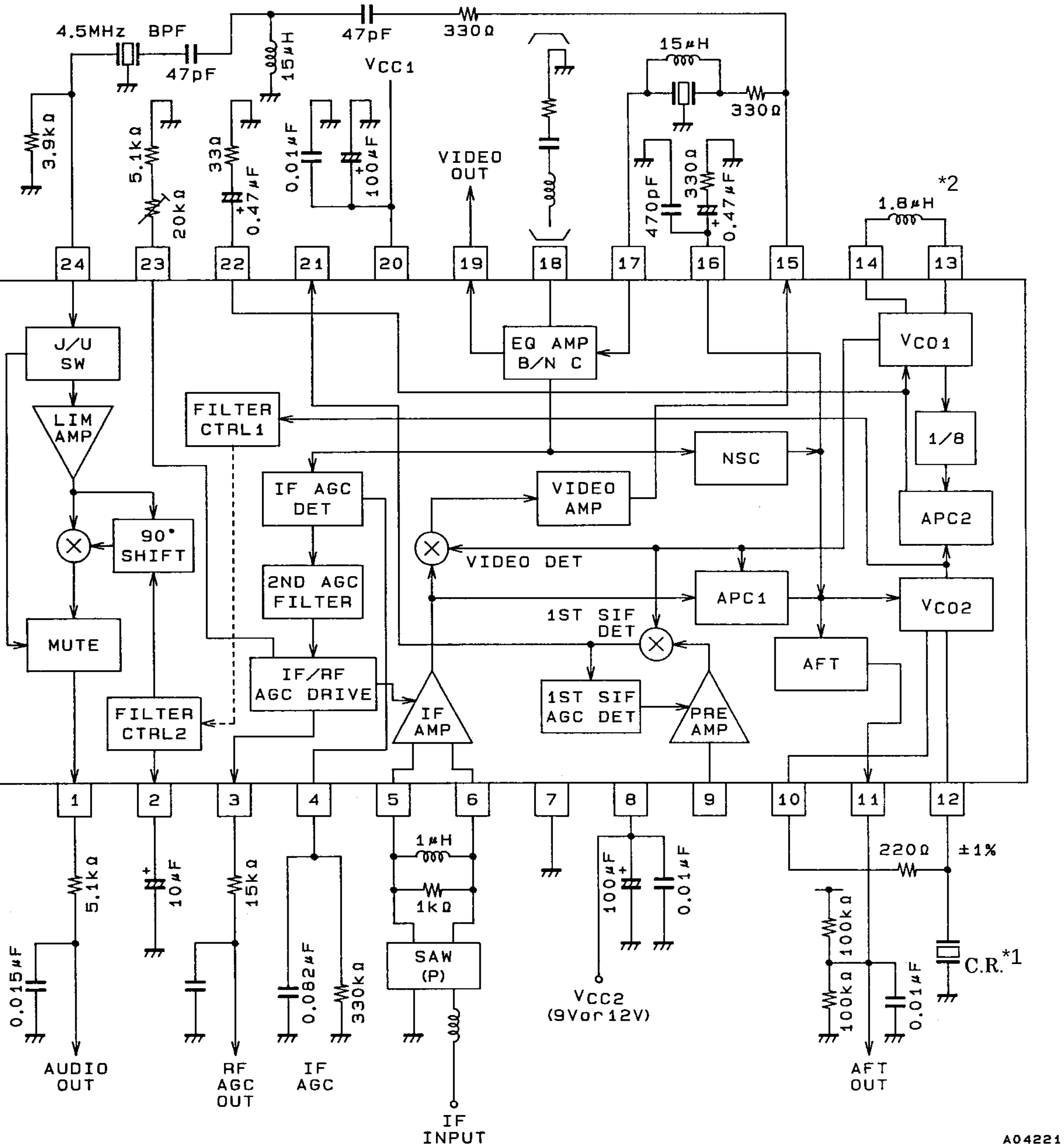
Japan TSF1137U
U.S. TSF1241U(with IS-31 Trap)

(b) INTER Carrier SAW Filter

Japan TSF1138P
U.S. TSF1220P

Test circuit Diagram

LA7583 (U.S.)



*1. TDK ceramic oscillator FCR5.71M2SF3

*2. Micro-inductor 5LC1R8, made by Tokyo Parts Industry Co., Ltd.