

M4051BP M4051BFP

8-CHANNEL ANALOG MULTIPLEXER/DEMULTIPLEXER

6249826 MITSUBISHI ELEK (LINEAR)

80C 09105

D7-51-11

DESCRIPTION

The M4051BP is a semiconductor integrated circuit consisting of a multiplexer/demultiplexer which uses a 3-bit digital input to perform selection of eight analog switches.

FEATURES

- Low ON resistance: 50Ω typ. ($V_{DD}=15V$)
- High OFF resistance: $10^9\Omega$ or greater (typ)
- Small differences in ON resistance between each switch in the package: 10Ω typ. ($V_{DD}=7.5V$, $V_{SS}=-7.5V$)
- Linearized transfer characteristics: 0.07% distortion (typ)
- Signals with amplitude greater than the logic level amplitude of the control inputs may be switched.
- Provided with an inhibit input

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

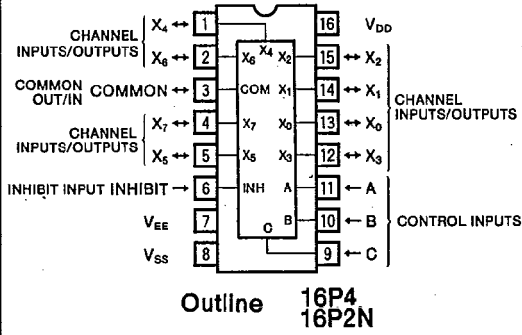
FUNCTIONAL DESCRIPTION

When a 3-bit binary input is applied to the control inputs (A, B, and C), the channel number corresponding to the binary value input (X_0 through X_7) is set at low impedance with respect to the (COMMON). All other channels remain at high impedance.

In this operation, if the (INHIBIT) input is held high, all channels (X_0 through X_7) will be put in the high-impedance state, regardless of the state of the other inputs.

It is possible to switch an analog signal of amplitude $V_{DD}-V_{EE}$ if this is greater than the logic level span $V_{DD}-V_{SS}$ for inputs (A, B, and C).

PIN CONFIGURATION (TOP VIEW)

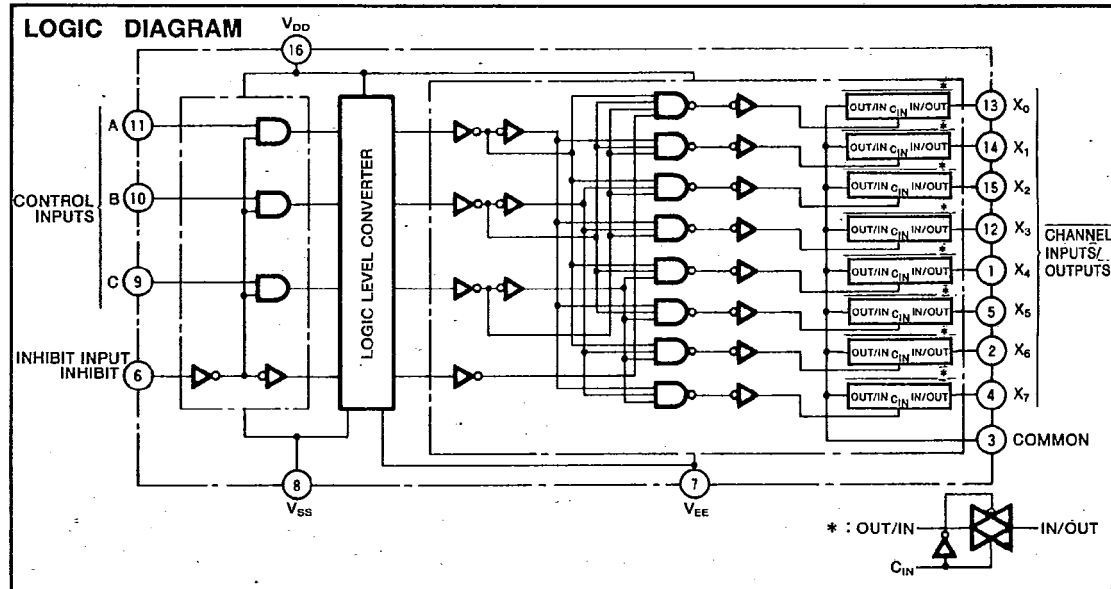


FUNCTION TABLE (Note 1)

Inhibit input	Control inputs			Channel INPUT/OUTPUT to COMMON switch selection							
	C	B	A	X_0	X_1	X_2	X_3	X_4	X_5	X_6	X_7
L	L	L	L	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF
L	L	L	H	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF
L	L	H	L	OFF	OFF	ON	OFF	OFF	OFF	OFF	OFF
L	L	H	H	OFF	OFF	OFF	ON	OFF	OFF	OFF	OFF
L	H	L	L	OFF	OFF	OFF	OFF	ON	OFF	OFF	OFF
L	H	L	H	OFF	OFF	OFF	OFF	OFF	ON	OFF	OFF
L	H	H	L	OFF	OFF	OFF	OFF	OFF	OFF	ON	OFF
L	H	H	H	OFF	OFF	OFF	OFF	OFF	OFF	OFF	ON
H	X	X	X	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF

Note 1 : X : Irrelevant
 ON : Low Impedance between X_n and COMMON ($n=0\sim7$)
 OFF : High Impedance between X_n and COMMON ($n=0\sim7$)

LOGIC DIAGRAM



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ABSOLUTE MAXIMUM RATINGS ($T_a = -40 \sim +85^\circ\text{C}$, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
$V_{DD}-V_{SS}$	Supply voltage		-0.5~20	V
$V_{DD}-V_{EE}$			-0.5~20	V
V_i	Input voltage	Control and inhibit inputs	$V_{SS}-0.5 \sim V_{DD}+0.5$	V
		Channel and common inputs	$V_{EE}-0.5 \sim V_{DD}+0.5$	V
V_{IO}	Input-to-output voltage		± 0.5	V
I_i	Input current	Control and inhibit inputs	± 10	mA
I_o	Output current	Switch-off	± 10	mA
V_o	Output voltage	Channel and common outputs	$V_{EE}-0.5 \sim V_{DD}+0.5$	V
T_{opr}	Operating temperature range		-40~+85	$^\circ\text{C}$
T_{stg}	Storage temperature range		-65~+150	$^\circ\text{C}$

RECOMMENDED OPERATING CONDITING CONDITIONS ($T_a = -40 \sim +85^\circ\text{C}$, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
$V_{DD}-V_{SS}$	Supply voltage	3		18	V
$V_{DD}-V_{EE}$		3		18	V
V_i	Input voltage	Control and inhibit inputs	V_{SS}	V_{DD}	V
		Channel and common inputs	V_{EE}	V_{DD}	V
V_o	Output voltage	V_{EE}		V_{DD}	V

ELECTRICAL CHARACTERISTICS ($V_{SS}=0\text{V}$)

Symbol	Parameter	Test conditions	Limits								Unit		
					-40 $^\circ\text{C}$			25 $^\circ\text{C}$				85 $^\circ\text{C}$	
			$V_{EE}(\text{V})$	$V_{OD}(\text{V})$	Min	Max	Min	Typ	Max	Min		Max	
V_{IH}	"H" Input voltage (A, B, C, INHIBIT)	Input-to-output current=10 μA	0	5	3.5		3.5			3.5		V	
			0	10	7.0		7.0			7.0			
			0	15	11.0		11.0			11.0			
V_{IL}	"L" Input current (A, B, C, INHIBIT)	Input-to-output current=10 μA	0	5		1.5			1.5		1.5	V	
			0	10		3.0			3.0		3.0		
			0	15		4.0			4.0		4.0		
R_{ON}	ON resistance	$V_i=5\text{V}$	0	5		500			600		800	Ω	
		$V_i=2.5\text{V}$	0	5		850			950		1300		
		$V_i=0.25\text{V}$	0	5		500			600		800		
		$V_i=10\text{V}$	0	10		210			250		300		
		$V_i=5\text{V}$	0	10		210			250		300		
		$V_i=0.25\text{V}$	0	10		210			250		300		
		$V_i=15\text{V}$	0	15		140			160		200		
		$V_i=7.5\text{V}$	0	15		140			160		200		
		$V_i=0.25\text{V}$	0	15		140			160		200		
		$V_i=5\text{V}$	-5	5		210			250		300		
		$V_i=\pm 0.25\text{V}$	-5	5		210			250		300		
		$V_i=-5\text{V}$	-5	5		210			250		300		
		$V_i=7.5\text{V}$	-7.5	7.5		140			160		200		
		$V_i=\pm 0.25\text{V}$	-7.5	7.5		140			160		200		
$V_i=-7.5\text{V}$	-7.5	7.5		140			160		200				
ΔR_{ON}	ON resistance variations between switches of the same package		-2.5	2.5				30			Ω		
			-5	5				15					
			-7.5	7.5				10					
I_{OFF}	Input-to-output off-state leakage current ($X_0 \sim X_7$ -COMMON)	$V_{IO}=10\text{V}, V_{OI}=0\text{V}$	0	10					125		nA		
		$V_{IO}=0\text{V}, V_{OI}=10\text{V}$	0	10					-125				
		$V_{IO}=18\text{V}, V_{OI}=0\text{V}$	0	18		250			250			1000	
		$V_{IO}=0\text{V}, V_{OI}=18\text{V}$	0	18		-250			-250			-1000	
I_{DD}	Quiescent supply current	$V_i=V_{DD}, V_{SS}$	0	5		20			20		150		
			0	10		40			40		300		
			0	15		80			80		600		
I_{IH}	"H" Input current (A~C, INH)	$V_{IH}=18\text{V}$	0	18		0.3			0.3		1.0 μA		
I_{IL}	"L" Input current (A~C, INH)	$V_{IL}=0\text{V}$	0	18		-0.3			-0.3		-1.0 μA		

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SWITCHING CHARACTERISTICS ($T_a=25^\circ\text{C}$, $V_{SS}=0\text{V}$)

Symbol	Parameter	Tset conditions	Limits			Unit		
			$V_{EE}(\text{V})$	$V_{DD}(\text{V})$	Min		Typ	Max
$f_{\text{max}(I/O)}$	Maximum transfer frequency	$R_L=10\text{k}\Omega$ $C_L=15\text{pF}$ Test circuit 2	-5	5		25		MHz
t_{PLH}	"L-H" and "H-L" output propagation time (A, B, C- $X_0\sim X_7$, COMMON)	$R_L=10\text{k}\Omega$ $C_L=50\text{pF}$ Test circuit 3	0	5			1000	ns
			0	10			500	
			0	15			400	
			-5	5			700	
			-7.5	7.5			500	
t_{PHL}			0	5			1000	ns
			0	10			500	
			0	15			400	
			-5	5			700	
			-7.5	7.5			500	
t_{PLH}	"L-H" and "H-L" output propagation time (INHIBIT- $X_0\sim X_7$, COMMON)	$R_L=10\text{k}\Omega$ $C_L=50\text{pF}$ Test circuit 4	0	5			1400	ns
			0	10			700	
			0	15			500	
			-5	5			900	
			-7.5	7.5			500	
t_{PHL}			0	5			1400	ns
			0	10			700	
			0	15			500	
			-5	5			900	
			-7.5	7.5			500	
t_{PLH}	"L-H" and "H-L" output propagation time ($X_0\sim X_7$ /COMMON-COMMON/ $X_0\sim X_7$)	$R_L=10\text{k}\Omega$ $C_L=50\text{pF}$ Test circuit 5	0	5			45	ns
			0	10			30	
			0	15			20	
t_{PHL}			0	5			45	ns
			0	10			30	
			0	15			20	
—	Sine-wave distortion	$R_L=10\text{k}\Omega$ $f_i=1\text{kHz}$ Test circuit 2	-5	5		0.1		%
—	Feedthrough (switch off)	$R_L=1\text{k}\Omega$ Test circuit 6	-5	5		500		kHz
—	Crosstalk (A, B, C, INHIBIT- $X_0\sim X_7$, COMMON)	$R_i=1\text{k}\Omega$ $R_L=10\text{k}\Omega$ $C_L=15\text{pF}$ Test circuit 7	0	5		200		mV
C_i	Input capacitance	Control and Inhibit Inputs					7.5	pF
		Channel and common inputs				10		

TEST CIRCUITS ($V_{SS}=0\text{V}$, capacitance C_L includes stray wiring capacitance and probe input capacitance)

1 ON resistance (R_{ON})

$R_{ON} = 10 \times \frac{(V_i - V_o)}{V_o} (\text{k}\Omega)$

Refer to the function table for conditions of control Inputs A, B, and C.

2 Maximum transfer frequency ($f_{\text{max}(I/O)}$)
Sine-wave distortion

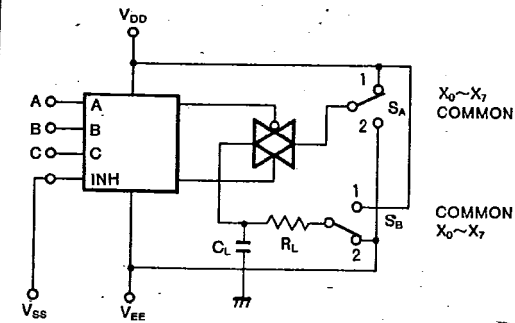
$f_{\text{max}(I/O)}$ is taken as that frequency f_i at which, using a sine-wave input of $2.5V_{P-P}$, $20 \log_{10}(V_o/V_i) = -3\text{dB}$. Refer to the function table for conditions of control Inputs A, B, and C.

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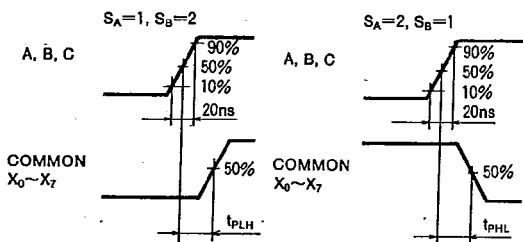
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3 "L-H" and "H-L" output propagation time
(A, B, C-X₀-X₇, COMMON)

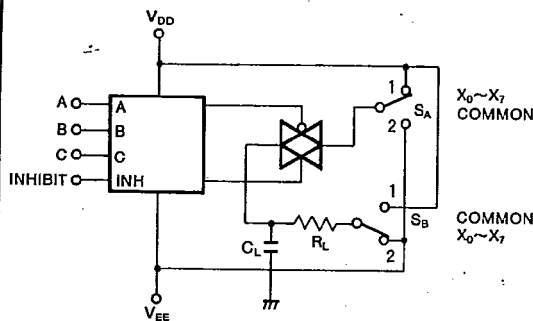


TIMING DIAGRAM

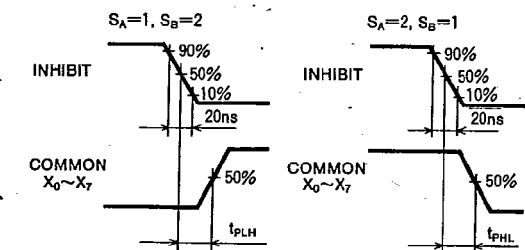


Refer to the function table for conditions of control inputs A, B, and C

4 "L-H" and "H-L" output propagation time
(INHIBIT-X₀-X₇, COMMON)

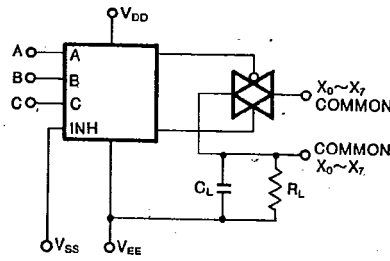


TIMING DIAGRAM

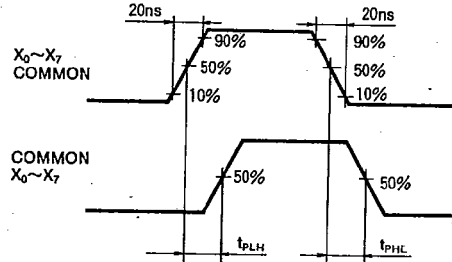


Refer to the function table for conditions of control inputs A, B, and C.

5 "L-H" and "H-L" output propagation time
(X₀-X₇/COMMON-COMMON/X₀-X₇)

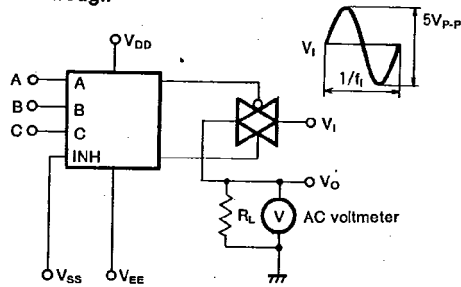


TIMING DIAGRAM



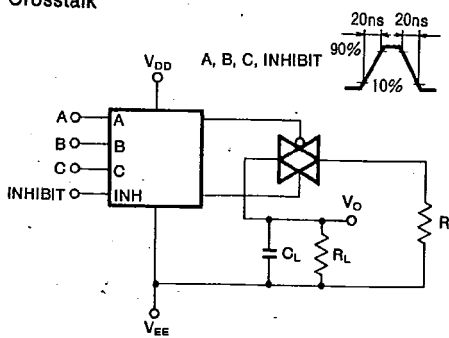
Refer to the function table for conditions of control inputs A, B, and C.

6 Feedthrough



The feedthrough is taken as that frequency f_1 at which, using a sine-wave input of $2.5V_{P-P}$, $20 \log_{10}(V_0/V_1) = -50dB$. Refer to the function table for conditions of control inputs A, B, and C.

7 Crosstalk



Refer to the function table for conditions of control inputs A, B, and C.