M56783AFP

3 CHANNEL ACTUATOR DRIVER

DESCRIPTION

The M56783AFP is a semiconductor integrated circuit in order to drive 3ch actuator.

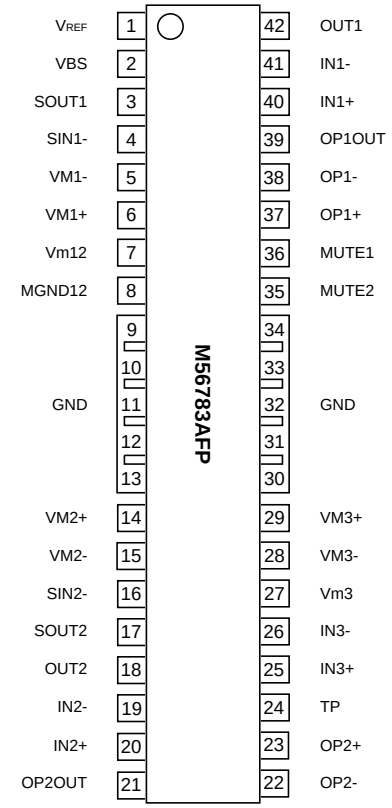
FEATURES

- 3.3V DSP available.
- Low saturation voltage.
- By taking advantage of the bootstrap function, the saturation voltage can be lower.
- There are two motor power supplies.
  Vm12 CH1, 2 motor power supply-1
  Vm3 CH3 motor power supply-2
- 7V power-supply is possible (Vm12 = 12V and MGND12 = 5V)
- Flexible Input amplifier setting. (It enables PWM control.)
- CH1 and CH2 can act in the Current Control mode.
- Low cross-over distortion.
- Wide supply voltage range. (4.5V – 13.2V)
- Including Thermal Shut Down circuit.
- Including 2 Operational Amplifiers.
- Including Mute circuit (2 lines).

APPLICATION

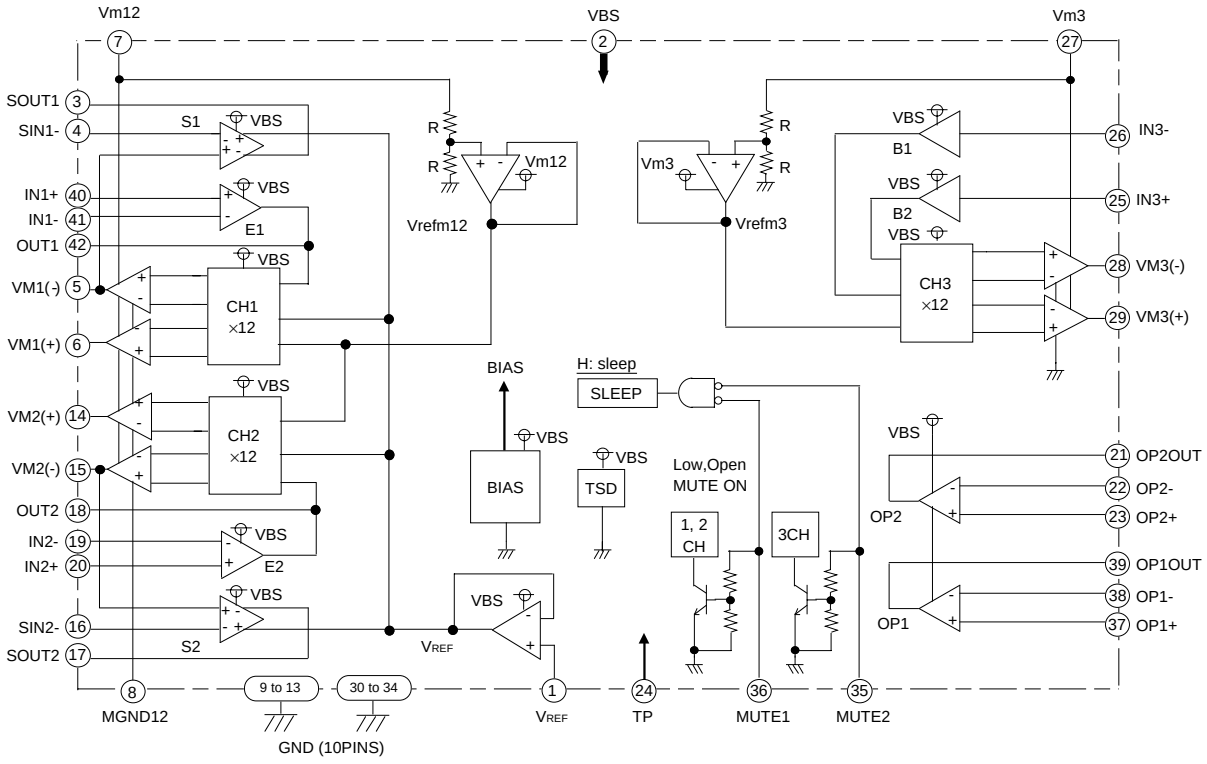
MD, CD-audio, CD-ROM, VCD, DVD etc.

PIN CONFIGURATION (TOP VIEW)



Outline 42P9R-F

BLOCK DIAGRAM



PIN DESCRIPTION

Pin No.	Symbol	Function	Pin No.	Symbol	Function
①	VREF	Reference voltage input	㊷	OUT1	E3 amplifier output
②	VBS	Bootstrap power supply	㊶	IN1-	E1 amplifier inverted input
③	SOUT1	S1 amplifier output	㊵	IN1+	E1 amplifier non-inverted input
④	SIN1-	S1 amplifier inverted input	㊴	OP1OUT	OP1 amplifier output
⑤	VM1-	CH1 inverted output	㊳	OP1-	OP1 amplifier inverted input
⑥	VM1+	CH1 non-inverted output	㊲	OP1+	OP1 amplifier non-inverted input
⑦	Vm12	1CH, 2CH Motor power supply	㊱	MUTE1	1CH, 2CH mute
⑧	MGND	Motor GND	㉟	MUTE2	3CH mute
⑨ – ⑬	GND	GND	㉘ – ㉞	GND	GND
⑭	VM2+	CH2 non-inverted output	㉙	VM3+	CH3 non-inverted output
⑮	VM2-	CH2 inverted output	㉘	VM3-	CH3 inverted output
⑯	SIN2-	S2 amplifier inverted input	㉗	Vm3	3CH Motor power supply
⑰	SOUT2	S2 amplifier output	㉖	IN3-	B1 buffer input
⑱	OUT2	E2 amplifier output	㉕	IN3+	B2 buffer input
⑲	IN2-	E2 amplifier inverted input	㉔	TP	TEST *Note1
⑳	IN2+	E2 amplifier non-inverted input	㉓	OP2+	OP2 amplifier non-inverted input
㉑	OP2OUT	OP2 amplifier output	㉒	OP2-	OP2 amplifier inverted input

*Note1. The ㉔ pin (TP) is test terminal. Please make an open the ㉔ pin (TP).

ABSOLUTE MAXIMUM RATING (Ta = 25°C)

Symbol	Parameter	Conditions	Rating	Units
VBS	Bootstrap power supply	VBS power supply	15	V
Vm	Motor power supply	Vm power supply	15	V
Io12	1CH, 2CH Output Current	*Note2	1.0	A
Io3	3CH Output Current		0.7	A
Vin	Maximum input voltage of terminals	①, ⑲, ⑳, ㉒, ㉓, ㉕, ㉖, ㉟, ㊱, ㊲, ㊳, ㊵, ㊶ Pins	0 – VBS	V
		④, ⑯ Pins	Vm12	V
Pt	Power dissipation	Free Air	1.2	W
Kθ	Thermal derating	Free Air	9.6	mW/°C
Tj	Junction temperature		150	°C
Topr	Operating temperature		-20 – +75	°C
Tstg	Storage temperature		-40 – +150	°C

*Note2. The ICs must be operated within the Pt (power dissipation) or the area of safety operation.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Limits			Units
		Min.	Typ.	Max.	
Vm12, Vm3	Motor power supply	4.5	5.0	13.2	V
VBS	Bootstrap power supply	—	Vm + 1.0	13.2	V

ELECTRICAL CHARACTERISTICS (Ta = 25°C, VBS = 12V, Vm12 = Vm3 = 5V unless otherwise noted)

Symbol	Parameter	Conditions	Limits			Units
			Min.	Typ.	Max.	
$I_{CC}1$	Supply current - 1	VBS, Vm12, Vm3 current	—	35	50	mA
$I_{CC}2$	Supply current - 2	VBS, Vm12, Vm3 current under Sleep Mode (MUTE1 = MUTE2 =0V).	—	—	10	μA
Vsat1	CH1 Saturation voltage	Top and Bottom saturation voltage. Load current 0.5A (bootstrap)	—	0.6	0.9	V
Vsat2	CH2 Saturation voltage		—	0.6	0.9	V
Vsat3	CH3 Saturation voltage		—	0.6	0.9	V
Voff1	CH1 output offset voltage	V_{REF} = OUT1 = 1.65V	-47	—	47	mV
Voff2	CH2 output offset voltage	V_{REF} = OUT2 = 1.65V	-47	—	47	mV
Voff3	CH3 output offset voltage	IN3+ = IN3- = 1.65V	-47	—	47	mV
VinOP	OP1, OP2 amplifier input voltage range		0	—	VBS-2.0	V
VoutOP	OP1, OP2 amplifier output voltage range	No load	0.5	—	VBS-1.0	V
VofOP	OP1, OP2 amplifier offset voltage	Vin = 1.65V and ±2mA load	-10	—	+10	mV
IinOP	OP1, OP2 amplifier input current		-1	—	0	μA
Vmute-on	Mute-on voltage	Mute-on	—	—	0.8	V
Vmute-off	Mute-off voltage	Mute-off	2.0	—	—	V
Imute	Mute terminal input current	Mute terminal input current (at 5V input voltage)	—	—	250	μA

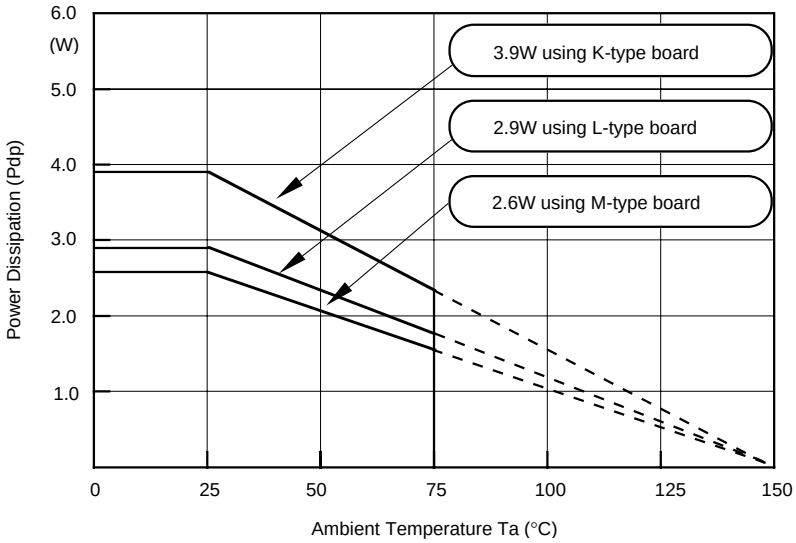
ELECTRICAL CHARACTERISTICS (Ta = 25°C, VBS = 12V, Vm12 = Vm3 = 5V unless otherwise noted)

Symbol	Parameter	Conditions	Limits			Units
			Min.	Typ.	Max.	
Gain1	CH1 Voltage Gain between input and output	$\frac{\{VM1(+) - VM1(-)\}}{(OUT1 - V_{REF})}$	10.8	12	13.2	V/V
Gain2	CH2 Voltage Gain between input and output	$\frac{\{VM2(+) - VM2(-)\}}{(OUT2 - V_{REF})}$	10.8	12	13.2	V/V
Gain3	CH3 Voltage Gain between input and output	$\frac{\{VM3(+) - VM3(-)\}}{(IN3(+) - IN3(-))}$	10.8	12	13.2	V/V
VinE	E1, 2 amplifier input voltage range		0.5	—	VBS-2.0	V
VoutE	E1, 2 amplifier output voltage range	no load	0.5	—	VBS-0.5	V
VofE	E1, 2 amplifier offset voltage	Vin = 1.65V (at buffer)	-10	—	+10	mV
IinE	E1, 2 amplifier input current	IN+ = IN- = 1.65V	-1	—	0	µA
VinB	B1, 2 buffer input voltage range	VBS=12V	0	—	5.0	V
		VBS=5.0V and Vm3=5.0V	0	—	3.0	
IinB	B1, 2 buffer input current	IN3+ = IN3- = 1.65V	-1	—	0	µA
GainS	S1, 2 amplifier Voltage Gain between input and output	S1: (SOUT1 – V_{REF}) / (VM1+ – SIN1-) S2: (SOUT2 – V_{REF}) / (VM2+ – SIN2-)	0.9	1	1.1	V/V
VinS	S_{IN}1-, S_{IN}2- input voltage range	V_{REF} = 1.65V	0	—	Vm12	V
VoutS	S1, 2 amplifier output voltage range	no load	1.0	—	VBS-1.0	V
VofS	S1, 2 amplifier offset voltage	S1: (SOUT1 – V_{REF}) at SIN1- = VM1+ S2: (SOUT2 – V_{REF}) at SIN2- = VM2+ V_{REF} = 1.65V	-20	—	+20	mV
VinV_{REF}	V_{REF} amplifier input voltage range		0.5	—	VBS-2.0	V
IinV_{REF}	V_{REF} amplifier input current	V_{REF} = 1.65V	-1	—	0	µA

THERMAL CHARACTERISTICS

Symbol	Parameter	FUNCTION START TEMPERATURE OF IC			FUNCTION STOP TEMPERATURE OF IC			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
TSD	Thermal Shut Down	—	165	—	—	125	—	°C

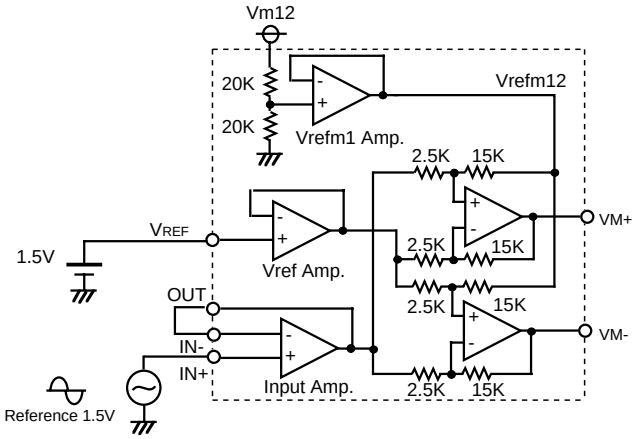
THERMAL DERATING

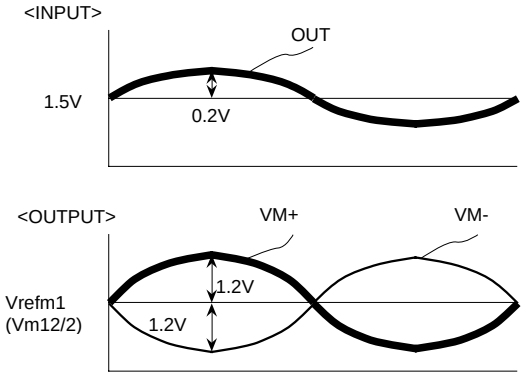


This IC's package is POWER-SSOP, so improving the board on which the IC is mounted enables a large power dissipation without a heat sink.
For example, using an 1 layer glass epoxy resin board, the IC's power dissipation is 2.6W at least. And it comes to 3.9W by using an improved 2 layer board.
The information of the K, L, M type board is shown in the board information.

I/O CHARACTERISTICS OF EACH CHANNELS

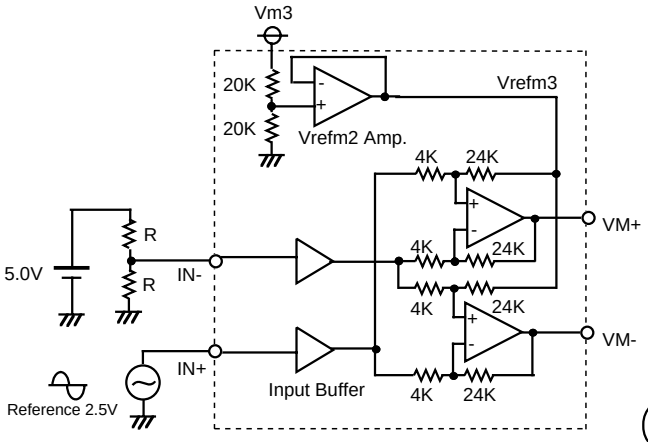
CH1, 2 amplifier

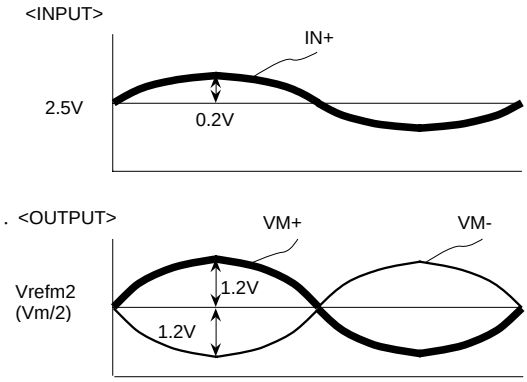




Gain = ×12

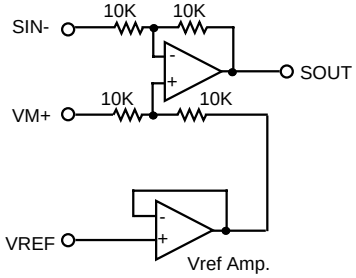
CH3 amplifier

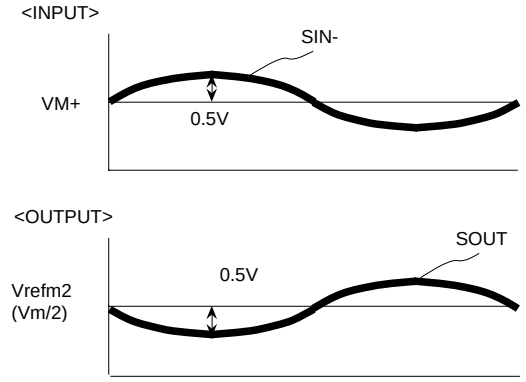




Gain = ×12

S1, S2 amplifier





Gain = ×1

MUTE FUNCTION

This IC has two MUTE terminal (MUTE1 and MUTE2).
It is possible to control ON / OFF of each circuit (CH1, CH2, CH3, etc) by external logic inputs.
The table 1 shows its function.
In case of both MUTE1 and MUTE2 is LOW or OPEN, the bias of all circuit becomes OFF.
Therefore, this mode is available in order to reduce the power dissipation when the waiting mode.

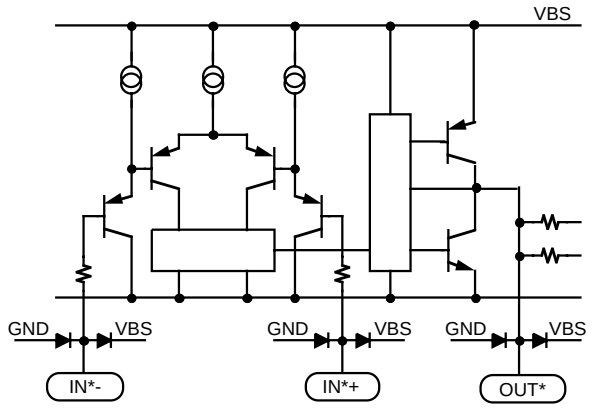
Table 1.

MUTE1	MUTE2	CH1, CH2 CIRCUIT	CH3 CIRCUIT	OP1, OP2 CIRCUIT	BIAS CIRCUIT	TSD CIRCUIT
H	H	ON	ON	ON	ON	ON
H	L,OPEN	ON	OFF	ON	ON	ON
L,OPEN	H	OFF	ON	ON	ON	ON
L,OPEN	L,OPEN	OFF	OFF	OFF	OFF	OFF

I/O TERMINAL EQUIVALENT CIRCUIT

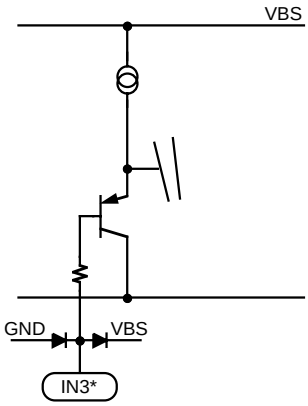
(1) E1, E2 input amplifier I/O terminal equivalent circuit

(IN1+, IN1-, OUT1, IN2+, IN2-, OUT2)



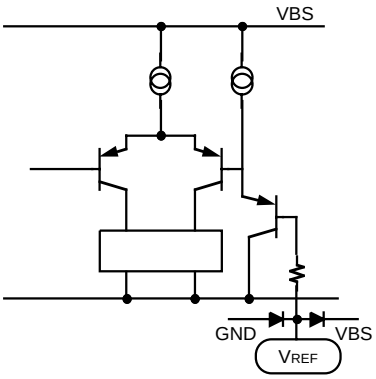
(2) B1, B2 input buffer input terminal equivalent circuit

(IN3+, IN3-)



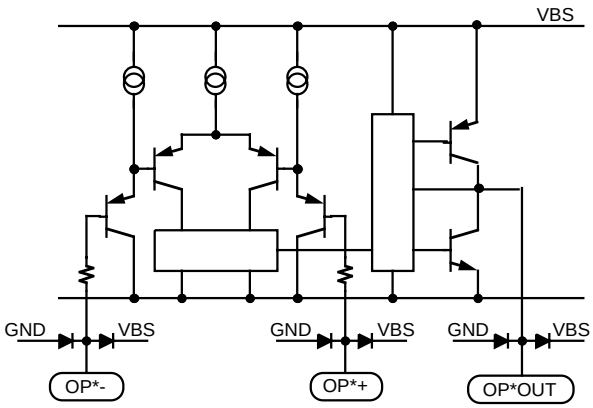
(3) V_{REF} amplifier input terminal equivalent circuit

(V_{REF})



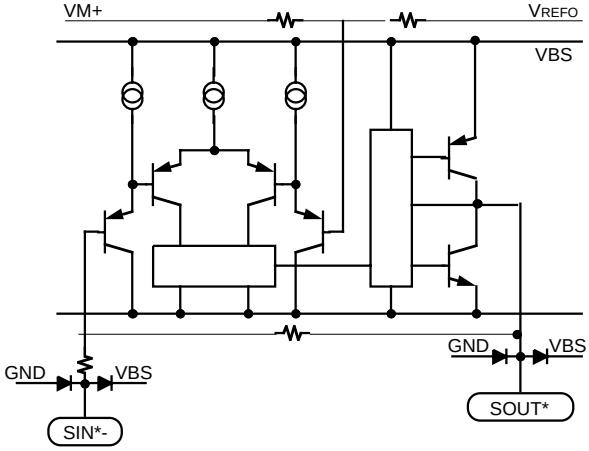
(4) OP1, OP2 input buffer I/O terminal equivalent circuit

(OP1+, OP1-, OP1OUT, OP2+, OP2-, OP2OUT)



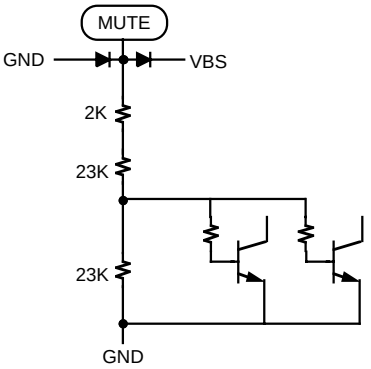
(5) S1, S2 input buffer I/O terminal equivalent circuit

(SIN1-, SOUT1, SIN2-, SOUT2)



(6) MUTE equivalent circuit

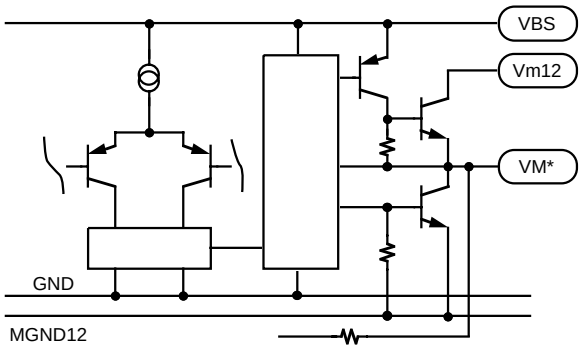
(MUTE1, MUTE2)



I/O TERMINAL EQUIVALENT CIRCUIT

(7) CH1,CH2 power amplifier output terminal equivalent circuit

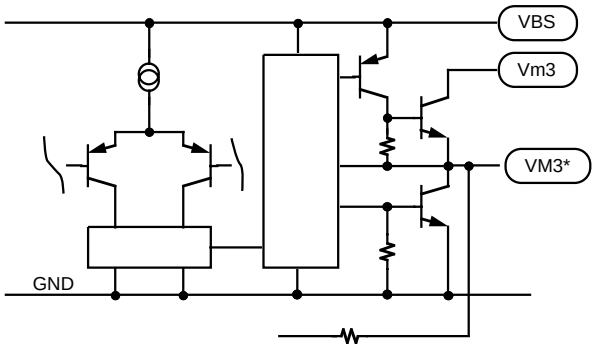
(VM1+, VM1-, VM2+, VM2-)



The equivalent circuits of an output stage of the power amplifiers are shown in (7).
The power supplies of CH1, CH2 are Vm12.
And the power supplies of CH3 are Vm3.
The source side of the power amplifier output stage consists of a PNP and a NPN.
The emitta of the PNP is connected to VBS. So the power of the PNP supplies can be adjusted externally.

(8) CH3 power amplifier output terminal equivalent circuit

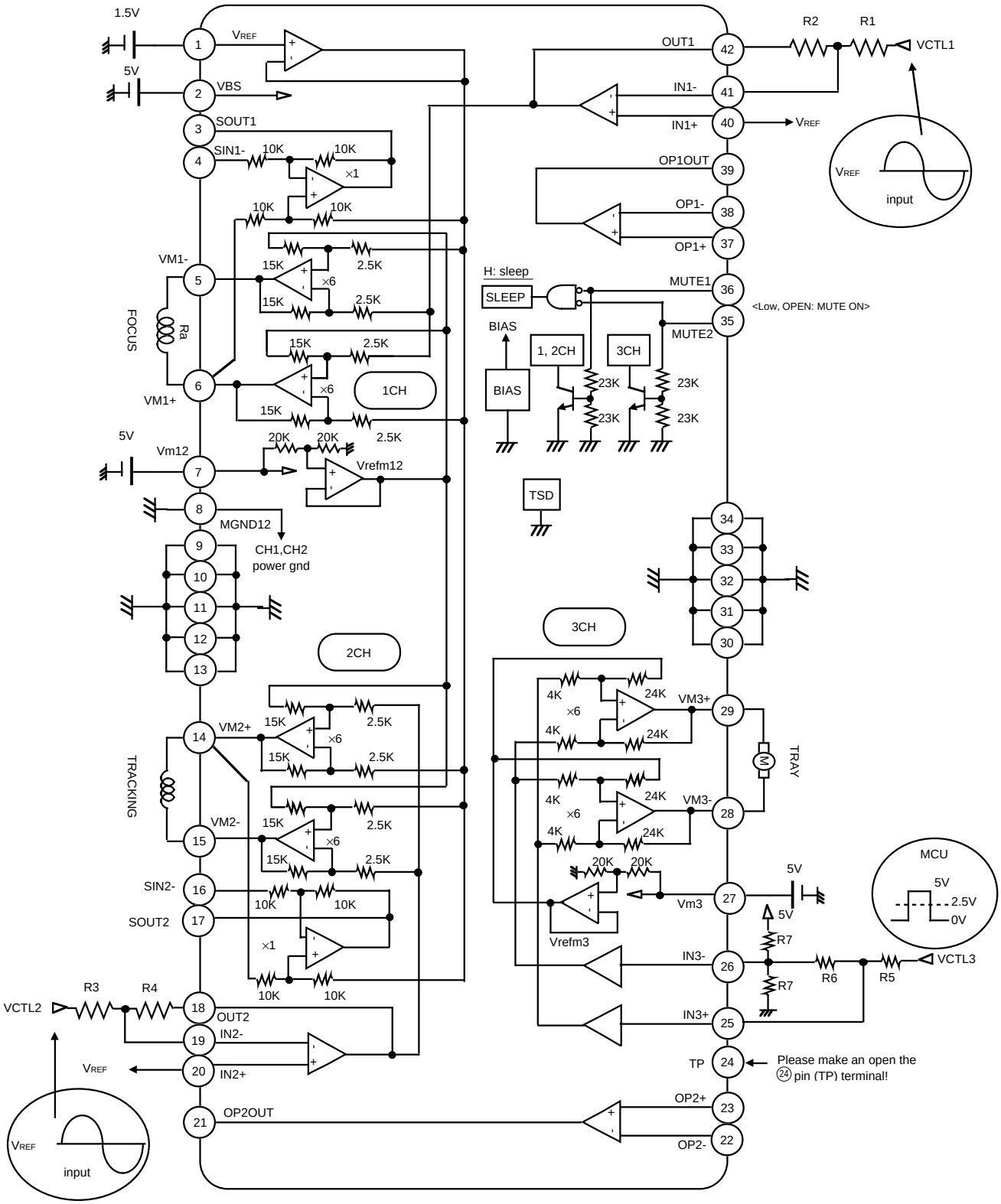
(VM3+, VM3-)



About bootstrap advantage
The output stage of the power amplifiers consists of the preceding components. If VBS is provided with higher voltage input than Vm* (The recommendation voltage is Vm+1V) externally, the output range can be wider than that of VBS = Vm.
Please take advantage of this bootstrap function for the system which has many power supplies. And it is the same with the external bootstrap circuit which provides VBS with higher voltage inputs than Vm*.
Also the bootstrap can decrease the saturation voltage at the source side of the power amplifier output stage. Therefore, when the outputs of the power amplifiers which drive motors and actuators are fully swung, the power dissipation of the IC will be decreased.

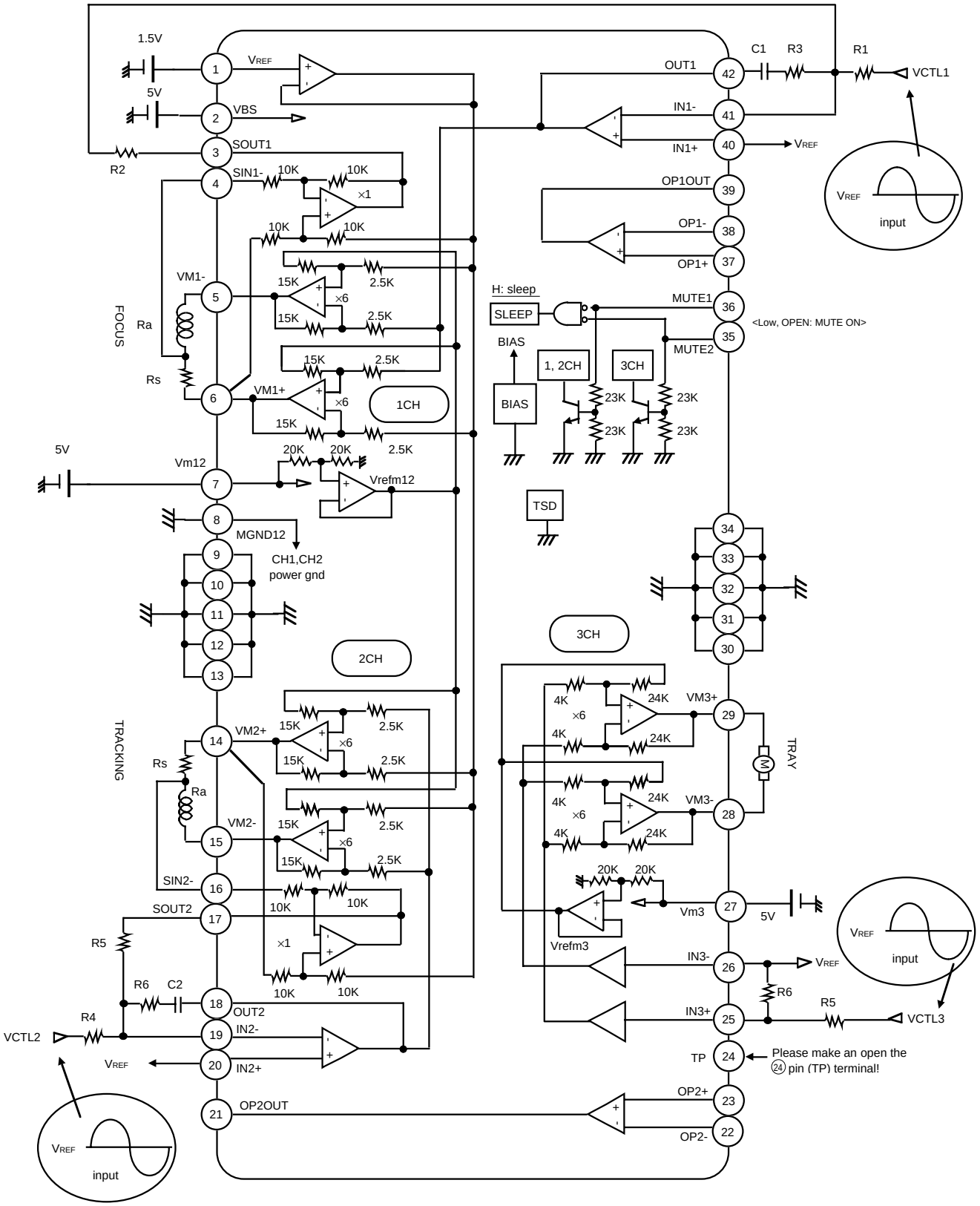
APPLICATION CIRCUIT NO. 1

- Single input (linear signal)
- Direct voltage control



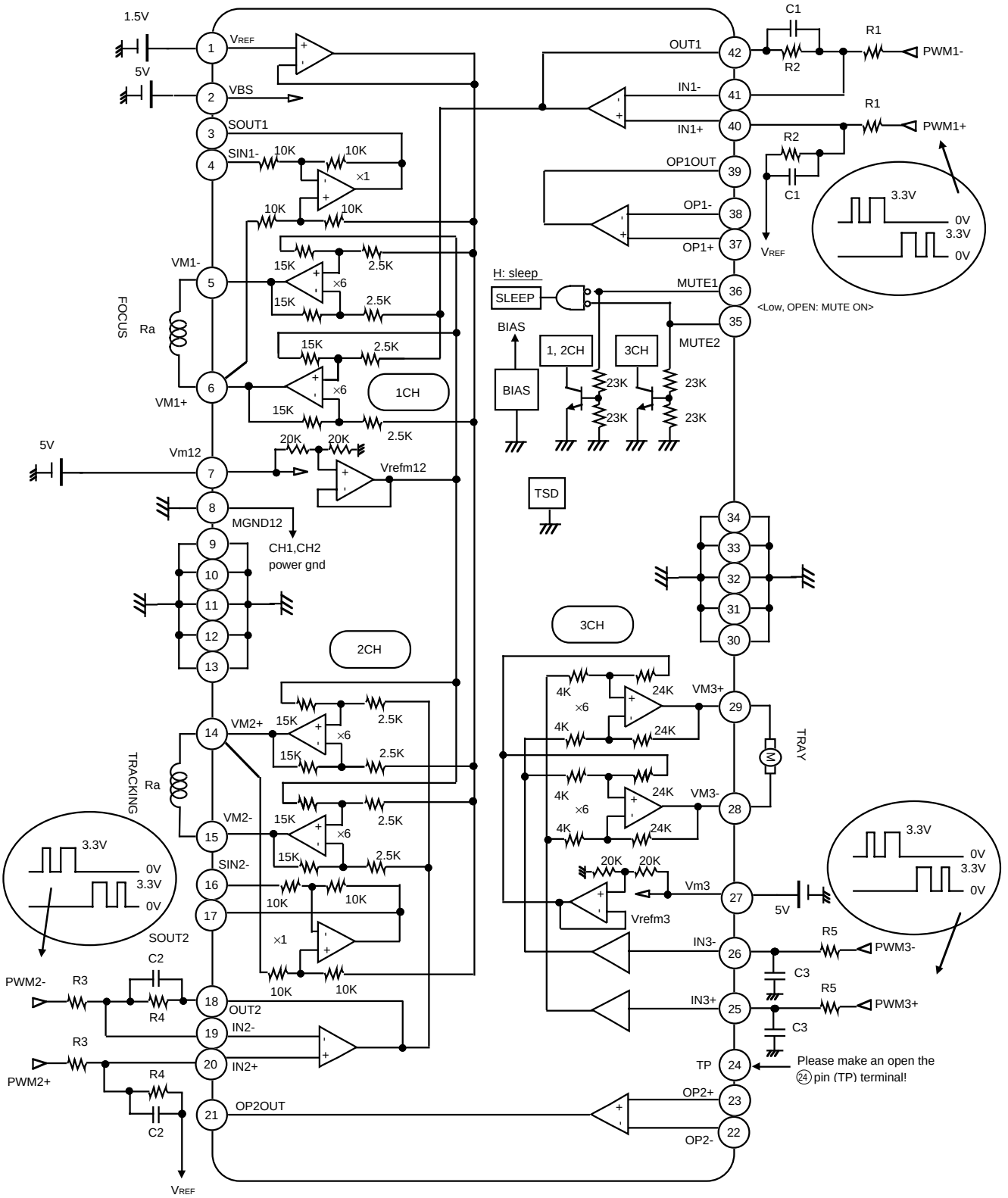
APPLICATION CIRCUIT NO. 2

- Single input (linear signal)
- Direct current control (for FOCUS and TRACKING)



APPLICATION CIRCUIT NO. 3

- Differential PWM input (for FOCUS and TRACKING and 3CH)
- Direct voltage control



APPLICATION CIRCUIT NO. 4

- Differential PWM input (for FOCUS and TRACKING and 3CH)
- Direct current control (for FOCUS and TRACKING)