



MOTOROLA

MCM4116B

16,384-BIT DYNAMIC RANDOM ACCESS MEMORY

The MCM4116B is a 16,384-bit, high-speed dynamic Random Access Memory designed for high-performance, low-cost applications in mainframe and buffer memories and peripheral storage. Organized as 16,384 one-bit words and fabricated using Motorola's highly reliable N-channel double-polysilicon technology, this device optimizes speed, power, and density tradeoffs.

By multiplexing row and column address inputs, the MCM4116B requires only seven address lines and permits packaging in Motorola's standard 16-pin dual in-line packages. This packaging technique allows high system density and is compatible with widely available automated test and insertion equipment. Complete address decoding is done on chip with address latches incorporated.

All inputs are TTL compatible, and the output is 3-state TTL compatible. The data output of the MCM4116B is controlled by the column address strobe and remains valid from access time until the column address strobe returns to the high state. This output scheme allows higher degrees of system design flexibility such as common input/output operation and two dimensional memory selection by decoding both row address and column address strobes.

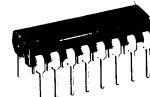
The MCM4116B incorporates a one-transistor cell design and dynamic storage techniques, with each of the 128 row addresses requiring a refresh cycle every 2 milliseconds.

- Flexible Timing with Read-Modify-Write, RAS-Only Refresh, and Page-Mode Capability
- Industry Standard 16-Pin Package
- 16,384 X 1 Organization
- $\pm 10\%$ Tolerance on All Power Supplies
- All Inputs are Fully TTL Compatible
- Three-State Fully TTL-Compatible Output
- Common I/O Capability When Using "Early Write" Mode
- On-Chip Latches for Addresses and Data In
- Low Power Dissipation — 463 mW Active, 20 mW Standby(Max)
- Fast Access Time Options: 150 ns — MCM4116BP-15, BC-15
200 ns — MCM4116BP-20, BC-20
250 ns — MCM4116BP-25, BC-25
300 ns — MCM4116BP-30, BC-30
- Easy Upgrade from 16-Pin 4K RAMs

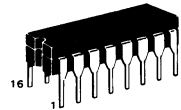
MOS

(N-CHANNEL)

16,384-BIT DYNAMIC RANDOM ACCESS MEMORY



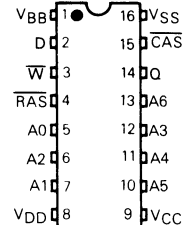
P SUFFIX
PLASTIC PACKAGE
CASE 648



C SUFFIX
FRIT-SEAL CERAMIC PACKAGE
CASE 620

DRAM

PIN ASSIGNMENT



PIN NAMES

A0-A6	Address Inputs
CAS	Column Address Strobe
D	Data In
Q	Data Out
RAS	Row Address Strobe
W	Read/Write Input
VBB	Power (-5 V)
VCC	Power (+5 V)
VDD	Power (+12 V)
VSS	Ground

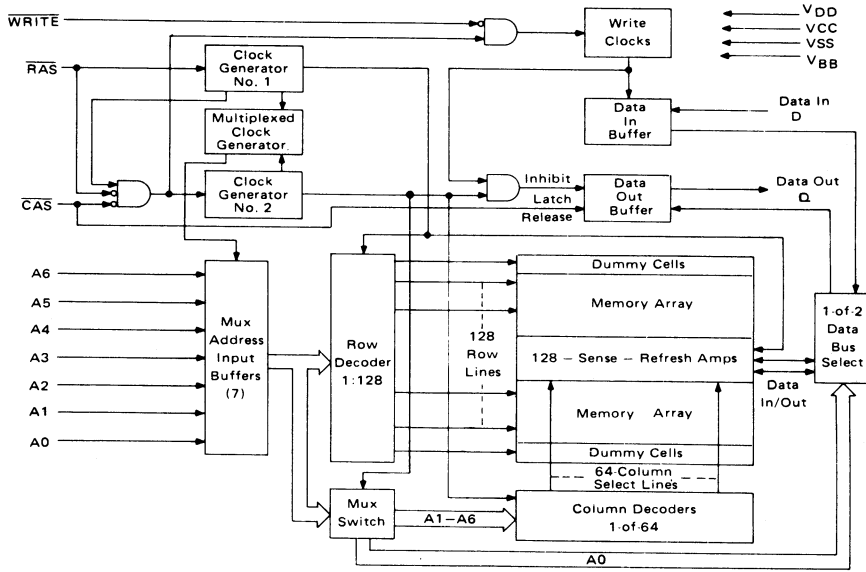
This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Voltage on Any Pin Relative to VBB	V_{in}, V_{out}	-0.5 to +20	V
Operating Temperature Range	T_A	0 to +70	$^{\circ}C$
Storage Temperature Range	T_{stg}	-65 to +150	$^{\circ}C$
Power Dissipation	P_D	1.0	W
Data Out Current	I_{out}	50	mA

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

BLOCK DIAGRAM



DC OPERATING CONDITIONS AND CHARACTERISTICS
(Full operating voltage and temperature range unless otherwise noted.)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Supply Voltage	V _{DD}	10.8	12.0	13.2	V	1
	V _{CC}	4.5	5.0	5.5	V	1, 2
	V _{SS}	0	0	0	V	1
	V _{BB}	-4.5	-5.0	-5.5	V	1
Logic 1 Voltage, RAS, CAS, WRITE	V _{IHC}	2.4	—	7.0	V	1
Logic 1 Voltage, all inputs except RAS, CAS, WRITE	V _{IH}	2.4	—	7.0	V	1-
Logic 0 Voltage, all inputs	V _{IL}	-1.0	—	0.8	V	1

DC CHARACTERISTICS (V_{DD} = 12 V ± 10%, V_{CC} = 5.0 V ± 10%, V_{BB} = -5.0 V ± 10%, V_{SS} = 0 V, T_A = 0 to 70°C.)

Characteristic	Symbol	Min	Max	Units	Notes
Average V _{DD} Power Supply Current	I _{DD1}	—	35	mA	4
V _{CC} Power Supply Current	I _{CC}	—	—	mA	5
Average V _{BB} Power Supply Current	I _{BB1,3}	—	200	μA	
Standby V _{BB} Power Supply Current	I _{BB2}	—	100	μA	
Standby V _{DD} Power Supply Current	I _{DD2}	—	1.5	mA	6
Average V _{DD} Power Supply Current during "RAS only" cycles	I _{DD3}	—	27	mA	4
Input Leakage Current (any input)	I _{I(L)}	—	10	μA	
Output Leakage Current	I _{O(L)}	—	10	μA	6, 7
Output Logic 1 Voltage @ I _{out} = -5 mA	V _{OH}	2.4	—	V	2
Output Logic 0 Voltage @ I _{out} = 4.2 mA	V _{OL}	—	0.4	V	

NOTES:

- All voltages referenced to V_{SS}. V_{BB} must be applied before and removed after other supply voltages.
- Output voltage will swing from V_{SS} to V_{CC} under open circuit conditions. For purposes of maintaining data in power-down mode, V_{CC} may be reduced to V_{SS} without affecting refresh operations. V_{OH(min)} specification is not guaranteed in this mode.
- Several cycles are required after power-up before proper device operation is achieved. Any 8 cycles which perform refresh are adequate.
- Current is proportional to cycle rate; maximum current is measured at the fastest cycle rate.
- I_{CC} depends upon output loading. The V_{CC} supply is connected to the output buffer only.
- Output is disabled (open-circuit) when CAS is at a logic 1.
- 0 V ≤ V_{out} ≤ +5.5 V.

CAPACITANCE (f = 1.0 MHz, T_A = 25°C, V_{CC} = 5 V, periodically sampled rather than 100% tested) (See Note 8)

Parameter	Symbol	Typ	Max	Unit	Notes
Input Capacitance (A0-A5), D _{in}	C _{I1}	4.0	5.0	pF	9
Input Capacitance RAS, CAS, WRITE	C _{I2}	8.0	10	pF	9
Output Capacitance (D _{out})	C _O	5.0	7.0	pF	7, 9

AC OPERATING CONDITIONS AND CHARACTERISTICS (See Notes 3, 9, 14)

READ, WRITE, AND READ-MODIFY-WRITE CYCLES

(V_{DD} = 12 V ± 10%, V_{CC} = 5.0 V ± 10%, V_{BB} = -5.0 V ± 10%, V_{SS} = 0 V, T_A = 0 to 70°C.)

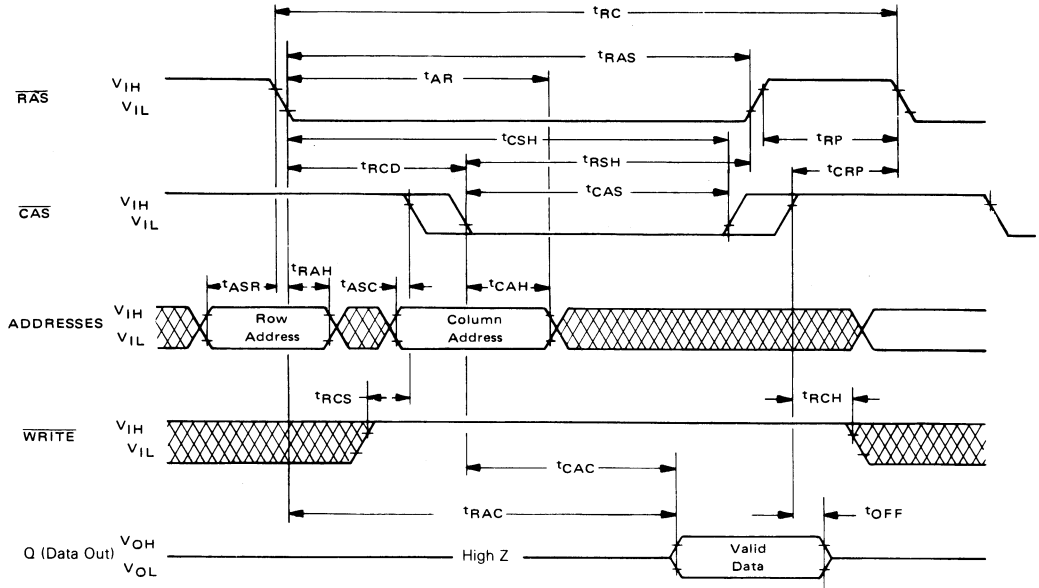
Parameter	Symbol	MCM4116B-15		MCM4116B-20		MCM4116B-25		MCM4116B-30		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Random Read or Write Cycle Time	t _{RC}	375	—	375	—	410	—	480	—	ns	
Read Write Cycle Time	t _{RWC}	375	—	375	—	515	—	660	—	ns	
Access Time from Row Address Strobe	t _{RAC}	—	150	—	200	—	250	—	300	ns	10, 12
Access Time from Column Address Strobe	t _{CAC}	—	100	—	135	—	165	—	200	ns	11, 12
Output Buffer and Turn-off Delay	t _{OFF}	0	50	0	50	0	60	0	60	ns	17
Row Address Strobe Precharge Time	t _{RP}	100	—	120	—	150	—	180	—	ns	
Row Address Strobe Pulse Width	t _{RAS}	150	10,000	200	10,000	250	10,000	300	10,000	ns	
Column Address Strobe Pulse Width	t _{CAS}	100	10,000	135	10,000	165	10,000	200	10,000	ns	
Row to Column Strobe Lead Time	t _{RCD}	20	50	25	65	35	85	60	100	ns	13
Row Address Setup Time	t _{ASR}	0	—	0	—	0	—	0	—	ns	
Row Address Hold Time	t _{RAH}	20	—	25	—	35	—	60	—	ns	
Column Address Setup Time	t _{ASC}	-10	—	-10	—	-10	—	-10	—	ns	
Column Address Hold Time	t _{CAH}	45	—	55	—	75	—	100	—	ns	
Column Address Hold Time Referenced to RAS	t _{AR}	95	—	120	—	160	—	200	—	ns	
Transition Time (Rise and Fall)	t _T	3.0	35	3.0	50	3.0	50	3.0	50	ns	14
Read Command Setup Time	t _{RCS}	0	—	0	—	0	—	0	—	ns	
Read Command Hold Time	t _{RCH}	0	—	0	—	0	—	0	—	ns	
Write Command Hold Time	t _{WCH}	45	—	55	—	75	—	100	—	ns	
Write Command Hold Time Referenced to RAS	t _{WCR}	95	—	120	—	160	—	200	—	ns	
Write Command Pulse Width	t _{WP}	45	—	55	—	75	—	100	—	ns	
Write Command to Row Strobe Lead Time	t _{RWL}	60	—	80	—	100	—	180	—	ns	
Write Command to Column Strobe Lead Time	t _{CWL}	60	—	80	—	100	—	180	—	ns	
Data in Setup Time	t _{DS}	0	—	0	—	0	—	0	—	ns	15
Data in Hold Time	t _{DH}	45	—	55	—	75	—	100	—	ns	15
Data in Hold Time Referenced to RAS	t _{DHR}	95	—	120	—	160	—	200	—	ns	
Column to Row Strobe Precharge Time	t _{CRP}	-20	—	-20	—	-20	—	-20	—	ns	
RAS Hold Time	t _{RSH}	100	—	135	—	165	—	200	—	ns	
Refresh Period	t _{RFSH}	—	2.0	—	2.0	—	2.0	—	2.0	ms	
WRITE Command Setup Time	t _{WCS}	-20	—	-20	—	-20	—	-20	—	ns	
CAS to WRITE Delay	t _{CWD}	70	—	95	—	125	—	180	—	ns	16
RAS to WRITE Delay	t _{RWD}	120	—	160	—	210	—	280	—	ns	16
CAS Precharge Time (Page mode cycle only)	t _{CP}	60	—	80	—	100	—	100	—	ns	
Page Mode Cycle Time	t _{PC}	170	—	225	—	275	—	325	—	ns	
CAS Hold Time	t _{CSh}	150	—	200	—	250	—	300	—	ns	

NOTES: (continued)

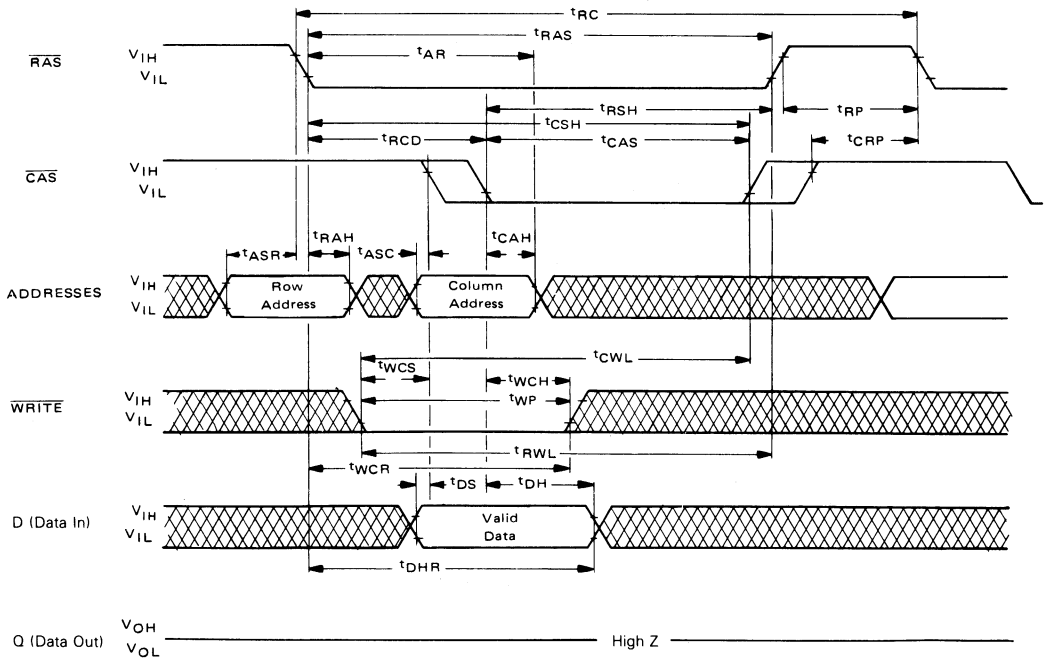
8. Capacitance measured with a Boonton Meter or effective capacitance calculated from the equation: $C = \frac{I \Delta t}{\Delta V}$.
9. AC measurements assume $t_T = 5.0$ ns.
10. Assumes that $t_{RCD} + t_T \leq t_{RCD}(\text{max})$.
11. Assumes that $t_{RCD} + t_T \geq t_{RCD}(\text{max})$.
12. Measured with a load circuit equivalent to 2 TTL loads and 100 pF.
13. Operation within the $t_{RCD}(\text{max})$ limit ensures that $t_{RAC}(\text{max})$ can be met. $t_{RCD}(\text{max})$ is specified as a reference point only; if t_{RCD} is greater than the specified $t_{RCD}(\text{max})$ limit, then access time is controlled exclusively by t_{CAC} .
14. V_{IHC} (min) or V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IHC} or V_{IH} and V_{IL}.
15. These parameters are referenced to $\overline{\text{CAS}}$ leading edge in random write cycles and to $\overline{\text{WRITE}}$ leading edge in delayed write or read-modify-write cycles.
16. t_{WCS} , t_{CWD} and t_{RWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only: If $t_{WCS} \geq t_{WCS}(\text{min})$, the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{CWD} \geq t_{CWD}(\text{min})$ and $t_{RWD} \geq t_{RWD}(\text{min})$, the cycle is a read-write cycle and the data out will contain data read from the selected cell; if neither of the above sets of conditions is satisfied the condition of the data out (at access time) is indeterminate.
17. Assumes that $t_{CRP} > 50$ ns.

DRAM

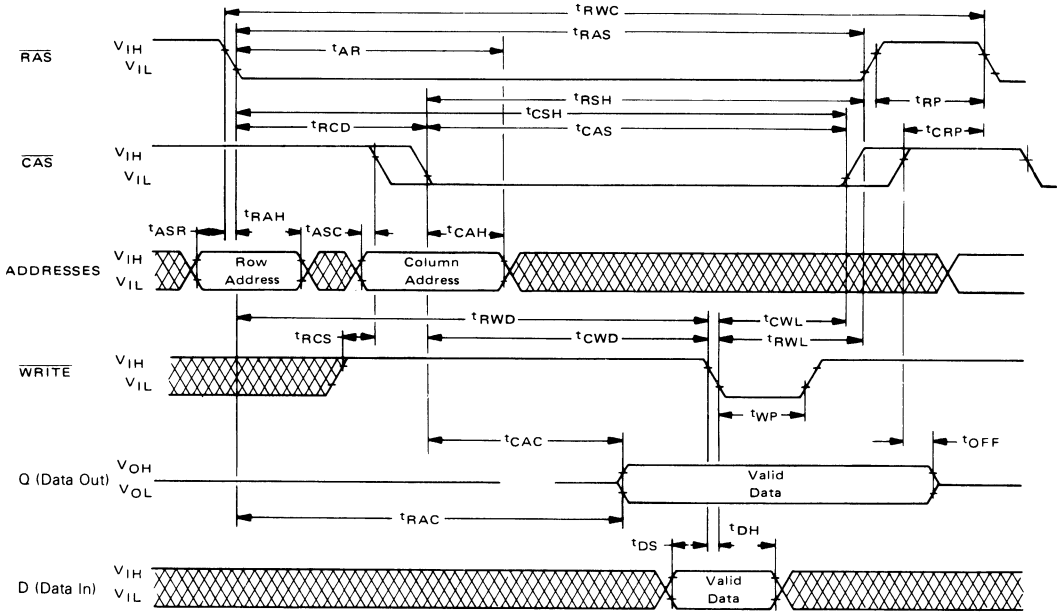
READ CYCLE TIMING



WRITE CYCLE TIMING

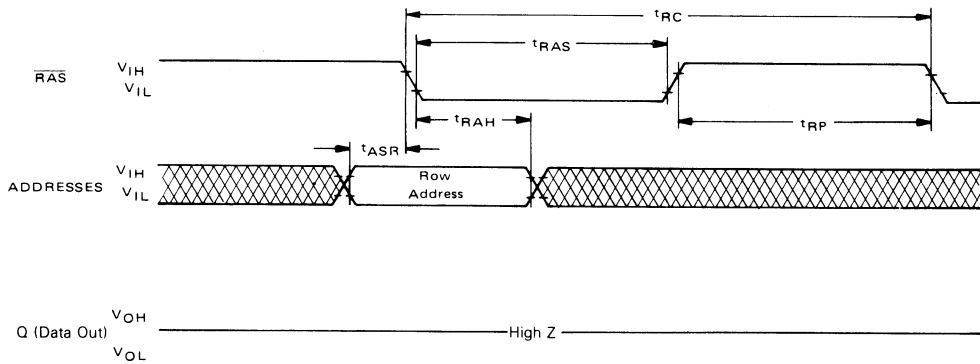


READ-WRITE/READ-MODIFY-WRITE CYCLE

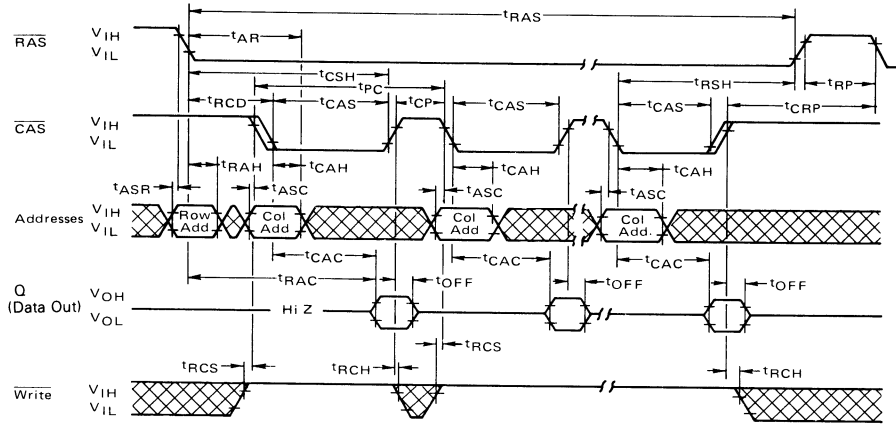


RAS ONLY REFRESH TIMING

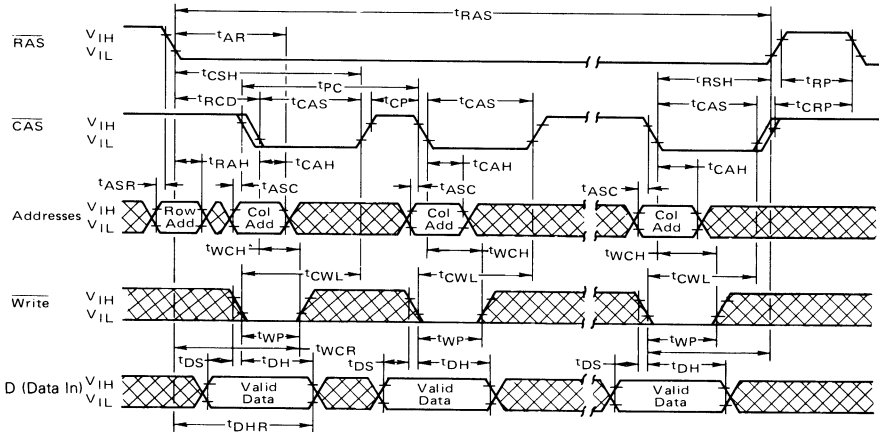
Note: CAS = VIH, WRITE = Don't Care



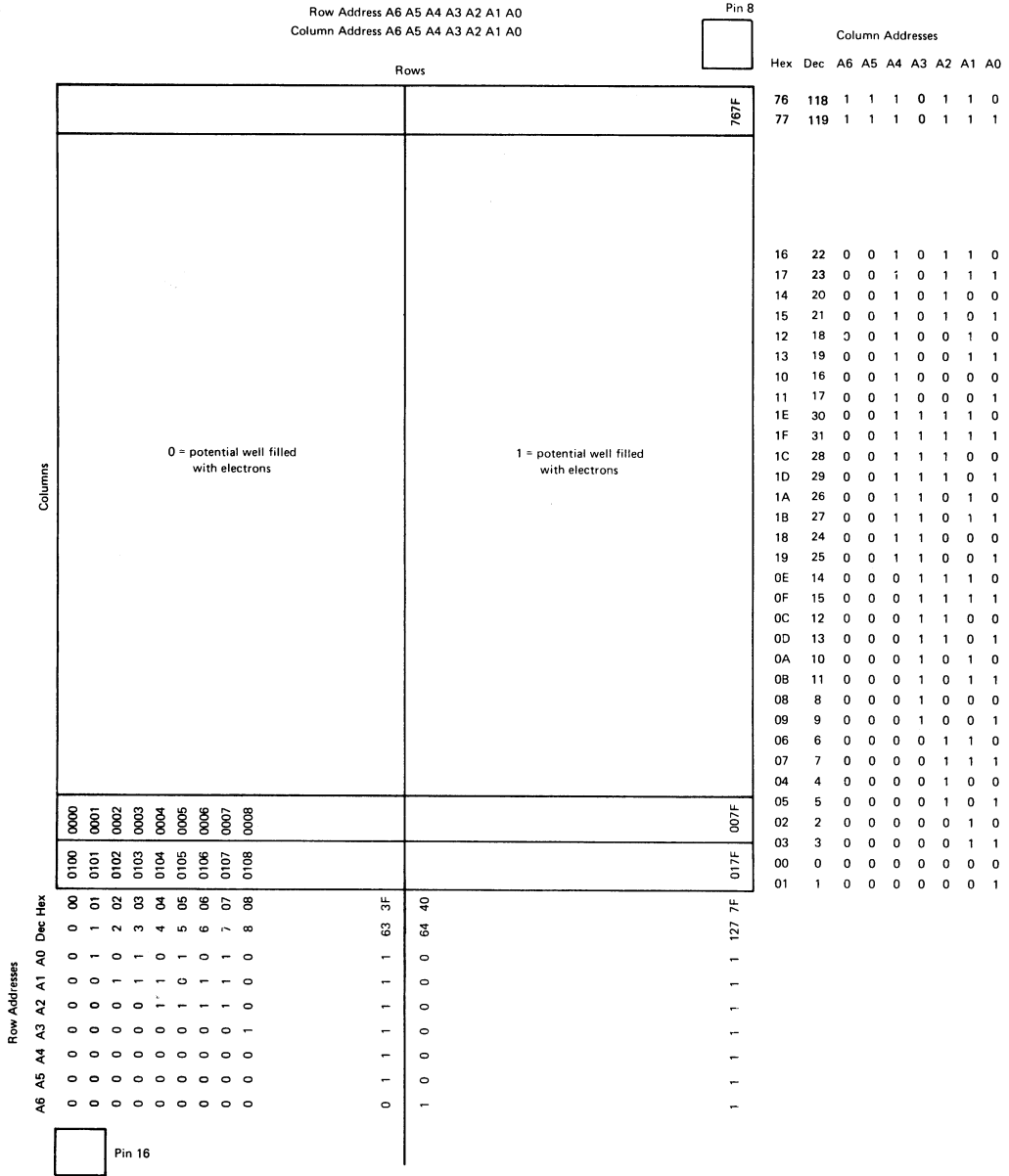
PAGE MODE READ CYCLE



PAGE MODE WRITE CYCLE



MCM4116B BIT ADDRESS MAP



DRAM